ISSN 2250-3153

Delay and Optimization of Random Number Generator

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Abstract- A digital system is tested and diagnosed during its lifetime on numerous occasions. Test and diagnosis must be quick and have very high fault coverage. One way to ensure this is to specify test as one of the system functions, so it becomes self-test. The system has several PCBs, each of which, in turn has multiple chips. The system controller can activate self-test simultaneously on all PCBs. These test result help to isolate faulty chips and boards. In this project Linear Feedback Shift Register (LFSR) method has been used to generate pseudo random tests. This method uses very little hardware and is currently the preferred built in self test pattern generation method. Mentor Graphics Design architect tool was used for designing of circuit. It was also used for measuring power and delay associated with the circuit for different technologies.

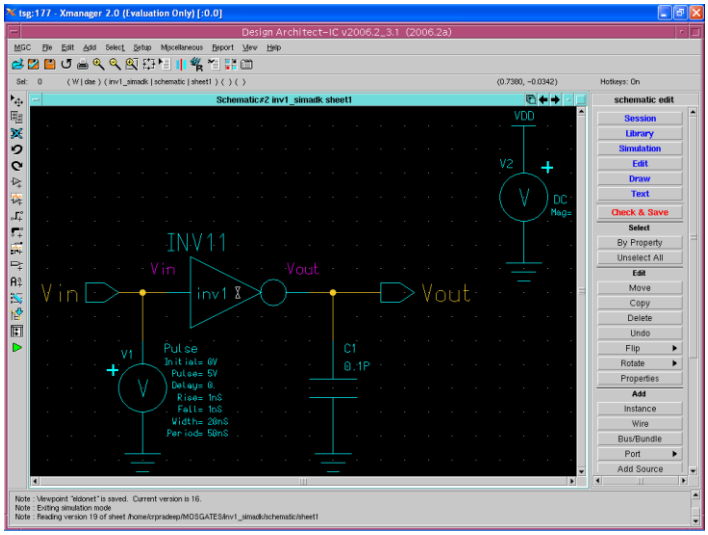
Index Terms- AT&T circa, Random Generator, TSMC Technology, Linear Feedback Shift Register

I. INTRODUCTION

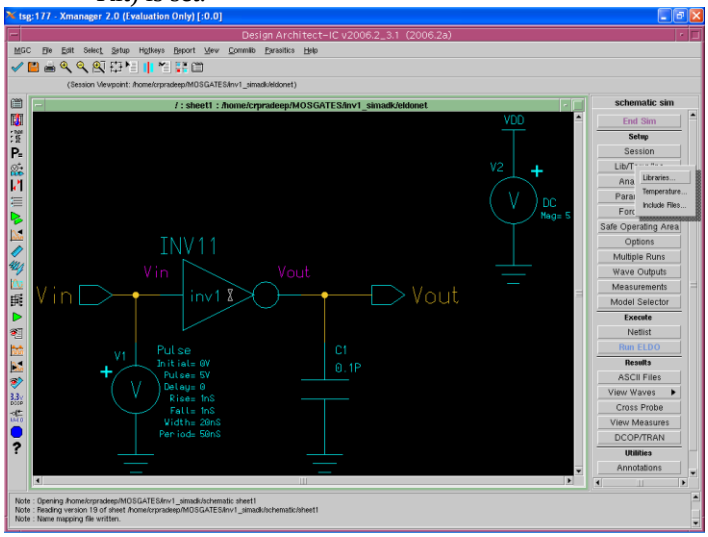
A digital system is tested and diagnosed during its lifetime on numerous occasions. Test and diagnosis must be quick and have very high fault coverage. At the highest level of systems test, the testing function is frequently implemented in software. Many digital systems designed at AT&T circa 1987 had self-test, usually implemented in software [5]. Its most common use was in maintenance and repair diagnostics. Although this approach provided flexibility, it also had disadvantages. The fault coverage and the diagnostic resolution of those software-implemented tests were not as high as desired. The diagnostic resolution may be poor because the software must test parts that are difficult to test, and therefore it may not effectively determine which part is at fault. Also, software tests can be long, slow and expensive to develop. It is also most effective to consider testing as early in the design cycle as possible. These lead to schedule slippages for product introduction.

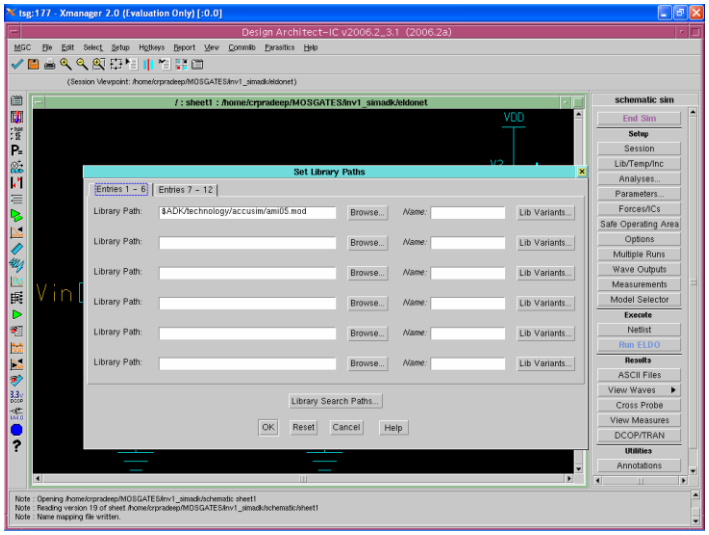
II. TRANSIENT SIMULATION AND MEASUREMENT

Step 1:-Setting the test bench for simulation.

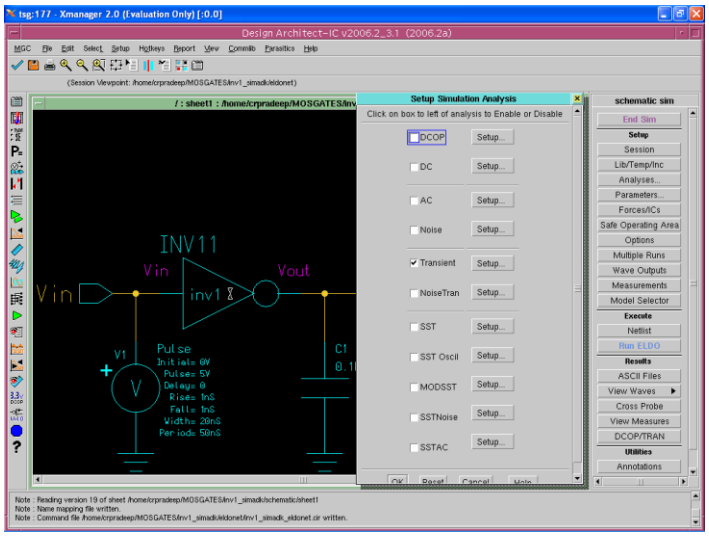


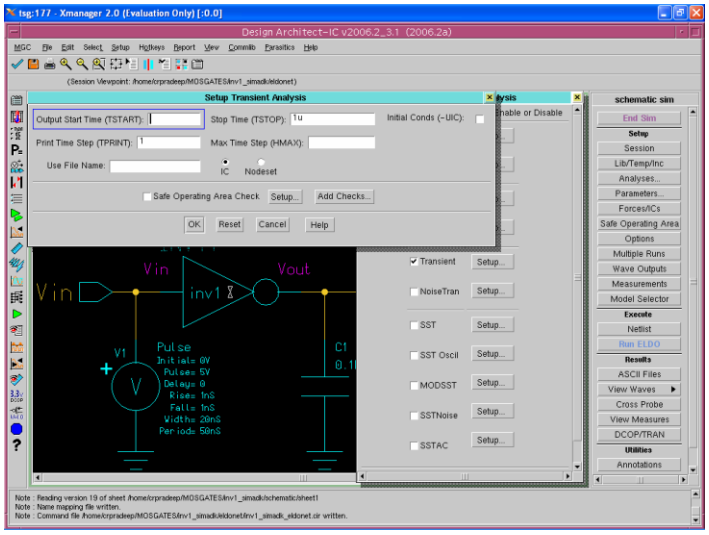
Step 2:- Simulation Settings – Library Settings
Simulation mode is entered and then the library (ADK Kit) is set.



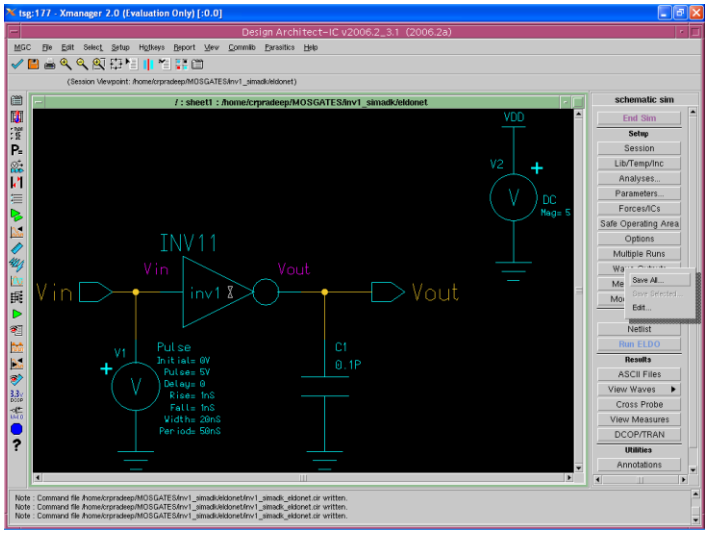


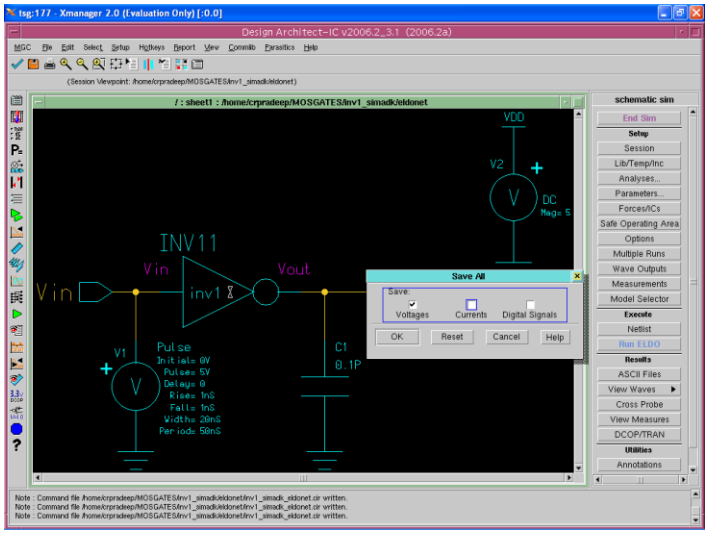
Sep 3:-Simulation Settings-Setup is then made for Transient analysis.





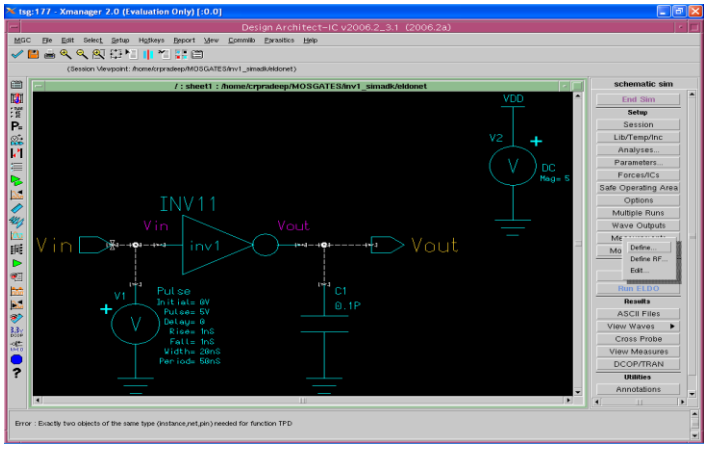
Stop:-1 u
Step 4:-Simulation Settings- Ports for Wave Outputs are selected



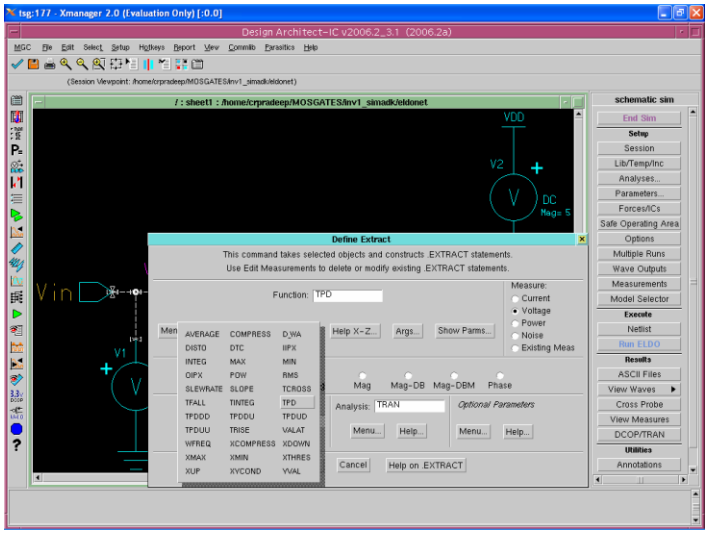


III. MEASUREMENT OF PROPAGATION DELAY(TPD)

Here both Input and Output signals are selected. Ctrl key is used for multiple selections.

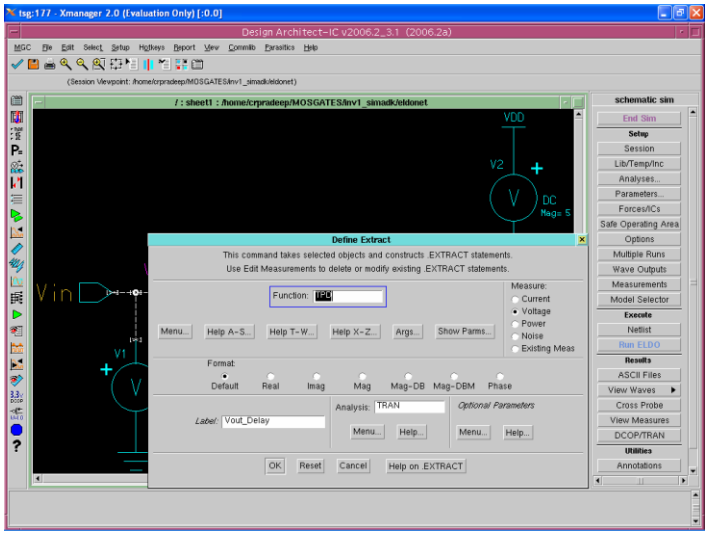


Select Menu->TPD

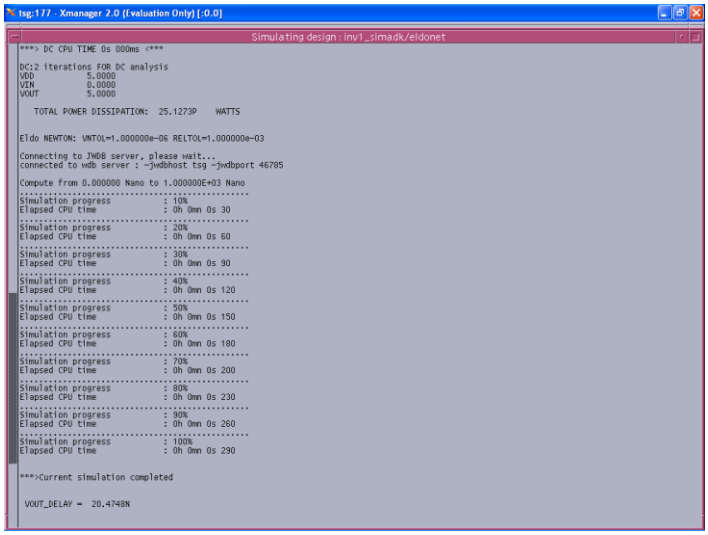


V_{OUT} Delay is written in the label > OK

Run



Run ELDO ->In the transcript we can see the total power dissipation and also the V_{out} Delay.

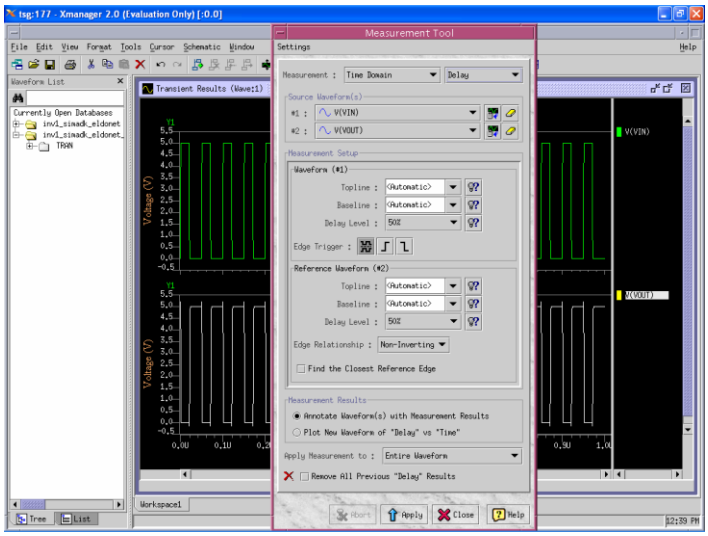


We can use the measurement for calculating the average voltage, power etc.

We can also measure the delay in the waveform viewer using "Measurement Tool"

Click on the V (V_{IN}) and click on the waveform database in the Measurement tool.

Similarly for V (V_{OUT}).



Click on Apply and then close the Measurement tool in order to get the below screen.

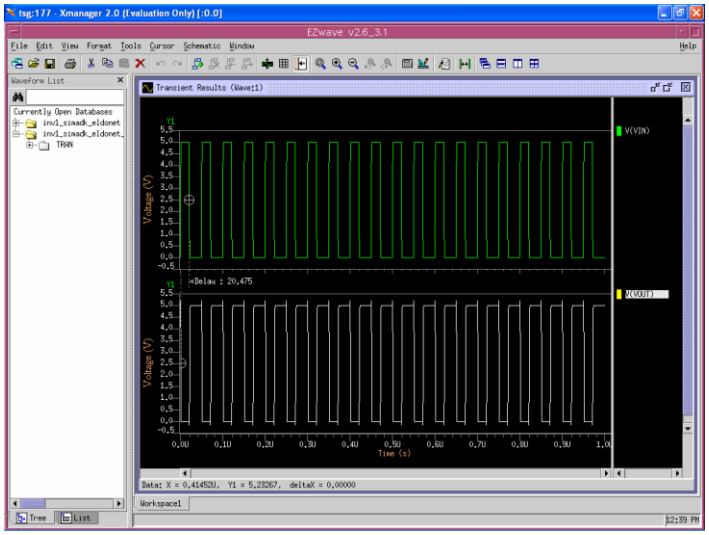


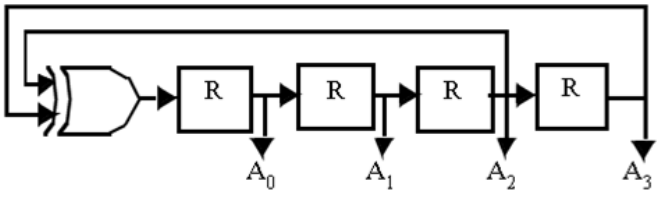
Figure 1: Block diagram of generate pseudo random

Random number generator used in the project uses linear feedback shift register (LFSR) to generate pseudo random tests. This method uses very little hardware and is currently the preferred BIST pattern generation method [1-2]. The circuit designed uses positive edge triggered D-Flip Flops as registers and a XOR Gate for implementing random number generation [3].

IV. RANDOM NUMBER GENERATORS

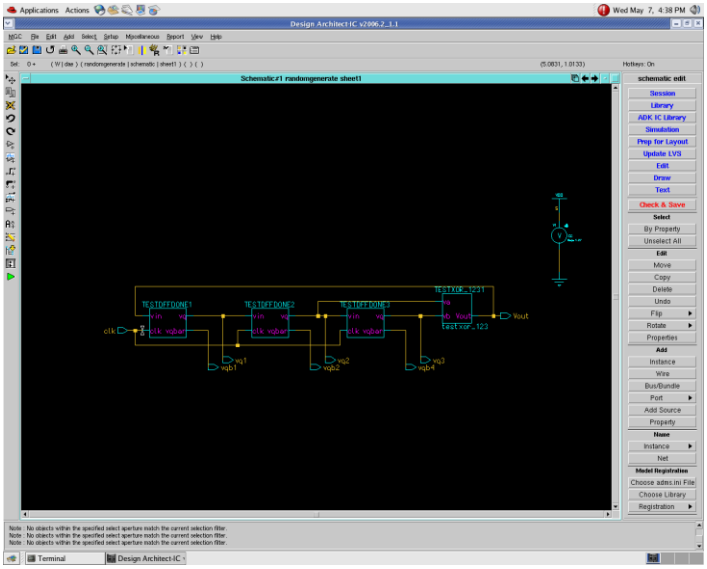
The benefit of BIST is lower test development cost, because BIST can be automatically added to a circuit with a CAD tool. In addition, BIST generally provides 90 to 95% fault coverage, and even 99% in exceptional cases. The test engineer needs no longer worry about back driving problem of in-circuit test, or how much memory is available in the ATE. BIST always requires added circuit hardware for a test controller to operate the testing process, design for testability hardware in the circuit to improve fault coverage during BIST, a hardware pattern generator to generate test patterns algorithmically during testing, and some form of hardware response compactor to compact the circuit response during testing [3]. The relative costs of added logic gates are declining, because hardware continue to become cheaper, but the relative costs of added long wires for test mode control are not really decreasing. Also, the test hardware can consume extra power, which is an additional cost. Since the BIST circuitry uses chip area, a final BIST cost is a decrease in the chip yield and chip reliability, due to the increased area. BIST feasibility for a system must be evaluated using benefit-cost analysis, in the context of assessing total life cycle costs.

For design and test development, BIST significantly reduces the costs of automatic test pattern generalizes (ATPG), also reduces the likelihood of disastrous product introduction delays because fully- designed system cannot be tested [4]. Such a delay has occurred in the Intel Merced project due to unexpected delays in inserting testability hardware into the chip, and fabrication line problems. There is a slight cost increase due to BIST in design and test development, because of the added time required to design and adds pattern generators, response compacters, and testability hardware. However, our experience is that this is less costly than test development with ATPC.

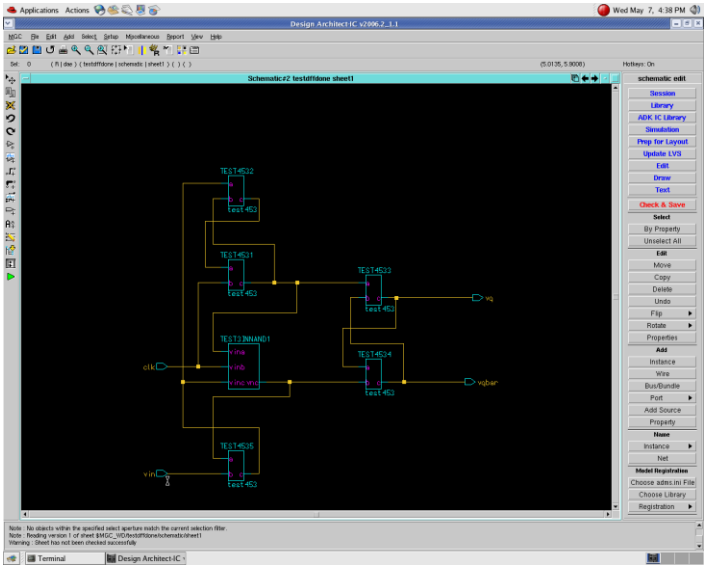


V. SIMULATION

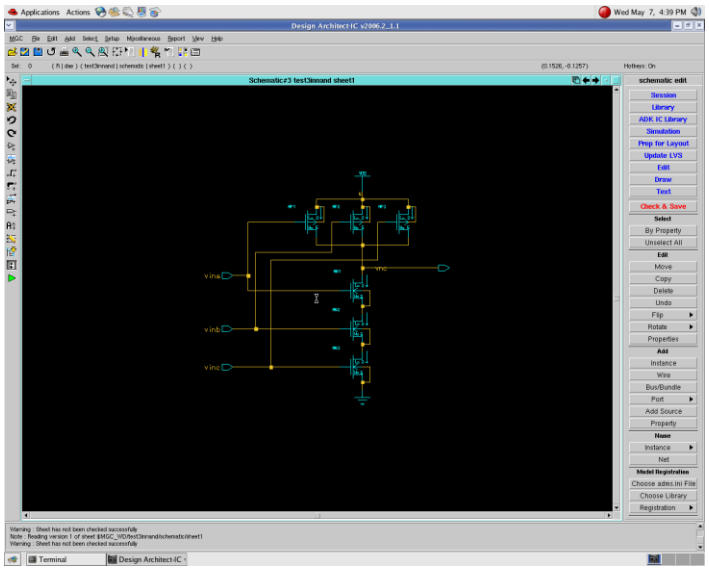
A. *Circuit Designed*

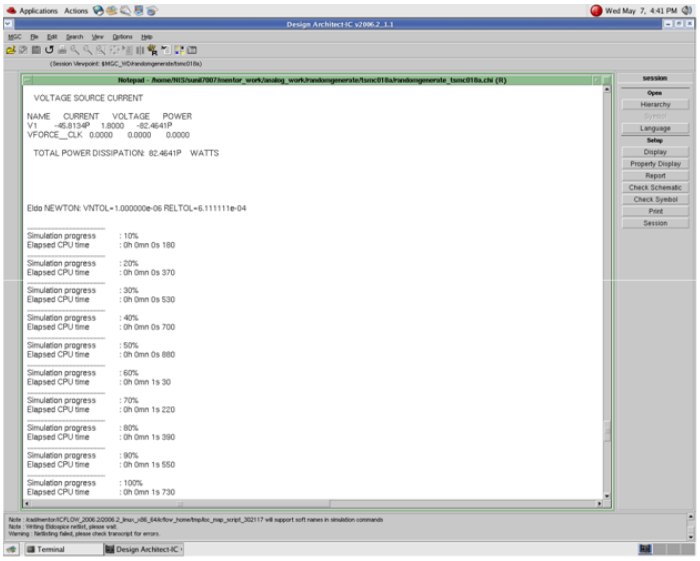


Sub-Circuit of random number generator circuit: Positive edge triggered D-flip flop



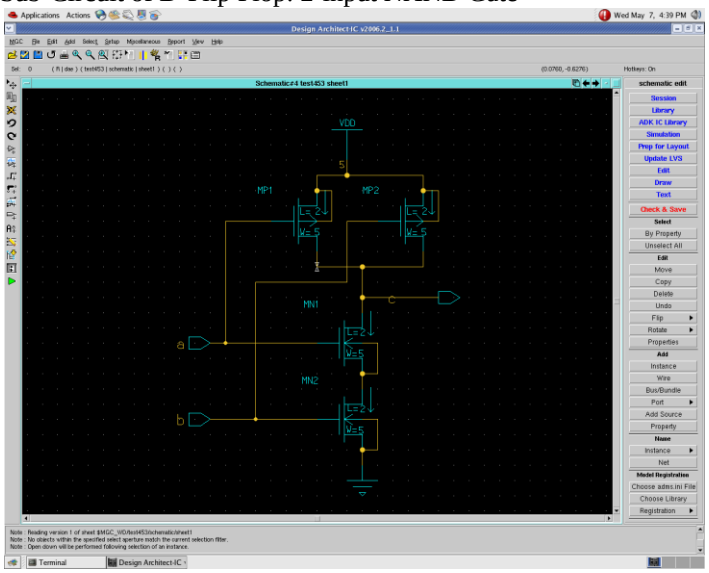
Sub-Circuit of D-Flip Flop: 3-input NAND Gate

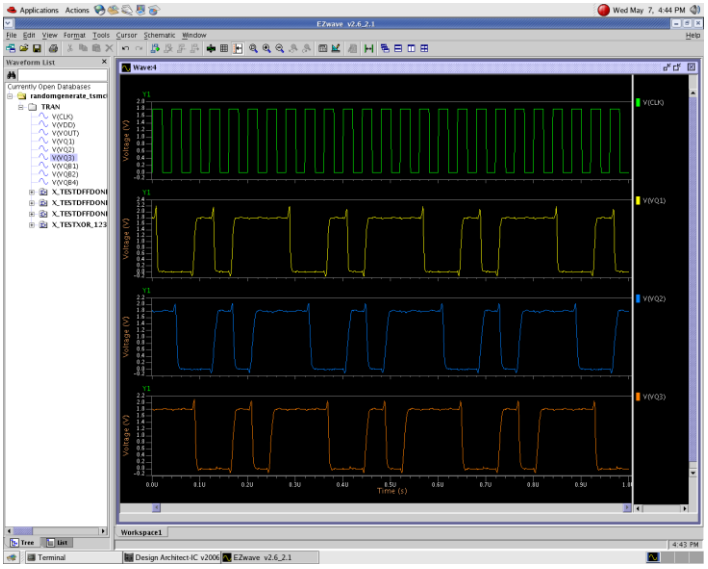




B. Power dissipation results of the circuit.

Sub-Circuit of D-Flip Flop: 2-input NAND Gate





VI. RESULTS

By applying the various technologies the result obtained were as follows:

Technology	Power	Delay
AMI05	82.46 pwatts	16.459ns
AMI12	83.00 pwatts	10.688ns
TSMC035	86.59 pwatts	12.36ns
TSMC025	375.54 pwatts	14.78ns
TSMC018	588.96 pwatts	14.43ns

VII. CONCLUSION

From the results the various power and delay values for random number, generator circuit was obtained. In AMI technology class ami12, the delay was 10.688ns, which is less as compared to ami05. Hence the former one was better for the

designing the circuit. In TSMC technology, class tsmc035 had the least power taken and the smallest propagation delay hence most suitable for the circuit designed. The tsmc018 technology has the least size hence can be preferred where the area of the hardware needed is small.

ACKNOWLEDGMENT

Special thanks to Mr. R. K. Patel Head of department of K.G. Polytechnic, Raigarh for his encouragements.The authors also express their greatly thanks to all persons who had concern to support in preparing this paper.

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