

# A Carrier Based Compact Model for Long Channel Undoped and Doped Body Symmetric Double Gate MOSFETS

Neha Goel, Dr.Vandana Nath

Electronics and Communication Engineering, USIT,  
Guru Gobind Singh Indraprastha University, India

**Abstract-** Double gate MOSFET is widely used for sub-50nm technology of transistor design .They have immunity to short channel effects, reduced leakage current and high scaling potential. The single gate Silicon-on-insulator (SOI) devices give improved circuit speed and power consumption .But as the transistor size is reduced the close proximity between source and drain reduces the ability of the gate electrode to control the flow of current and potential distribution in the channel. To reduce SCE we need increase gate to channel coupling with respect to source/drain to channel coupling. This paper deals with the compact modeling of long channel undoped and doped symmetric double-gate MOSFET. The formulation starts with the solution of Poisson's equation which is then coupled to the Pao-Sah current equation to obtain the analytical drain-current model in terms of carrier concentration. The performance analysis will be done by using the model.

**Index Terms-** Symmetric DGMOS, Doped body, undoped body, Compact model, Volume inversion.

## I. INTRODUCTION

Double gate MOSFET is widely used for sub-45nm technology of transistor design .They have immunity to short channel effects, reduced leakage current, nearly ideal sub-threshold swing and high scaling potential. The single gate Silicon-on-insulator (SOI) devices give improved circuit speed and power consumption .But as the transistor size is reduced the close proximity between source and drain reduces the ability of the gate electrode to control the flow of current and potential distribution in the channel. To reduce SCE we need to increase the gate to channel coupling with respect to source/drain to channel coupling. Several technological approaches can be followed to design multiple gate MOSFETs. The various proposed architectures differ mainly by the number of gates and by the orientation of the conduction channel. We can define three main types of multiple gate devices: planar transistors, in which the gates and the channel are horizontal, FinFETs, in which the channel is vertical and the conduction is parallel to the wafer surface and the vertical transistors, in which the conduction direction is vertical.

This paper deals with the compact modeling of long channel undoped and doped symmetric double-gate MOSFET. While modeling DG MOSFETs, we have to take a different approach

from that of CMOS Technology as it has unique physical effects such as the two conducting interface coupling, volume inversion and carrier energy level quantization. Highly accurate physics based compact models are required which are computationally efficient. These requirements are easier to meet in the case of undoped body MOSFETs because of the absence of fixed charge in the channel.

Recently, extensive study has been performed on the DG MOSFETs device physics.

Some researchers have solved 1-D Poisson's equation for DGMOS to derive the analytical solution for surface potential and inversion layer charge density. But due to the complexity and need to solve a number of transcendental equations and auxiliary functions, these models needs more efforts to be implemented in the circuit simulator. Other groups used the charge based approach and focused on analytical charge and current expressions. These models provide simplified derivation of I-V characteristic but require special assumptions and approximations that compromise the physical detail in describing the device behavior.

A fundamental complication of DG MOS's is the existence of multiple interfaces that coupled to each other. As a result, the drain current can't be fully described by an equation with respect to only source and drain surface potential but it requires the potential at the center of the Si film at the source and drain each.

This carrier based method avoids the difficulties in calculating the surface and Si-film centric potential as long as the carrier concentrations at the boundaries are known. The calculations of the carrier concentrations are obtained directly by using Poisson's equation and thus we use minimum approximations. The model is formulated from the solution of the Poisson's equation and Pao-Sah drift-diffusion current expression and covers all three operating regions of a DG MOSFET: linear, active and saturation. Also in this model, we are ignoring some second order physical effects such as Short Channel Effects, Drain induced barrier lowering and quantum effects for the sake of simplicity.

The paper is arranged as follows:

- 1) Abstract
- 2) Introduction
- 3) Model Discussion for undoped body DGMOS
- 4) Model Formulation for undoped body DGMOS
- 5) Results and Discussions

6) Conclusion

II. MODEL DISCUSSION FOR UNDOPED BODY DGMOS

Fig. 1 shows the energy level distribution diagrams of a symmetric double-gate MOSFET. The same voltage is applied to the two gates with the same work function to make them work as symmetric DGMOS. The voltage levels are referred to the electron quasi - fermi level of the source as there is no contact to the silicon body. Assuming that the quasi-fermi level is constant across the silicon film direction so that the device current flows only along the channel (y direction). The formulation starts with 1-D Poisson's equation along the vertical direction considering the gradual channel approximation.

$$\frac{d^2\phi}{dx^2} = \frac{qn}{\epsilon_{si}} \tag{1}$$

Where, n and  $\phi$  are the mobile electron concentration and spatial electrostatics respectively,  $\epsilon_{si}$  is the permittivity of the silicon material. The transport due to holes is minimum in the n-channel and hence can be ignored. According to Boltzmann statistics, the mobile electron concentration is expressed by the potential

$$n = n_i \exp\left(\frac{q(\phi - \phi_f)}{KT}\right) \tag{2a}$$

And

$$n_o = n_i \exp\left(\frac{q(\phi_o - \phi_f)}{KT}\right) \tag{2b}$$

Where  $n_i$  and  $n_o$  are the intrinsic carrier concentration and the induced carrier concentration respectively at the reference point in x-direction.

The spatial derivative of the electron concentration from (2a) is written as

$$\frac{d\phi}{dx} = \frac{KT}{qn} \frac{dn}{dx} \tag{3}$$

Again differentiating the above equation we get

$$\frac{d^2\phi}{dx^2} = \frac{KT}{qn} \frac{d^2n}{dx^2} - \frac{KT}{qn^2} \left(\frac{dn}{dx}\right)^2 \tag{4}$$

Substituting (4) into (1) gives the equation for the electron concentration as

$$\frac{d^2n}{dx^2} = \frac{1}{n} \left(\frac{dn}{dx}\right)^2 + \frac{q^2n^2}{\epsilon_{si}KT} \tag{5}$$

There is a geometry symmetric point in the silicon film center due to the symmetric characteristic of double-gate MOSFETs. The symmetry boundary condition of a symmetric double gate MOSFET sets the electric field in the center of the silicon film to be zero. Thus, the reference coordinate takes the center of the silicon film as the coordinate point of  $x = 0$ . For consistency the value of the  $n(x)$  at  $x=0$  is taken as  $n_o$ .

$$n(x) = \frac{n_o}{\cos^2\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}x\right]} \tag{6}$$

Substituting (6) into (2a) we get

$$(\phi(x) - \phi_f) = \frac{KT}{q} \ln\left[\frac{n_o}{n_i}\right] + \frac{KT}{q} \ln\left[\sec^2\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}x\right]\right] \tag{7}$$

The electric field distribution is obtained by differentiating equation (7)

$$E(x) = \left[\frac{2n_oKT}{\epsilon_{si}}\right]^{1/2} \tan\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}x\right] \tag{8}$$

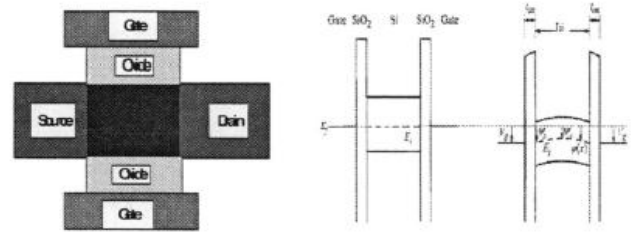


Fig.1 Structure and Energy Level Diagram of undoped DGMOS

The symmetry of the boundary condition of the DGMOS allows the surface potential and the surface electric field to be calculated from equation (7) and (8) respectively.

$$\phi(x) = \phi_f + \frac{KT}{q} \ln\left[\frac{n_o}{n_i}\right] \left[\sec^2\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}\frac{t_{si}}{2}\right]\right] \tag{9}$$

$$E(x) = \left[\frac{2n_oKT}{\epsilon_{si}}\right]^{1/2} \tan\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}\frac{t_{si}}{2}\right] \tag{10}$$

Defining  $Q_{in} = q \int_0^{\frac{t_{si}}{2}} n(x) dx$  we can calculate half of the total inversion charge.

$$Q_{in} = (2 \epsilon_{si} KTn_o)^{\frac{1}{2}} \tan\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}\frac{t_{si}}{2}\right] \tag{11}$$

The surface potential, concentration and field need to obey the Gauss's law for the applied gate to source voltage. So, we have  $V_{gs} - \phi_m = \phi_s + Q_{in}/C_{ox}$  (12)

Substituting the expressions for surface potential and inversion charge in (12) we get

$$V_{gs} - \phi_m = \phi_f + \frac{KT}{q} \ln\left[\frac{n_o}{n_i}\right] \left[\sec^2\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}\frac{t_{si}}{2}\right]\right] + \frac{t_{ox}}{\epsilon_{ox}} (2 \epsilon_{si} KTn_o)^{\frac{1}{2}} \tan\left[\left(\frac{q^2n_o}{2\epsilon_{si}KT}\right)^{\frac{1}{2}}\frac{t_{si}}{2}\right] \tag{13}$$

Using (13)  $n_o$  is first solved for a given value of  $V_{gs}$ . along the channel direction the quasi -Fermi potential varies from  $\phi_f = 0$  at the source end to  $\phi_f = V_{ds}$  at the drain end.

This expression is useful because of its exactness, solid physics background, and the analytical characteristics in compact model construction.

The current continuity principle requires the current to be constant and independent of the quasi -Fermi potential, following which we can determine the functional dependence between  $\phi_f(y)$  and  $n_o(y)$ .

Following the Pao- Sah current formulation which assumes that the drift-diffusion transport is valid for the long channel DGMOS , the drain current is obtained by integrating  $I_{ds} dy$  from the source to the drain ,expressed as  $\left(\frac{d\phi_f}{dn_o}\right)\left(\frac{dn_o}{dy}\right)$

$$I_{ds} = \mu \frac{W}{L} \int_0^{V_{ds}} Q_i(\phi_f) d\phi_f = \mu \frac{W}{L} \int_{n_{0s}}^{n_{0d}} Q_i(n_o) \frac{d\phi_f}{dn_o} dn_o \tag{14}$$

Where  $n_{0s}$  and  $n_{0d}$  are the solutions of (13) corresponding to  $\phi_f=0$  to  $V_{ds}$  respectively,  $\mu$  is the effective mobility and  $W$  and  $L$  are the channel width and length of the DGMOS respectively.

Calculating  $\frac{d\phi_f}{dn_0}$  from equation (13) and substituting it in (14)

We get

$$I_{ds} = 2 * \mu \frac{W\epsilon_{si}}{L} \left(\frac{2KT}{q}\right)^2 \left\{ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \tan \left[ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \frac{t_{si}}{2} \right] - \frac{q^2 n_0 t_{si}}{8KT\epsilon_{si}} + \frac{t_{ox}}{\epsilon_{ox}} \frac{q^2 n_0 \epsilon_{si}}{KT} \tan^2 \left[ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \frac{t_{si}}{2} \right] \right\} n_{0d} \quad (15)$$

As the charge formulation accounts for only half of the channel, so the final current for symmetric DGMOS is doubled in (15).

### III. MODEL FORMULATION FOR DOPED BODY DGMOS

In the doped body DGMOS there are significant mobile charges and fixed charges so the Gauss's law changes to

$$V_{gs} - \phi_m = \phi_s + \frac{Q_{in}}{C_{ox}} + \frac{Q_{fix}}{C_{ox}} \quad (16)$$

Where  $Q_{fix}$  is fixed charge and its value is:

$$Q_{fix} = q^2 * n_a * \frac{t_{si}}{KT} \quad (17)$$

So the value of  $V_{gs}$  is increased which leads to an increase in the threshold voltage.

$$V_{gs} - \phi_m = \phi_f + \frac{KT}{q} \ln \left[ \frac{n_0}{n_i} \right] \left[ \sec^2 \left[ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \frac{t_{si}}{2} \right] \right] + \frac{t_{ox}}{\epsilon_{ox}} (\epsilon_{si} KT n_0)^{\frac{1}{2}} \tan \left[ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \frac{t_{si}}{2} \right] + \frac{Q_{fix}}{C_{ox}} \quad (18)$$

We'll calculate the value of  $n_{0d}$  and  $n_{0s}$  using the previous considerations and using the Pao-Sah drift-diffusion current equation the value of the drain current is:

$$I_{ds} = 2 * \mu \frac{W\epsilon_{si}}{L} \left(\frac{2KT}{q}\right)^2 \left\{ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \tan \left[ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \frac{t_{si}}{2} \right] - \frac{q^2 n_0 t_{si}}{8KT\epsilon_{si}} + \frac{t_{ox}}{\epsilon_{ox}} \frac{q^2 n_0 \epsilon_{si}}{KT} \tan^2 \left[ \left(\frac{q^2 n_0}{2\epsilon_{si}KT}\right)^{\frac{1}{2}} \frac{t_{si}}{2} \right] \right\} n_{0d} \quad (19)$$

### IV. RESULTS AND DISCUSSIONS.

We use this model to simulate an undoped double-gate MOSFET with the channel length of  $2\mu m$  and gate oxide thickness of  $2nm$ . Fig.2 show the DG MOSFET current voltage characteristics predicted by the derived analytical model with the constant mobility of  $300 cm^2 / V.s$ .

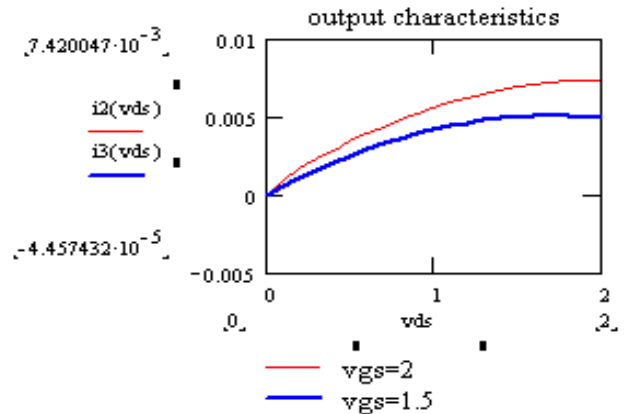


Fig.2 I-V Characteristics of undoped body Symmetric DGMOSFET

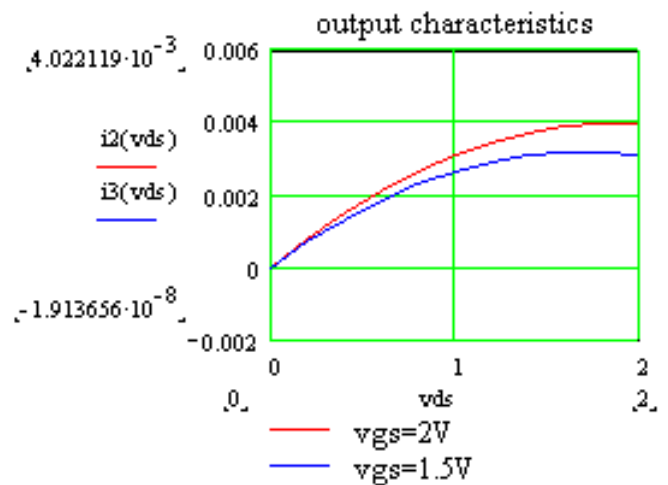


Fig.3: I-V Characteristics of doped body Symmetric DGMOSFET

#### A. Transconductance curve:

The transconductance curves of the two types of symmetric DGMOS clearly shows that as the concentration of the channel increases the threshold voltage also increases. So the threshold voltage for undoped body DGMOS is lower than the doped body DGMOS.

Also as we can see from fig.4 as the silicon film thickness  $t_{si}$  increases the subthreshold current also increases so the value of  $t_{si}$  should be kept low but more than  $2nm$ .

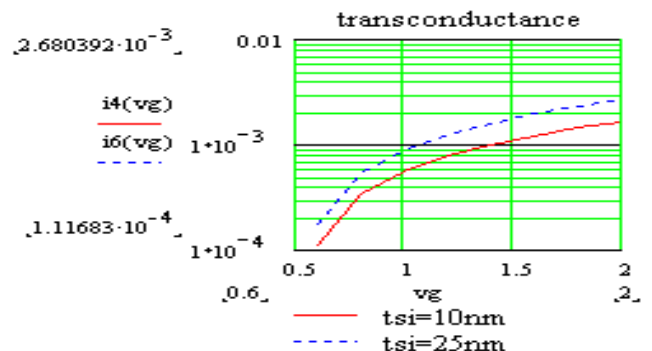


Fig.4: Transconductance characteristics of undoped body Symmetric DGMOSFET

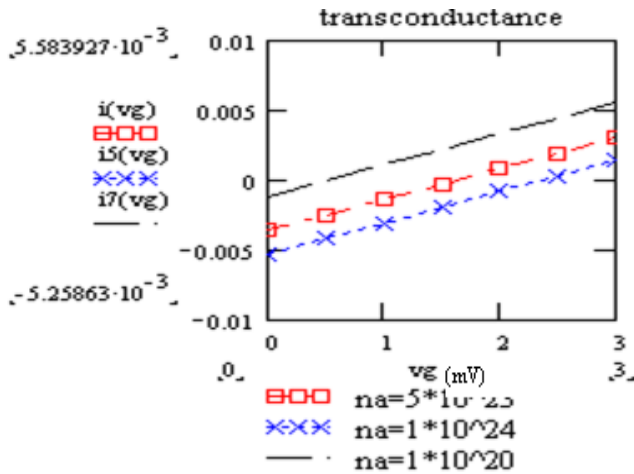
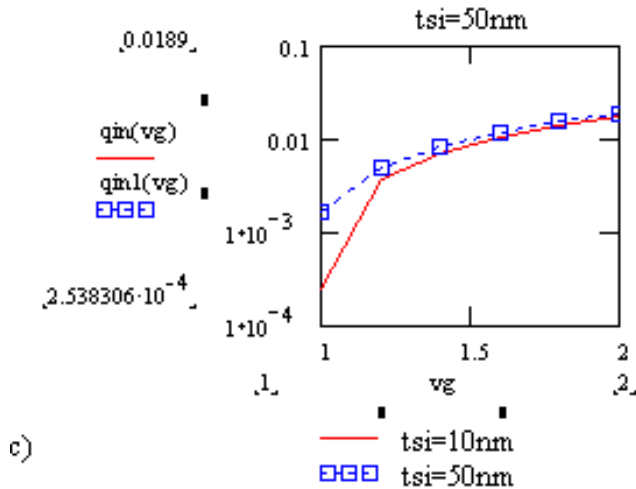


Fig.5: Transconductance characteristics of doped body Symmetric DGMOSFET

**B. Volume inversion**

Fig.5 demonstrates the inversion charge versus gate voltage characteristics. The silicon film thickness affects the amount of sub-threshold inversion charge but has no effect on the strong inversion charge density. This verified the existence of the volume inversion and implies that decrease of the silicon thickness can effectively control the sub-threshold region leakage current. It illustrates a potential weakness in the used of undoped symmetric double MOSFETs for nano-CMOS application. To optimize the device performance, the silicon film thickness should be reduced to suppress the off-current.



c)

Fig.6: Inversion charge density per unit area is plotted at different values of Vgs and studied at tsi=10nm and tsi=50nm

**V. CONCLUSIONS**

In this paper a carrier based analytical model for long channel undoped body symmetric DGMOS is studied using carrier based approach. The drain is described by a single explicit equation with respect to the carrier concentration at the boundaries that is valid for all region of operation. This model is further extended to develop the model for doped symmetric DGMOS. Also we can check the performance of this model and compare it with the 2-D numerical simulation so as to check for the validity of the model. We can also derive the capacitance model for both the devices and study the radio-frequency characteristics of the two devices.

**REFERENCES**

- [1] Zhang L.;J.He;Liu F.;Zhang J.;Song Y., "A unified charge based model for symmetric DGMOSFETs valid for both heavily doped body and undoped body", in MIXDES 2008 Poland 19-21 June 2008 ,pp-367-372,2008.
- [2] Yadav K.Vinay;Rana K.Ashwani, "Impact of Channel Doping on DGMOSFET Parameters in Nano Regime-TCAD Simulation", in International Journal of Computer Applications (0975 – 8887) Vol. 37– No.11, January 2012,pp-36-40,2012.
- [3] Gupta, R.S.; Sharma, N.; Bansal, J.; Chaujar, R.; Gupta, M., "Two dimensional analytical modeling of multi-layered dielectric G4 MOSFET-A novel design", in Recent Advances in Microwave Theory and Applications, 2008. MICROWAVE 2008., pp47 – 49,2008.
- [4] Yuan Taur; Jooyoung Song; Bo Yu, "Compact modeling of multiple-gate MOSFETs", in Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE, pp. 257 – 264,2008.
- [5] Kasturi, P.; Saxena, M.; Gupta, M.; Gupta, R.S., "Dual Material Double-Layer Gate Stack SON MOSFET: A Novel Architecture for Enhanced Analog Performance—Part I: Impact of Gate Metal Work function Engineering" in Electron Devices, IEEE , vol.55 Issue 1, pp372 – 381.
- [6] Jin He,Feng Liu, Jian Zhang, Jinhua Hu, Shengqi Yang and Mansun Chan, " A Carrier based Approach for compact modeling of the long channel undoped symmetric Double-gate MOSFETs",IEEE transactions on Electronic Devices,vol.54,pp-1203- 1209,2007.

**AUTHORS**

**First Author** – Neha Goel, Pursuing M.Tech in ECE, Indira Gandhi Institute of Technology, GGSIP University and e-mail – neha.agarwal12@gmail.com.

**Second Author** – Dr. Vandana Nath, Electronics and Communication Dept. U.S.I.T., GGSIP University and e-mail – vandana.usit@gmail.com