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Design and Implementation of a Two-Bit Binary Comparator Using Reversible Logic

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Abstract- Modern digital circuit designing is now focussing on the reversible circuits. It aims towards the designing of low power loss circuits in the area of nanotechnology, quantum computing, optical computing, signal processing etc. This paper presents an optimized two-bit binary comparator based on reversible logic using Feynman, Toffoli, TR, URG and BJN gates. Optimization of the comparator circuit is achieved on the basis of total number of gates used in the circuit and total number of garbage outputs generated. Proposed circuits have been simulated using ModelSim and implemented using Xilinx Spartan2 FPGA platform.

Index Terms- Reversible Logic, Circuit Designing using Reversible Gates, Reversible Logic Gates, Binary Comparator.

I. INTRODUCTION

Conventionally digital circuits were made up of basic logic gates which were irreversible in nature. These irreversible gates produce energy loss due to the information bits lost during the operation. Information loss occurs because total number of output signals generated is less than total number of input signals applied. In reversible circuits conventional logic gates were used for designing which were irreversible in nature, whereas in reversible logic these design entities are replaced by basic reversible logic gates. In 1961, R. Landauer has demonstrated that an irreversible circuit dissipates some energy for every bit of lost information [1], later in 1973, Bennett has shown that this energy loss of the circuit can be minimized or even removed if the circuit is constructed using reversible logic [2].

Reversible circuit designing is gaining wide scope in the area of Quantum computing, nanotechnology, low power CMOS design, advanced computing etc due to its ability to design low-loss or approximately lossless circuits. Reversible logic gates are (n,n) logic gates where (n,n) refers to the (number of input signals, number of output signals)[3]. In reversible gates input signal can be formulated by knowing the output signals. Reversible logic approach can optimize the design entity with less number of gates. The key issue of designing the reversible circuit apart from fewer gates is the minimization of garbage output signals generated [4, 5].

In this paper we propose the reversible circuit for two-bit binary comparator which is designed using the concept of implementing circuits for any two outputs of the comparator and then inferring the third output from this circuit. In this paper optimization of comparator circuit is achieved for the total number of gates used in the circuit and total number of garbage outputs generated for the various combinations of basic reversible logic gates used for circuit design. The reversible two-bit binary comparator is optimized on the basis of number of gates used, number of garbage outputs generated and CPU usage. All the circuits are modelled and simulated with VHDL on ModelSim platform.

Structure of this paper is as follows: Section 1 gives the brief introduction about the reversible circuit designing. Section 2 provides the details of basic reversible logic gates used in the comparator circuit designing. In section 3, irreversible two-bit binary comparator circuit is explained. Section 4 includes the successive optimized approaches for reversible circuit designing. In section 5, the paper is concluded.

II. REVERSIBLE LOGIC FUNDAMENTALS

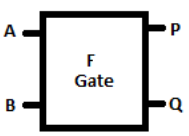
A. Reversible Logic Circuits

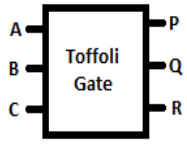
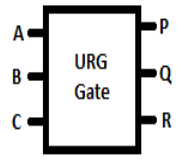
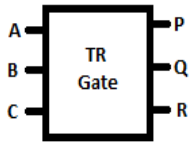
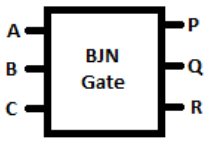
Reversible circuits are designed with the help of basic reversible gates which have the property of input signal being inferred from obtained output signal. In this logic information loss is tried to have minimum so the energy loss will be approximately zero. A circuit implemented using reversible gate should have no fan-out, no feedback, minimum garbage outputs and minimum delay. But to obtain an ideal circuit is practically very tedious [6, 7]. In the present investigation we had tried to attain an optimized reversible circuit of an irreversible comparator.

B. Reversible gates

Reversible logic gates have equal number of input and output signals. Basic reversible logic gates used to design two-bit comparator circuit are Feyman gate [8,9], Toffoli gate [4], R-Gate [10], URG gate [11], TR gate [12] and BJN gate [13]. Brief introduction of these gates are as given in the table 1.

Table 1: Basic Reversible Gates

S. No.	Gate	Block Diagram	Output
1	Feynman Gate		P = A Q = A ⊕ B

2	Toffoli Gate		P = A Q = B $R = A \cdot B \oplus C$
3	URG Gate		$P = (A + B) \oplus C$ Q = B $R = A \cdot B \oplus C$
4	TR Gate		P = A $Q = A \oplus B$ $R = A \cdot \overline{B} \oplus C$
5	BJN Gate		P = A Q = B $R = (A + B) \oplus C$

III. IRREVERSIBLE TWO-BIT BINARY COMPARATOR

A. Comparator Circuit

The comparator circuit is used to compare one or more than one bit numbers. In a comparator circuit output signals generated for either A>B, A=B, or A<B where A and B are input binary numbers to be compared. Optimized one bit comparator circuit using reversible gate was presented by Nagami AN, Jayashree HV and HR Bhagyalakshmi [13].

In this paper we have proposed an optimized circuit for a 2-bit binary comparator with a comparative analysis in terms of total number of reversible gates used, total unused outputs generated (garbage output) and CPU usage in various designs.

B. Two-bit binary Comparator Circuit

Block diagram of an irreversible two bit binary comparator circuit is shown in figure 1 [14]. Here two input binary numbers are A (A_1, A_0) and B (B_1, B_0) and output signals are $F_{A>B}$, $F_{A=B}$, $F_{A<B}$.

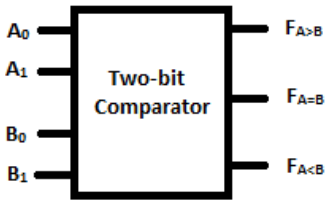


Figure 1: Block Diagram of Two-Bit Comparator

Above comparator compares two 2-bit numbers A and B and generate the comparison result in the form of three signals $F_{A>B}$, $F_{A=B}$ and $F_{A<B}$. The output functions of $F_{A>B}$, $F_{A=B}$ and $F_{A<B}$ can be expressed using K.map as follows-

$$F_{A>B} = A_1 \cdot \overline{B_1} + A_0 \cdot \overline{B_1} \cdot \overline{B_0} + A_1 \cdot A_0 \cdot \overline{B_0}$$

$$F_{A=B} = \overline{A_1} \cdot \overline{A_0} \cdot \overline{B_1} \cdot \overline{B_0} + \overline{A_1} \cdot A_0 \cdot \overline{B_1}.B_0 + A_1 \cdot \overline{A_0} \cdot B_1 \cdot \overline{B_0}$$

$$F_{A<B} = \overline{A_1} \cdot B_1 + \overline{A_0} \cdot B_1 \cdot B_0 + \overline{A_1} \cdot \overline{A_0}.B_0$$

C. Reversible Comparator Circuit Design

In order to design 2-bit binary comparator, we require two inputs. From these two given inputs we have derived two outputs using the concept of reversible logic. With the help of these two derived output we inferred the third output. The above approach can be summarised as under

1) Firstly we have designed reversible circuit for two output signals $F_{A=B}$ and $F_{A>B}$ of the comparator.

2) Then with the help of these obtained signals (in step a) third output signal has been generated through following logic

$$F_{A<B} = \overline{F_{A=B}} \cdot \overline{F_{A>B}}$$

IV. IMPLEMENTATION OF TWO-BIT COMPARATOR USING REVERSIBLE LOGIC

In literature there are so many combinations of reversible gates and approaches are available to design a combinational circuit using reversible logic [15, 16, 17]. In the designing of reversible comparator circuit we have used only Feynman, Toffoli, UGR, TR and BJN gates. In the present paper we propose three designs for comparator to achieve optimized circuit. These three designs have been simulated using ModelSim. The performances of circuits are analyzed on the basis of total gates, garbage outputs and macro statistics. Proposed design approaches have been presented in proceeding subsections.

A. Design 1

In this design Feynman gate which is a (2, 2) reversible gate and Toffoli, TR, URG and BJN gates which are (3, 3) reversible gate have been used. TR gates are used in input stage and the outputs are derived from URG and Toffoli gates. Output signal $F_{A>B}$ is derived from URG gate whereas output $F_{A=B}$ derived from Toffoli gate. These two outputs are utilised to derive $F_{A<B}$ using Toffoli gate. The block diagram of this design is shown in the figure 2. Here 14 reversible gates have been used in various configurations and number of garbage output signal generated are 17.

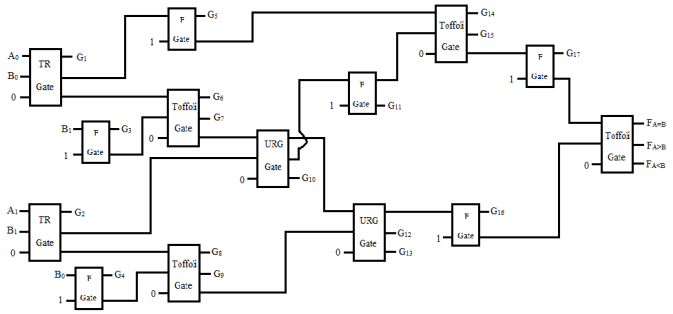


Figure 2: Design 1 of Reversible 2-Bit Comparator

B. Design 2

As shown in figure 3, in this design Feynman gate, a (2, 2) reversible gate and a combination of (3, 3) reversible gates i.e. BJN, URG, Toffoli and TR gates are used. In this proposed design the TR gates are used in input stage and the outputs are derived from Toffoli, URG and BJN gates. Output signal $F_{A>B}$ is derived from URG gate whereas outputs $F_{A=B}$ from Toffoli gate.

Utilizing these two outputs we have derived $F_{A<B}$ from BJN gate. In this design total number of reversible gates used is 12 and garbage outputs generated is 15.

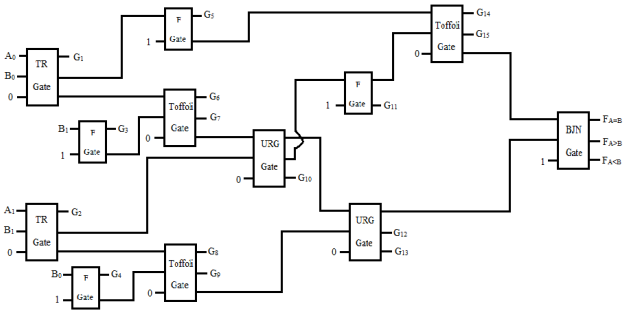


Figure 3: Design 2 of Reversible 2-Bit Comparator

It is more optimized reversible comparator circuit as compared to design 1. But it can be further optimised with respect to configuration and gates so that number of total gates used and garbage outputs can be minimized. So, moving towards the top of the optimization hierarchy we propose a better design in terms of various leading parameters.

C. Design 3

The most optimized reversible 2-bit comparator circuit is shown in figure 4. This design uses a combination of Feynman gate, a (2,2) reversible gate and TR, URG and BJN gates which are (3, 3) reversible gates. In this optimized design TR gates are used in input stage and outputs are derived from TR, Feynman gates. It has been further simplified and all three outputs have been derived from BJN gate. Here total gates used are 9 and garbage output generated is 10.

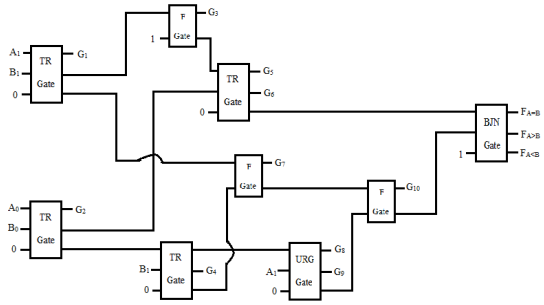


Figure 4: Design 3 of Reversible 2-Bit Comparator

D. Result and Analysis

The various proposed designs of reversible two-bit binary comparator have been analysed on the basis of performance parameters as shown in figure 5.

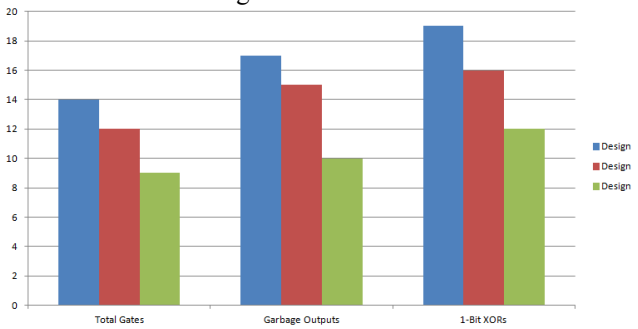


Figure 5: Comparison Chart

The above comparison chart shows the clear variations among all three designs. From above analysis we can conclude that design 3 is the most optimized configuration in terms of number of total gates used, number of garbage outputs generated, 1-bit XORs created and CPU usage as compared to other two designs. This design has been simulated using Modelsim simulator. Structural modelling has been used for the programming. Figure 6 shows the simulated waveform for each and every input and output signals.

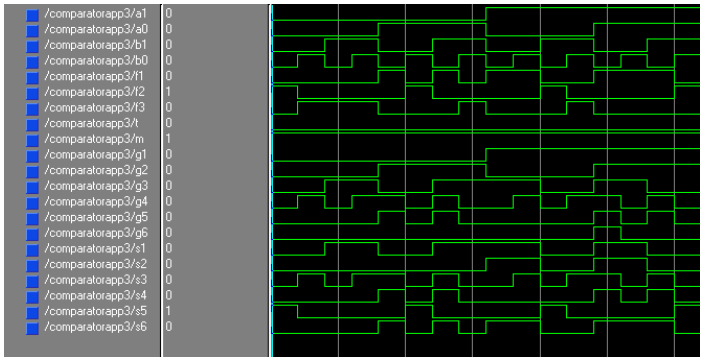


Figure 6: Simulated Waveform of Reversible Comparator

The optimized design is synthesized using Xilinx ISE 6.1i and implemented using Xilinx Spartan2 FPGA platform. Figure 7 shows the floor plan of the design.

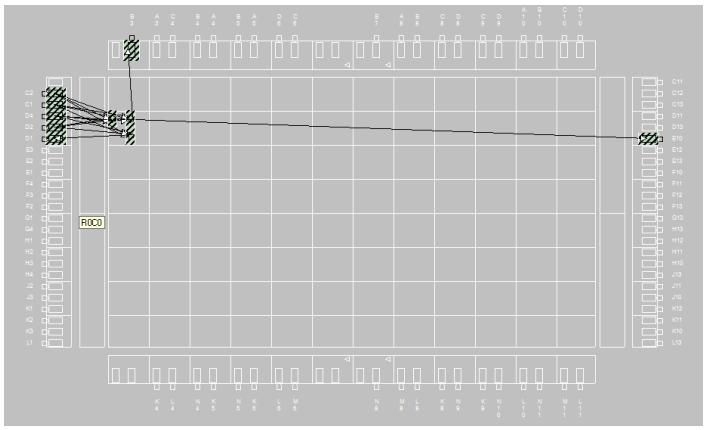


Figure 7: Floor Plan of Reversible Comparator

V. CONCLUSION

Reversible logic is becoming the modern way of digital logic circuit designing. Here in this paper we have tried to attain highly optimized two-bit reversible comparator circuit by using some of the basic reversible gates. The base of optimization is total reversible gates used and garbage outputs generated. Optimized comparator circuit (shown in figure 4) has 9 total reversible gates used and 10 unused outputs generated. This design can be employed in low power logical design applications.

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