ISSN 2250-3153

Analysis, Design and Control of Zero Current Switching DC To DC Buck Converter

Naseem Zaidi, Aziz Ahmad

Al-Falah School of Engineering & Technology, Faridabad, Haryana, India

Abstract- A soft-switching buck converter is proposed for battery charging application. This converter can also be used with other low voltage miniature applications. Resonant inductor and capacitor helps to turn on-off the switch at zero current. This reduces switching losses in our conventional converter. In order to determine two (current) zero-cross points for switch-on and switch-off, the quasi-resonant state is employed. The quasi-resonant state is performed in full-waveform mode. This makes output voltage independent of output load variation. This leads to efficiency higher than conventional converter due to ZCS. Complete design-oriented mathematical calculations were done for zero current resonant switching converters. The performance of the proposed converter is evaluated on a 3.24-W (6 V/0.54 A) experimental prototype.

Index Terms- Soft switching, Zero current switching (ZCS)

I. INTRODUCTION

Advances in power electronics in the last few decades have led not only to improvements in power devices, but also to new concepts in converter topologies and control [1].

Electromagnetic interference (EMI) generally exists in all electrical and electronic equipment, especially in all DC/DC converters. Since the switching frequency applied in DC/DC converter is high it causes significant EMI if carelessly designed [2]. The high dv/dt and di/dt involved in the switching operation of traditional hard-switched power electronics devices are the major source of EMI emission. In order to improve the energy efficiency and reliability of power converters soft-switching techniques created in 1980s have been proposed to reduce [4].

- The switching power losses across the power devices,
- The switching stress of switched-mode power electronics circuits.

Zero current switch quasi-resonant-converters implement ZCS operation. Since switches turn-on and turn-off at the moment that the current is equal to zero, the power losses during switch-on and -off become zero. Consequently, these converters have high power density and transfer efficiency usually, the repeating frequency is not very high and the converter works in the resonance state, the components of higher order harmonics is very low. Therefore, the electromagnetic interference (EMI) is low, and electro-magnetic susceptibility (EMS) and electromagnetic compatibility (EMC) are reasonable.

In this proposed soft switching converter output L-C filter is also designed to give constant output voltage with less than 0.01% ripple. Experimental results based on 3.24-W (6 V/0.54 A) prototype circuit are presented to verify the performance of the proposed converter.

II. CIRCUIT CONFIGURATION

Fig .a. shows the block diagram of proposed converter. From it it's clear that input DC voltage is changed to low voltage DC output. It is basically a DC- DC converter. Converter used here is off resonant type; particularly here zero current switching converters are used. Converter is controlled through 3524 PWM IC and totem pole driver circuit.

Fig.1. shows a circuit diagram of the proposed converter. Circuit consists of resonant capacitor (Cr) parallel with diode (D). Resonant inductor (Lr) is in series with switch (S) and supply DC voltage. Here MOSFET is used as switch. It contains parasitic diode inbuilt with it. This diode helps in full waveform mode operation of resonant converter. Filter inductor (L_f) and capacitor (C_f) is used for getting constant DC output voltage. L_f is made high to get approximately constant output current. Resistive load (R) is used to verify the result. Characteristic impedance is defined as :

$Z = \sqrt{Lr/Cr}$.

One need to ensure Vin/ Z > Io to guarantee that current will return to zero. Io is the output current and I(lr) is resonant inductor current. As soon as switch is turn on Cr and Lr forms series resonant circuit having capacitor parallel load (Io). Switch is turn on till resonant current comes to zero again. This leads to zero current turn off the switch .This reduces switching losses and results in increase in efficiency of the converter.

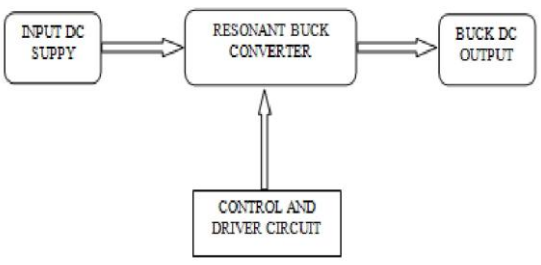


Fig.a: Block diagram of proposed converter

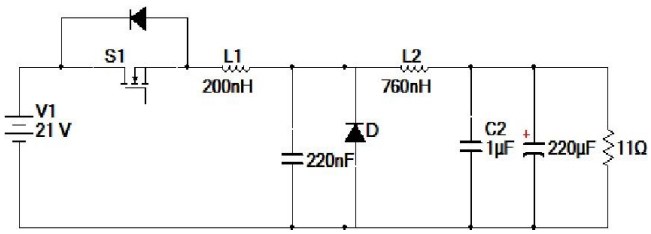


Fig.1: Circuit diagram of the proposed soft-switching converter

III. OPERATION PRINCIPLE

Various ZCS can work either in half wave mode (fig.7) or full wave mode (fig.6) as given in reference [4].It can be seen that output voltage is sensitive to the load variation in half wave mode. At light load conditions, the unused energy is stored in Cr, leading to an increase in the output voltage. Thus, the switching frequency has to be controlled in order to regulate the output voltage. If an anti-parallel diode is connected across the switch, the converter will be operating in full-wave mode. The operation is similar to the one in half-wave mode. However, the inductor current is allowed to reverse through the anti-parallel diode and the duration for the resonant stage is lengthened. This permits excess energy in the resonant circuit at light loads to be transferred back to the voltage source Vi. This significantly reduces the dependence of Vo on the output load.

Various ZCS relationship in full wave mode has been derived by assuming various ideal conditions. But as this is not practical one, so later in this article non-ideality is also taken into account for getting the exact relations. But first start with ideal conditions

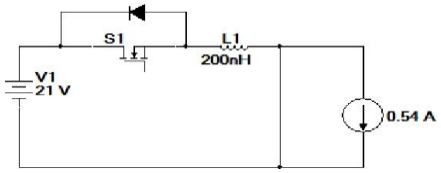
Followings is the assumptions:-

- Filter inductor is assumed to be very large so that output current Io assumed to be off constant magnitude.
- Diode D is assumed to be ideal, and so there is no voltage during ON state.
- MOSFET is also assumed to be ideal and so there is no resistive and switching loss.
- Voltage source is also assumed to be ideal voltage source means there is no inductance.
- Capacitor and inductor is also assumed to be ideal, assuming there is no resistance across it.

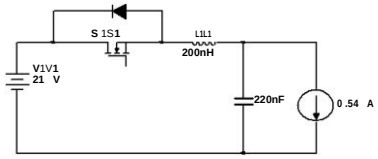
This ZCS configuration has been discussed in mainly four mode of operation namely mode a, b, c, d as shown in fig.5. Each configuration has been divided into four different time intervals as shown in fig.6.

Now various modes of operations are discussed as follows:

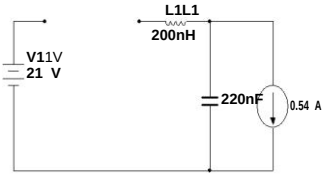
Mode a (t_0 - t_1): At time to, the switch is turned on. Because of Io flowing through the diode it appears as short circuit and the entire input voltage V_{in} appears across L_r. Therefore, the switch current builds up linearly until it becomes equal to I out at time t_1. Beyond this time, the diode turns off and the voltage clamp across Cr is removed. Switch S1 turns on at t_0, the source current increases linearly with the slope V_{in} / L_r; this is called current linear rising interval. This current is smaller than the constant loading current I_{out}. Therefore, current doesn't flow through the resonant capacitor Cr. The transistor turn on, causing current to ramp at di/dt = Vin/Lr -------- **(b)**



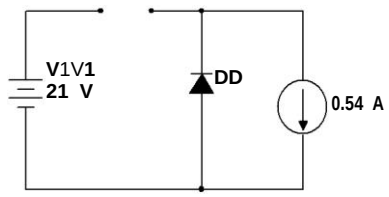
Mode a



Mode b



Mode c



Mode d

Mode b, mode c, mode d: Beyond $t_{1,}$ it > Iout and their difference (It− Iout) flows through Cr. At t, it peaks and Vc= Vd. The circuit configuration give

Vin =Lr(di/dt)+Vd - (1)

icd = Cd(dv/dt) = it - Iout- (2)

Differentiating (1) and substitute it in (2). If the time when the diode turns off is used as the reference time t=0, the initial conditions are taken as it (0) = Iout. The solution is an undamped sinusoid,

it(t)=(Vin/Zc)sin(Wrt)+Iout - (a)

Where:

Wr is the resonant frequency.

Zc = √Lr/Cr

Notice that we need to ensure Vin/Zc > Iout to guarantee that the current will return to zero. This is an important detail: the characteristic impedance must be low enough to provide large variations in the inductor current when the resonant circuit is operating. In this case

I_1 = Vin/Zc

Resonant converter action is generated as follows:

- Keep the MOSFET gate signal high until the current it (t) reverses polarity. When the current reverses, the internal diode of the MOSFET will carry it.
- Turn the gate signal off at the current is negative (this will make the internal diode control the turn –off process).
- The MOSFET will turn off at the current zero crossing from negative to positive when its internal current reaches zero.

This action is illustrated in Fig.6. The turn on-time of MOSFET is the time from t=0 until the rising zero-crossing of the current occurs. This is just slightly less than one cycle of the resonant waveform. This point is the MOSFET turn-off is the solution of the set of equations:

0 = (Vin/Zc)sin(Wrt)+ Iout------- (d)

- To find the output voltage, the voltage Vd (across the Cd) is needed. The configuration of interest is mode b and mode c, since Vd is zero otherwise. In mode b, the voltage equation can be derived from earlier relation
  (1) and (a) to give:

Vd (t) = Vin (1-cos(Wrt)) ----- (3)

This equation is valid till t_{off2} . At time t_{off2} the mode c is valid and entire load current flows out of the capacitor. The capacitor voltage drops linearly according to **- Iout = Cd(dv/dt) .**when the voltage reaches zero, the diode turns on and the converter returns to **mode d.**

- Over a switching period T, average diode voltage will be required output voltage:

$<Vd> = 1/T[\int_0^{toff2} Vin(1-cos(Wrt))dt + \int_{toff2}^{T(diodeon)} Vd(t)dt]$

Using above relation required output voltage can be found out just by changing the total time period T. We can get varied range of voltage using the above relation but meanwhile we have to insure that there is enough time for the operation of various modes without any fail, otherwise our objective of ZCS won't fulfill. To ensure ZCS operation of the output diodes, the half resonant period of inductor current should be finished before the power switches are turned off. So for proper operation gate pulse is given till little longer time than calculated to ensure zero switching operation. This is taken as safety precaution from designer point of view.

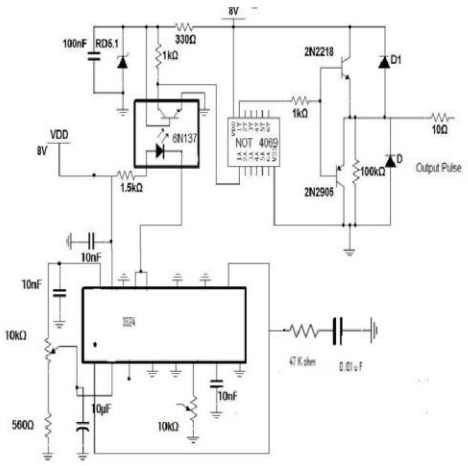


Fig.2: Driver and control circuit

Fig.2 shows a driver and control circuit diagram of the proposed converter. Control circuit consists of 3524 IC which is used for PWM. As from the datasheet of 6N137 Optocoupler pin 2 is connected to +12 V supply through a 1.5 kilo ohm resistor to limit the high current. Whenever 3524 output transistor turn on pulse at output goes to zero as diode in the optocoupler starts conducting and output gets shorted to ground. Output of optocoupler which is at pin 6 is connected to the 4069 IC. It inverts the input waveform .In addition to that it also rejects the noise present at the output of optocoupler. It results into perfect noise free PWM output at output pin. Output of 4069 is connected to the base of totem pole configuration through 1 kilo ohm resistor.

Totem pole configuration is used basically to drive the MOSFET in a healthy manner. MOSFET contains parasitic capacitances between Gate-Source (Cgs) and Gate –drain (Cgd). So as soon as gate pulse is given it (mosfet) draws initial current to charge its parasitic capacitors from the driver circuit. So for proper operation of MOSFET, driver should be in position to provide appropriate charging current. For charging purpose only 2N2218 is used. Gate pulse voltage applied between gate and source should be greater than threshold voltage (Vth) to turn on the device.

The gate drive must charge both Cgd and Cgs. The Cgd portion produces interesting effects in some converter arrangements: Since switch action causes the drain voltage to swing quickly between low and high voltage values, it is possible that a substantial current Igd = Cgd (dv/dt) will flow. The gate drive must provide enough charge to account for this current as well as the current needed to charge Cgs [4].

To make the mosfet change state, the gate drive must charge the capacitor to sufficiently high voltage for turn-on, and then remove the charge for turn-off. The charge – discharge process is a time limiting step. It can also be reliability limiter. IRF 450 has got turn on time of about 90 s. so low –impedance gate drives are necessary, but create problems of their own. As the impedance drops lower and lower, the gate driver becomes a switching power converter in its own right the gate drive switches then require gate drives, which in turn require gate drives, and we are left with an unsolvable problem, real gate drives are limited to impedance on the order of five to ten ohms.

Gate drive resistance is calculated with the following relation:

$Rg = t_r / (2.2*Ciss)$

Where, Ciss = Cgs + Cgd

IV. DESIGN EXAMPLE

To verify the operation and performance of the proposed converter, a 3.24-W (6 V/0.54 A) experimental prototype circuit was built for battery charging application. A design procedure for the 3.24-W converter is presented. The specification are as follows:

$$\mathbf{V_{in} = 21V}$$

$$\mathbf{V_{out} = 6V}$$

$$\mathbf{I_{out} = 0.54\ A}$$

The selection of the resonant inductor and capacitor
Is determined by the need to satisfy the relation

Vin/Zc > Iout.

Where, Zc = √Lr/Cr

So keeping these things in mind value chosen are:

C_r = Cd = 0.22 micro farad

L_r = L1 = 120 micro Henry

According to the relation given in b, as the transistor turn on, causing current to ramp at

di/dt=21/120=0.175*10^{-6} A/s

so diode current will be zero in
0.6*10^{-6} /0.1782=3μs
so the diode current will drop to zero in 3 micro-second after transistor turn on, then the circuit enters into mode 2.

Zc = √Lr/Cr =√120/0.22= 23.386 (it is also called characteristic impedance)

According to relation given in (c)

I_1 = Vin/Zc= 21/23.3 = 0.899

This show:

Vin/Zc > Iout**.** So resonant condition gets fulfilled.

However if load increases above 0.899, this LC combination will no longer support soft switching.

Wr =1/√LC=0.01946*10^6

fr = Wr/2Π =30.97 kHz

From the relation (d)

$$W_r t_{off} = 36.86$$

It (t) will be zero at 216.86(in degree) and 323.14(in degree). Corresponding time can be calculated as

t_{off1} =216.86*Π/180*0.1988= 19.03 μs

t_{off2} =323.14*Π/180*0.1988= 28.36 μs

So MOSFET gate signal should be held high until (3+19.03 = 22.03 μs). And it should be turn – off before t_{off2} is reached. The gate signal of 22.5 μs will work nice in this case.

- The second integral is the area of a triangle. The triangle peak value is given (3):

Vd (t_{off2}) = 21 (1- cos(323.14)) = 4.19 V

The time until Vd reaches zero is:

t=Vd(toff2)/(Iout/Cd)=(4.19*0.22)/0.54=1.70μs

From (ii)

ΔArea=(0.22*4.19)/(2*0.54)=3.57*10^{-6}Vs

From (i)

$$[{}_0\int^{toff2} Vin(1-\cos(Wrt))dt]$$

$$=21[28.36+3.49]$$

$$668*10^{-6}\ Vs$$

So th average output voltage is

<Vd>=(668+4.19)/T **-----(F)**

Since the desired output is 6v then:

6=(668+4.19)/T

T=112 μs

So from above we get f ≅ 9 kHz in **ideal** condition. But in **practical** case we have to take care the drop across the diode also over the period of time which is around 1.5 V during turn on time of diode.

6T = (668+4.19)) -1.5 (T- 33.53) [33.53 is the off time of diode]

Which gives T ≅ 96 μs

And frequency = 10.37 kHz

By taking other non ideality in MOSFET, inductor, capacitor practical switching frequency is coming around 13.4 kHz.

V. EXPERIMENTAL RESULTS

3.24-W (6 V/0.54 A) prototype of the ZCS converter, as shown in Fig. 1, is built to verify the theory. And the result is compared with simulation.

The specifications of the experimental prototype is as follows:

Input voltage = 21V, Output voltage = 6V, output current = 0.54 A.

Circuit parameters of the proposed converter are as follows.

1) Switch: MOSFET IRFP450.
2) Diode: PFR856.
3) Resonant capacitor: 0.22 uF/400 kV.
4) Filter capacitor: 220 uF/400 V.
5) Resonant inductor: 0.2mH (Pot core 26/11).
6) Output filter inductor: 0.67 uH (pot core).

Fig.13 shows the simulated waveforms for the above designed circuit.

Fig 8.Shows that as soon as we turn on the MOSFET current through the resonant inductor start increasing and it reaches maximum current (I max) during resonance and again come back to zero .And that instant gate pulse has to be turned off. Then also current flow in small amount in negative direction due to the inherent diode connected inside the MOSFET. So MOSFET turns off at diode voltage drop.

Fig 8. Shows that maximum capacitor voltage reaches to around 38 V. But from the resonant theory it's clear that voltage should be twice the input voltage in ideal case. But in practical case due to drop in MOSFET and Inductor, voltage is less than ideal case. Voltage will start rising only when current has reached output current of 0.54, as you can appreciate these things in a better way from fig.12.

Fig 10.Shows that Output voltage is constant DC output voltage of magnitude 6 V for a particular frequency of 13.5 kHz. As from above relation (F) we can increase the output voltage by increasing the switching frequency but we have to also insure proper zero crossing of inductor current. Output voltage contains ripple of about 0.001%.

Fig 11.Shows that during turn on and during turn off there is no voltages shoot up as you can see these things in conventional buck converter. This results into less voltage stress of switches during switching times. During off state voltage waveform has got some short of oscillations due to parasitic capacitance and inductance of driver circuit.

Efficiency

From current waveform, average input current can be found out to be

I avg = 0.192 A

Pout = (6* 054) = 3.24 watt

Pin = V * I avg

= 21* 0.192

= 4.03 watt

Efficiency=Pout/Pin=3.24/4.03=**80.35%**

Without resonance
I avg = 0.198 A

Efficiency=Pout/Pin=3.24/4.15=**77.9%**

And efficiency of this converter is coming around 81% mainly because of the on state drop of diode at freewheeling time. This drop is coming around 1.2 V with PFR 856. This reduces my efficiency. To overcome this problem, we can replace diode with MOSFET having on state drop of around 0.3 V. This will improve the efficiency of above converter above 90%.

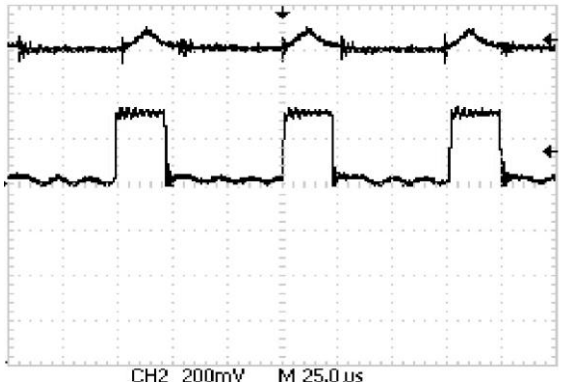


Fig 8: Current waveform with gate pulse

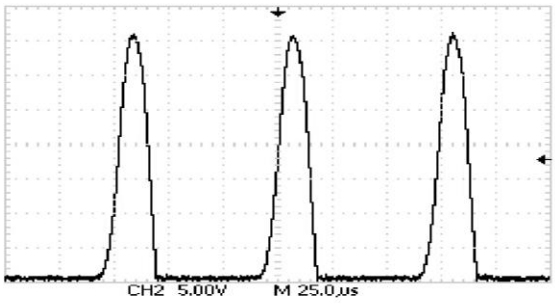


Fig 9 : Voltage waveform

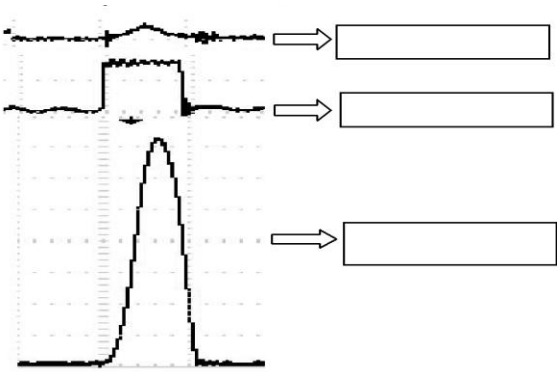


Fig 12: Waveform for combined inductor current and resonant capacitor voltage with gating pulse

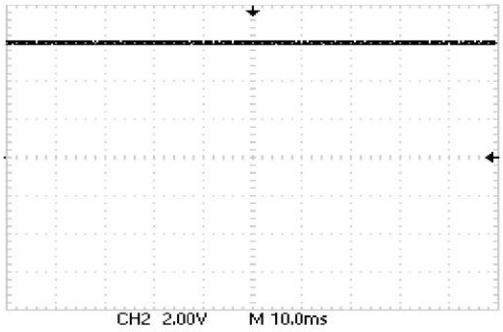


Fig 10: Output Voltage

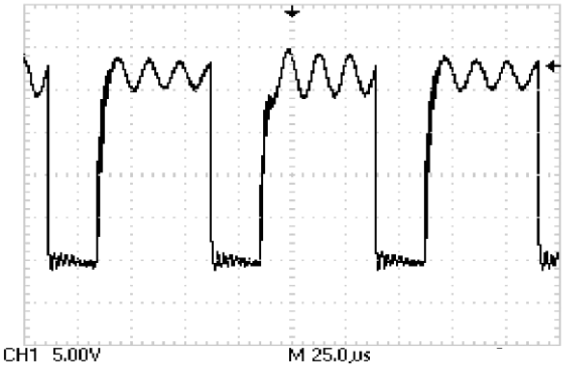


Fig 11: Voltage waveform across Switch

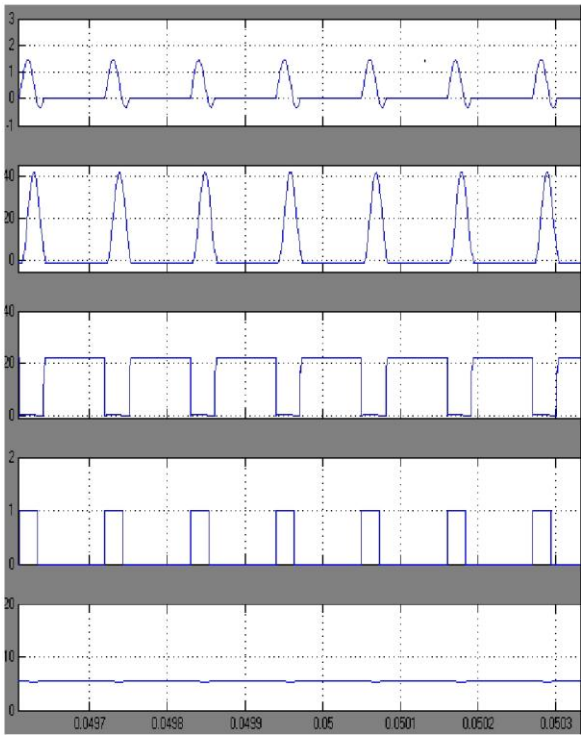


Fig 13: Simulation waveform
(From top to bottom- resonant inductor current, resonant capacitor voltage, MOSFET voltage, Gate pulse, Output voltage)

VI. CONCLUSION

In this project zero current soft switching DC- DC has been designed and implemented using hardware. Switching losses has been reduced to a greater extent. Furthermore, power conversion efficiency can be improved by the soft-switching operation of switching devices. This operation requires a larger output filter. The resonant inductor current works here in DCM. The reverse-recovery loss of the output switch is reduced. Experimental results based on a 3.24-W (6 V/0.54 A) prototype have evaluated the performance of the proposed converter. The efficiency of the proposed converter is potentially better than the conventional buck converter.

REFERENCES

[1] Fang Lin Luo and Hong Ye, "Advanced dc-dc converter," pp. 11.1- 11.6, 2004.

[2] Philip T Krein, "element of power electronics," First Indian Edition, pp.300-307, 2008.

[3] Ned Mohan and Tore M. Undeland, "power electronics," Third edition, pp. 249-289, 2007.

[4] K.M. Muttaqi ,"electromagnetic interference generated from fast switching power electronics devices" International journal of innovation in Energy system and power, vol3, no1 , April 2008.

AUTHORS

First Author – Naseem Zaidi, Al-Falah School of Engineering & Technology, Faridabad, Haryana, India, Email: nimmizaidi@gmail.com

Second Author – Aziz Ahmad, Al-Falah School of Engineering & Technology, Faridabad, Haryana, India, Email: azizjmi98@gmail.com