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Design and FPGA Implementation of DAA Based FIR Filter

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Abstract- DSP functions such as FIR filters and transforms are used in a number of applications such as communication and multimedia. FIR Filter is an LTI system its output is a convolution function of input and impulse response of the system. It involves multiplication and addition operations. Application of DAA (Distributive Arithmetic Algorithm) in this implementation avoids the usage of multiplication to minimize the hardware complexity. In this paper a novel architecture for a 16 tap FIR filter is designed and implemented by using optimized DA algorithm. Xilinx Xc5vfx200T FPGA is targeted using Xilinx ISE 10.1i software. Performance of the implemented FIR filter in this paper is measured in terms of relative error in result by comparing the FPGA output with theoretical value calculated in MATLAB.

Index Terms- FIR, LTI, DA, FPGA, MATLAB, LUT, ASIC

I. INTRODUCTION

FIR filter is an LTI system, eq(1) represents the response of a 16 tap FIR filter, where x(n) represents the input sequence and h(n) represents the impulse response of the FIR filter.

$$y(n)=\sum_{k=0}^{n} h(k)*x(n-k) \quad \ldots\ldots (1)$$

It is evident from eq(1) that, convolution involves multiplication and addition. But using multiplier is not economical in view of hardware complexity. Using Look Up Tables is one Solution to avoid the multipliers, which is described in DA algorithm.

$$\begin{aligned} y(n)=\sum_{k=0}^{n} h(k)\bullet x_{k,0} + h(0)\bullet x_n + h(1)\bullet x_{n-1} \\ + \quad \ldots + h(n)\bullet x_{n-k} \qquad \ldots(2) \\ =\sum_{k=0}^{n} h(k)\bullet x_{k,0} + \{h(0)\bullet x_{n,1} + h(1)\bullet x_{n-1,1} \\ + \quad \ldots \quad + h(n)\bullet x_{n-k,1}\}\bullet 2^{-1} + \\ \{h(0)\bullet x_{n,2} + h(1)\bullet x_{n-1,2} + \ldots \\ + h(n)\bullet x_{n-k,2}\}\bullet 2^{-2} + \\ . \\ . \\ . \\ \{h(0)\bullet x_{n,7} + h(1)\bullet x_{n-1,7} + \ldots \\ + h(n)\bullet x_{n-k,7}\}\bullet 2^{-7} \\ \ldots(3) \end{aligned}$$

Input sample magnitudes in this implementation are taken as fractional. So, by using DA algorithm [2] the way eq (1) rearranged is described in eq(2) and eq(3):

So, In eq(3) each sum term can be stored in LUT, fetched appropriately and added to achieve y(n).

II. OPTIMIZED DA ALGORITHM

In the convolution equation (3), maximum coefficient sum term may have 16 coefficients. So 2^M sum combinations are possible in M tap FIR filter implementation, it implies that ROM depth required is 2^M locations. It is a huge requirement. To minimize this, DA algorithm can be optimized [1] as in eq(4).

$$\begin{aligned} \sum_{k=1}^{M} A_k x_{kn} &= \sum_{k=1}^{M/2} A_k x_{kn} + \sum_{k=M/2}^{M} A_k x_{kn} \\ &= \sum_{k=1}^{M/4} A_k x_{kn} + \sum_{k=M/4+1}^{M/2} A_k x_{kn} \\ &\quad + \sum_{k=1+M/2}^{3M/4} A_k x_{kn} + \sum_{k=3M/4+1}^{M} A_k x_{kn} \\ &\qquad \ldots(4) \end{aligned}$$

In equation (4), each floating point sample can be expressed as

$$x_m = -x_{m0} + \sum_{k=1}^{N-1} x_{mk} \bullet 2^{-n} \qquad ....(5)$$

In this implementation, value of N (number of bits) is 8. First bit represents sign and other bits represent the magnitude.
A typical term in eq(4) can be expanded as follows

$$\sum_{k=1}^{M/2} A_k x_{kn} = \sum_{m=1}^{M/2} A_m (-x_{m0} + \sum_{k=1}^{N-1} x_{mn} \bullet 2^{-n})$$

$$= \sum_{m=1}^{M/2} \sum_{k=1}^{N-1} x_{mn} \bullet 2^{-n}) + \sum_{k=1}^{M/2} A_m (-x_{m0})$$

$$.....(6)$$

To implement the equation (4), required ROM dept is $2^{2+M/4}$. Before optimization, required memory size is 2^M. So that it can save $2^{-2+3M/4}$ memory locations. This is 62.5% of ROM size in case of 16 tap FIR filter.

III.FPGA IMPLEMENTATION

Each input sample is represented in sign magnitude form with 8 bits. Controller module generates the address for lookup tables to fetch the appropriate coefficient sum terms in equation (4). Multiplication of sum terms with 2^{-k} is implemented using shift registers. Sum of the terms is achieved with accumulator.

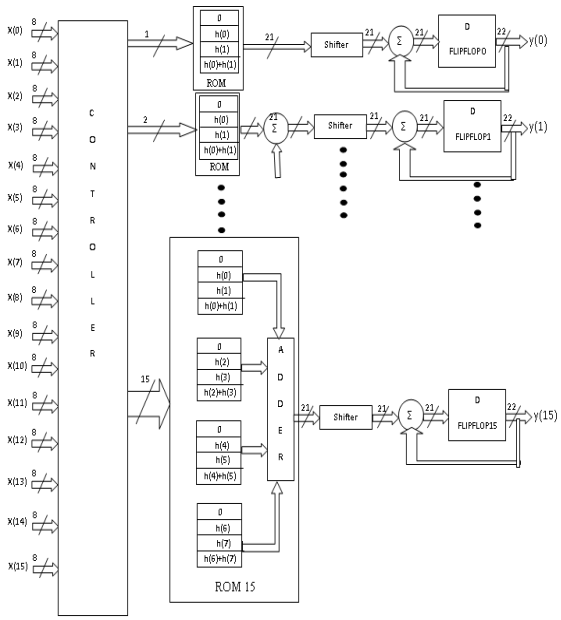

Fig. 3.1 FIR Filter Architecture

Processor takes eight clock cycles to result the output. In this implementation output is represented with 22 bits.

IV. RESULTS

A. *Simulation Results*

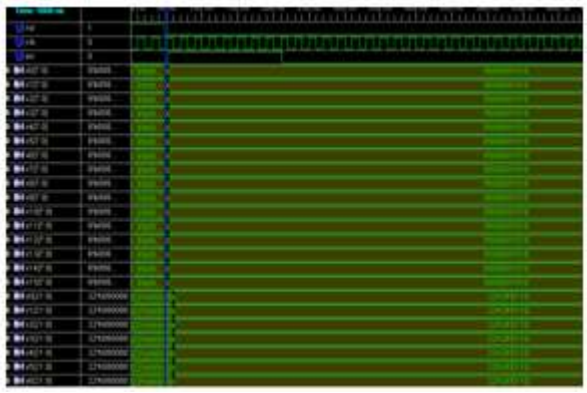

Fig 4.1 Input Output Waveforms from top module

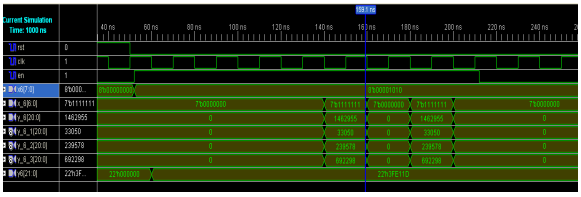

Fig 4.2 Typical waveforms of LUT6

B. *Synthesis Results*

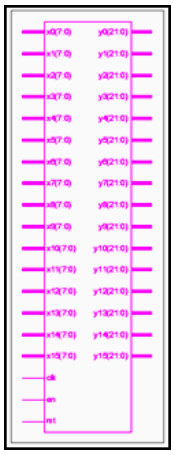

Fig 4.3 Top module's Port layout

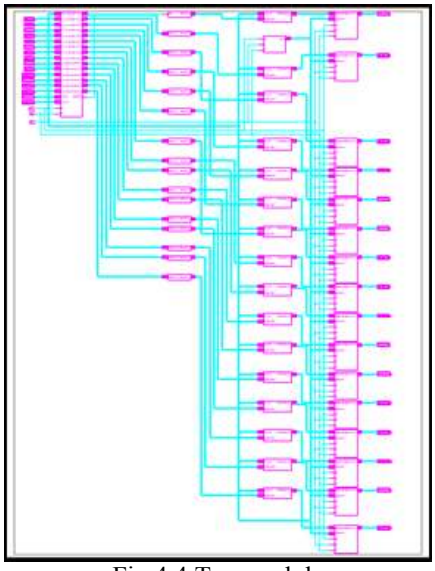

Fig 4.4 Top module

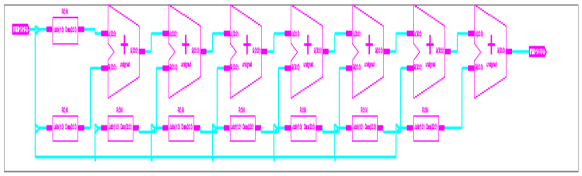

Fig 4.5 A typical LUT cum internal adder

C. *Device utilization summary*

Table 1. FPGA Resource Utilization

S. No.	FPGA Resource	Utilization
1	Slice registers	376
2	Slice LUTs	2364
3	LUT Flip Flop pairs	2381
4	IOs	483
5	Bonded IOBs	483

D. Relative Error

For a 16th-order FIR filter, the sampling frequency is 2.25 MHz; the pass band cutoff frequency is 100 kHz; The h (k) is as follows:

h(0)=h(15)=298D h(1)=h(14)=578D
h(2)=h(13)=1364D h(3)=h(12)=2718D
h(4)=h(11)=4503D h(5)=h(10)=6400D
h(6)=h(9)=7996D h(7)=h(8)=8908D

For a simple set of input points, i.e. x(0) = x(1) = x(2) = x(3) = x(4) = x(5) = x(6) = x(7) = x(8) = x(9) = x(10) = x(11) = x(12) = x(13) = x(14) = x(15) = $(0.00001010)_2$

7^{th} output point values calculated using Mat lab is (R1) =114290.
Respective FPGA simulation result (R2) = 114256
Percentage of relative error in FPGA calculation
= (R1-R2)/R1 *100% = 0.0297%

It is as typical relative error in the 7^{th} output (y(6)) of the FIR filter circuit proposed in this paper. Relative error in all other output points also lies in the same order.

V. CONCLUSION

Architecture is implemented in Verilog and Xilinx Xc5vfx200T FPGA of Vertex5 family is targeted. FPGA simulation result obtained is very close to the theoretical result from MATLAB. Therefore it can be concluded that with improved DA algorithm, it is feasible to have a processor with performance almost closer to the theoretical expectation. And also this can be used as a reusable IP (Intellectual Property) in signal processing related ASICs.

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