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A Novel Method for Analysis of Power Consumption in VLSI Global Interconnects

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Abstract- The analysis of effects induced by interconnects become increasingly important as the scale of process technologies steadily shrinks. While most analyses focus on the timing aspects of interconnects, power consumption is also important. We study the trends of interconnect power consumption based on current and figure technology node parameters. We know that 20%–30% of power is consumed by interconnect resistance in optimally buffered global interconnect system. We also study the analysis method based on a reduced-order model and discrete domain Z transform. The theoretical results can be used for any kind of linear circuits including RLC circuits.

Index Terms- Interconnect, Power consumption, Optimal, Buffered, Z transform

I. INTRODUCTION

As the scale of process technologies steadily shrinks and the size of designs increases , interconnects have increasing impact on the area, delay, and power consumption of circuits. Reduction in scale causes a continual increase in interconnect delays, although of course overall circuit performance continues to increase. As regards power, the situation is similar in that the portion of power associated with interconnects is increasing. This is an important fact because the conventional design, analysis, and synthesis of VLSI circuits are based on the assumption that gates are the main sources of on-chip power consumption. To analyze interconnects, extensive studies have been made of the use of model order reduction over the last few years, following the method for the power distribution analysis of an interconnect, based on a reduced-order model. It has been known that show power consumption can be computed efficiently in the *s*-domain using an algebraic formulation, instead of improper integration in the time-domain.[1] The theoretical results relies on the poles and residues of a transfer function, and can thus be used in any kind of model order reduction technique introduction of Asymptotic Waveform Evaluation [2]. Model order reduction is based on approximating the Z-domain transfer function of a linear (or linearized) network by a relatively small number of dominant poles and zeros. Such reduced-order models can be used to predict the time-domain or frequency-domain response of the linear network. Although there has been significant progress in the analysis and simulation of performance-related aspects of VLSI interconnects, less work has been devoted to the analysis of power consumption (or distribution) of interconnects. Furthermore, the analysis of power-related aspects of interconnects is limited to power distribution networks, and deals with quantities such as IR drop, ground bounce, and electro migration. In this paper, we introduce a method based on model order reduction technique & discrete domain Z-transform. We show that the power which involves improper integration can be derived from discrete domain Z-transform.
The remainder of the paper is organized as follows- In section II, power consumption of CMOS circuit, in section III, trends of interconnect power distribution, in section IV, analysis of interconnect power distribution, in section V, experimental result and in section VI conclusion of the paper is mentioned.

II. POWER CONSUMPTION OF CMOS CIRCUITS

It is a well known fact that there are three components of power consumption in CMOS circuits [3], which is given by

$$P_{tot} = P_{dp} + P_{stat} + P_{dyn} \quad \ldots\ldots\ldots(1)$$

where the first component is due to a direct current path from V_{DD} to ground when the pull-up and pull-down networks are both on for a short period of rising and falling transition. The second term is due to a leakage current that flows between the supply rails in the absence of switching activity. P_{dyn} represents a *capacitive dissipation* and the dominant factor in typical CMOS circuits. For example of cascaded inverters as shown in Fig. 1(a), the load seen by a driver is usually modeled as a lumped capacitance as shown in Fig. 1(b), where *Cg* denotes a gate capacitance of a receiver. During the rising transition, the total energy of $C_L V_{DD}^2$ is delivered by the source, the half is stored on C_L and the other half is dissipated by PMOS. The energy stored on the capacitor, $1/2 C_L V_{DD}^2$ dissipated by NMOS during the falling transition. Thus, the energy of $C_L V_{DD}{}^2$ is entirely dissipated by MOSFETs. The basic assumption of this model is that the interconnect resistance, denoted as R_I in Fig. 1(a), is *negligible* compared to *drain effective resistance* of MOSFETs. This is generally true in local interconnects where small MOSFETs, thus having large drain effective resistance, are connected through short wires, which have small wire resistance. However, the situation is different in global interconnect system, where large MOSFETs drive long (frequently in mm order) global interconnects, which implies small drain effective resistance and large wire resistance. This is very common in System-on-a-Chip (SoC) style integration, where many bus interconnects are implemented through long global wires Another example is a global clock [4], where global clock is constructed through huge clock buffers to simplify clock networks. The implication of this situation is that the traditional model for power analysis such as the one in Fig. 1(b) is not valid for an interconnect system where wire resistance is significant. Thus, we need an RC (or even RLC) network such as the one infig.1(c).

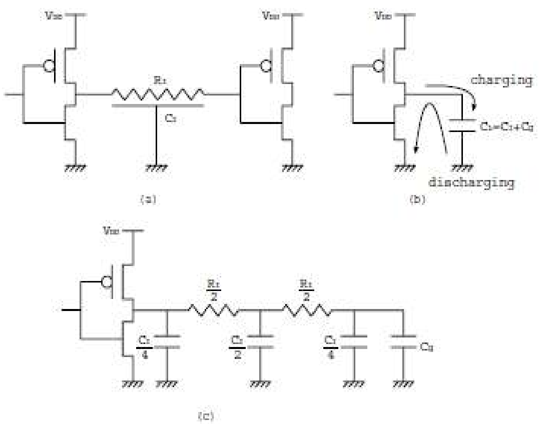

Fig. 1. (a) Two cascaded inverters, (b) lumped capacitance model for power estimation, and (c) RC tree model for interconnect.

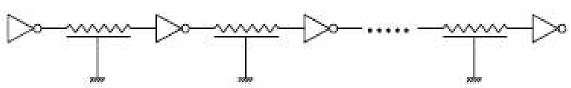

Fig. 2. Buffered global interconnects.

III. TRENDS OF INTERCONNECT POWER DISTRIBUTION

In order to investigate power consumption of interconnects, we consider a buffered global interconnect system as shown in Figure 2. Especially, we consider *optimally buffered interconnect*, where buffer size and interconnect length are determined in such a way that delay is minimized. The optimal buffer size end the optimal interconnect length can be derived from the delay equation of buffered interconnect [5], where the delay is from the input of the first buffer to the output of the last buffer:

$$t = k\left[p_1 \frac{r_i L}{k}\frac{c_i L}{k} + \frac{r_t}{h} h c_t + \frac{r_t}{h}\frac{c_i L}{k} + p_2 \frac{r_i L}{k} h c_t\right] \quad \ldots\ldots\ldots (2)$$

where k is the number of interconnect sections consisting of k+1 buffers, L is the total length of the interconnect, c_i and r_i are capacitance and resistance of the wire of unit length respectively, and c_t and r_t are gate capacitance and drain effective resistance of minimum size MOSFET respectively. The constants p_1 and p_2 depend on the switching model of the buffer, and are about 0.377 and 0.693 respectively, when 50% of the swing at the receiver side is of interest.

TABLE I
TECHNOLOGY PARAMETERS

Technology (nm)	V_{DD} (V)	T_{ox} (A)	r_t (kΩ)	c_t (fF)
180	1.8	40	3.3	1.18
130	1.5	33	3.5	0.79
100	1.2	25	3.6	0.59
70	1.0	16	4.3	0.44

TABLE III
PARAMETERS OF OPTIMALLY BUFFERED INTERCONNECT SYSTEMS

Technology (nm)	h_o	l_o (mm)	R_i (Ω)	C_i (fF)
180	169	1.76	38.7	271
130	182	1.23	38.1	194
100	203	0.94	34.8	161
70	259	0.80	32.8	154

By differentiating (2) in terms of h, setting the derivative equal to zero, and solving the equation for h, we obtain the optimal buffer size:

$$h_o = \frac{1}{\sqrt{p_2}}\sqrt{\frac{c_i r_t}{r_i c_t}} \quad \ldots\ldots\ldots\ldots (3)$$

Differentiating (2) again in terms of k, setting the derivative equal to zero, and solving the equation for k gives us the optimal number of stages for the interconnect of length L, denoted by ko. Dividing L by ko can be shown to give us the optimal interconnect length of each section.

$$l_o = \frac{1}{\sqrt{p_1}}\sqrt{\frac{r_t c_t}{r_i c_i}} \quad \ldots\ldots\ldots\ldots (4)$$

In order to project the optimal buffer size and the optimal interconnect length for the current and future technology generations, we use technology parameters extrapolated from BPTM [7], which are summarized in TABLE I. For each technology node, we obtain the optimum size of buffer and the optimum length of interconnect via (3) and (4), which are tabulated in TABLE II. The total resistance (*Ri*) and capacitance (*Ci*) of the interconnect are also shown in the last two columns of the table

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For each technology node, we configure one section of the circuit (two buffers and interconnects between them) shown in Fig. 2 with parameters in TABLE II. The interconnect is approximated by 5 sections of π-ladder circuits [6]. We obtain the power consumption of the buffer, denoted as P_b, and that of the interconnect (sum of power consumption of 5 resistors in π ladders), denoted as Pi, through SPICE simulation. The ratio of power consumed by the buffer to the total power consumption is defined by

$$\eta_b = \frac{P_b}{P_b + P_i} \quad \text{………………(5)}$$

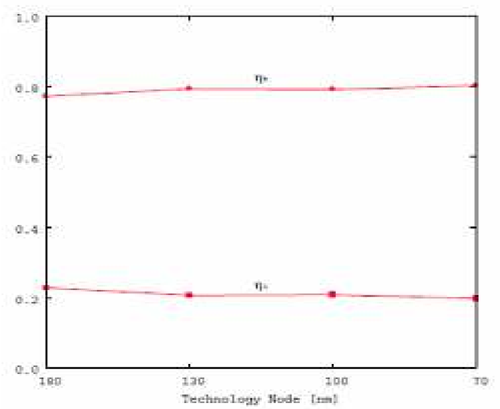

Fig.3 (a)

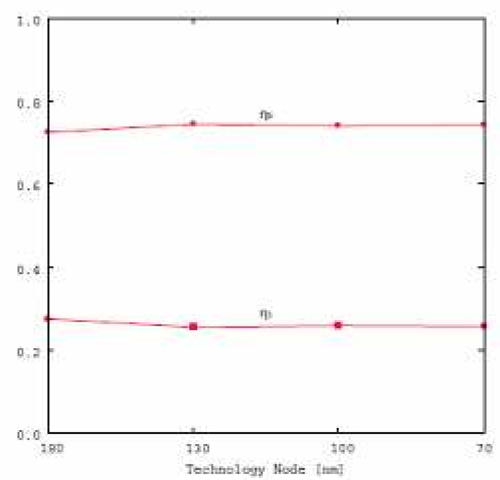

Fig.3 (b)

Fig. 3 Trends of power distribution of optimally buffered inter connect system when (a) Step (b) Clock is applied at the input of the buffer.

and similarly for η*i*. When the step is applied at the input of the buffer, the ratios of power are shown graphically in Fig. 3(a). Since we use the step at falling edge, most of power consumed by the buffer is due to PMOS operated in a linear region, thus we neglect the power consumed by NMOS, which consists of mostly leakage power. The trends show that about 80% of the total power is consumed at the transistor and the remaining power is changed to heat in the interconnect.

The trends do not change significantly when we use clock instead of step and taking all power components of the buffer into account as shown in Fig. 3(b). Since clock trees consume significant power and large buffer and long interconnect (even larger and longer than those for optimally buffered interconnect as presented in this paper) are frequently used to build clock trees [4], the power consumption of interconnects should be considered as an important factor in the design of clock distribution networks.

IV. ANALYSIS OF INTERCONNECT POWER DISTRIBUTION

In order to find the power consumption (or energy dissipation)' of a particular resistor element in a linear (linearized) circuit, we first obtain the reduced order model of current flowing through the resistor, denoted by J(s) (with the corresponding time-domain function j (t) *using* a model order reduction techniques. The approximate energy dissipated by R_i, denoted by E_i, during time period [t1 t2] is then given by

$$\hat{E}_i = R_i \int_{t_1}^{t_2} j^2(t)dt$$

If we are interested in the total energy dissipated by a specific resistor element during signal transition, we can choose to consider semi-infinite interval of t, without loss of generality. We make t1 the time origin and t2 infinite time. Then J(t) will reach a steady state, provided that j (t) corresponds to the reduced-order model of an individual transition. This leads us to the improper integral.

$$\hat{E}_i = R_i \int_{0}^{\infty} j^2(t)dt$$

It is very difficult to calculate the integration, so we use different approach. For this we use discrete domain Z-transform. the reduced order model of current following through resistor j(s) is converted into H(Z) using bilinear transformation where we put

$$S = \frac{2}{T} \; \frac{1 - Z^{-1}}{1 + Z^{-1}}$$

Where T is sampling time =1/ fs, fs=sampling frequency

Now after getting H (Z) we put $Z = re^{jw}$ where r=1, w = digital frequency =ΩT_s, Ω=analog frequency, T_s=Sampling time. For particular frequency we find the magnitude $H(e^{jw})$, which is the energy. As this is the r-c circuit it works as band pass filter. So at particular resonance frequency we find the value of $H(e^{jw})$, which is the same result of

$$\widehat{E}_i = R_i \int_0^{\infty} \widehat{h}^2(t)dt$$

But we find a range of frequency where the value is near about same of the original value in time domain. Now if we take time average then we can calculate power at particular register element.

Example:

$$H(S) = \frac{3S+5}{(S+1)(S+2)}$$

We are taking f=4 KHz; f_s=8 KHz

$$T_s = \frac{1}{8 \times 10^3} sec$$

Now

$$S = \frac{2}{T_s}\left[\frac{1-Z^{-1}}{1+Z^{-1}}\right]$$

$$= \frac{2}{\frac{1}{8 \times 10^3}}\left[\frac{1-Z^{-1}}{1+Z^{-1}}\right]$$

$$H(Z) = \frac{3.16 \times 10^3 \left[\frac{1-Z^{-1}}{1+Z^{-1}}\right] + 5}{\left[16 \times 10^3 \left[\frac{1-Z^{-1}}{1+Z^{-1}}\right] + 1\right]\left[16 \times 10^3 \left[\frac{1-Z^{-1}}{1+Z^{-1}}\right] + 2\right]}$$

Putting $Z = re^{jw}$ where

$r = 1$

$w = \Omega T_s$

$$= 2.\pi.f \frac{1}{2.\pi.f_s}$$

$$= 0.5$$

So that

$Z = 1.e^{j.0.5} = \cos(0.5) + j\sin(0.5)$

$|Z| = 0.99996$

By putting the Z value at

$|H(Z)|$

. We find

$|H(e^{jw})| = 3.54$

Now if we calculate in the time domain, then

$$H(S) = \frac{3S+5}{(S+1)(S+2)}$$

by taking inverse- Laplace transform we find

$h(t) = 2e^{-t} + e^{-2t}$

so that energy is

$$\int_0^{\infty} h^2(t)dt = 3.57$$

we showed that both result are near about same.

In order to verify the validity of the proposed analysis method, we implement a prototype tool written in C++, and based on the results presented in this section with moment matching-based model order reduction [2]. The program reads in a circuit in a SPICE-like format and outputs the power distribution of the interconnect. For the experiments, we randomly generate RC tree networks while varying the number of nodes from 100 to 500, and compare the energy distribution obtained by SPICE with that obtained by our method. As an example, Fig. 4 shows the result for a circuit with 300 nodes.

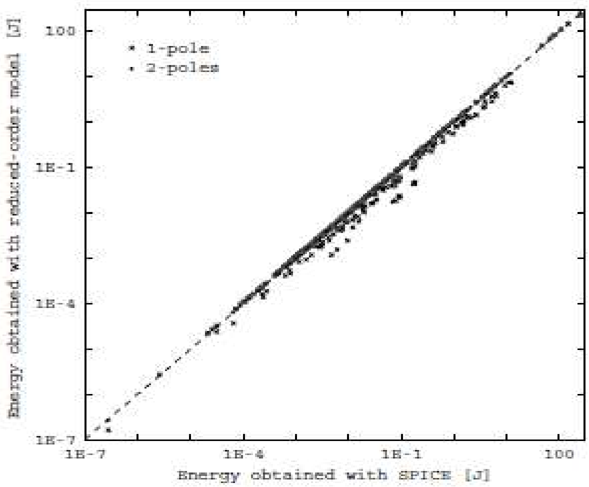

Fig-4 comparison of energy distribution for randomly generated circuit with 300 nodes.

V. CONCLUSION

We study the power consumption based on current and future technology parameters. the study shows 20-30% power is changed to heat in interconnects.

We describe a method for power distribution analysis of interconnects based on reduced order model. We show that power consumption can be computed efficiently in Z-domain using an algebraic formulation, instead of improper integration in time domain. The theoretical result relies on the pole and residues of transfer function and can be used in any kind of model order reduction technique.

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REFERENCES

[1] Analysis of power consumption in VLSI global interconnect by Youngsoo and Hyung-ok kim.

[2] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. on Computer-Aided Design*, vol. 9, no. 4,pp. 352–366, Apr. 1990.

[3] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*. Prentice Hall, 2003.

[4] K. M. Carrig, N. T. Gargiulo, R. P. Gregor, D. R. Menard, and H. E. Reindel, "A new direction in ASIC high-performance clock methodology,"

[5] in *Proc. IEEE Custom Integrated Circuits Conf.*, 1998.T. Sakurai, "Superconnect technology," *IEICE Trans. on Electron.*, vol. E84-C, no. 12, pp. 1709–1716, Dec. 2001.

[6] ——, "Approximation of wiring delay in MOSFET LSI," *IEEE Journal of Solid-State Circuits*, vol. SC-18, no. 4, pp. 418–426, Aug. 1983.

[7] D. G. at UC Berkeley. (2004) Berkeley predictive technology model. [Online]. Available: http://www-device.eecs.berkeley.edu/˜ ptm.

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