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Analysis of Several 2:1 Multiplexer Circuits at 90nm and 45nm Technologies

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Abstract- The increasing prominence of portable system and the need of limit power consumption in very high density VLSI chip have led to rapid and innovative development in low-power design during the recent years. A multiplexer, sometimes referred to as a "MUX", is a device that selects between a numbers of input signals. This paper represents the simulation of different 2:1 MUX configurations and their comparative analysis on different parameters such as Power Supply Voltage, Operating Frequency and Temperature etc.

Index Terms – *CMOS Logic, Low power, 2:1 Multiplexer and VLSI.*

INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. A 2:1 multiplexer is a basic building block of the "switch logic". The concept of the switch logic is that logic circuits are implemented as combination of switches, rather than logic gate. Multiplexers are used in building digital semiconductors such as CPUs and graphics controller, as programmable logic devices, in telecommunications, in computer networks and digital video. This paper compares the different 2:1 multiplexer circuits on the basis of the power dissipation, speed, operating frequency range and their temperature dependence.

LITERATURE REVIEW OF DIFFERENT 2:1 MULTIPLEXER CIRCUITS

2.1 NMOS MULTIPLEXER CIRCUIT

The schematic diagram of NMOS 2:1 MUX is shown in Fig. 1(a). This circuit is based on Complementary Pass Transistor Logic. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors [1]. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected

2.2 CMOS MULTIPLEXER CIRCUIT

Fig. 1(b) is depicting the circuit diagram of CMOS 2:1 multiplexer based Double Pass Transistor Logic. DPL eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors, with dual logic paths for every function.
While it has high speed due to low input capacitance, it has only limited capacity to drive a load [2].

2.3 MSL MULTIPLEXER CIRCUIT

MSL stands for multiplexer single with level restoration block which is shown in Fig.1(c). One problem with the CPL or DPL circuits is the requirement of both non-inverting and inverting signals, which leads to a large wiring area [2]. So a logic design based on CPL like circuits called MSL arised, which uses only the non-inverting output of the original CPL multiplexer circuit appended by a p-latch inverter which is the heart of this circuit [3].

2.4 MD MULTIPLEXER CIRCUIT

Schematic of MD circuit is shown in the Fig. 1(d). MD stands for multiplexer double. With the help of this circuit we find the inverted output also [3].

2.5 MDL MULTIPLEXER CIRCUIT

Schematic of MDL Based circuit is shown in the Fig. 1(e). MDL stands for multiplexer double with level restoration block. With the help of this level restoration block we can avoid swing problems, but it has high-area and high-power drawbacks [3].

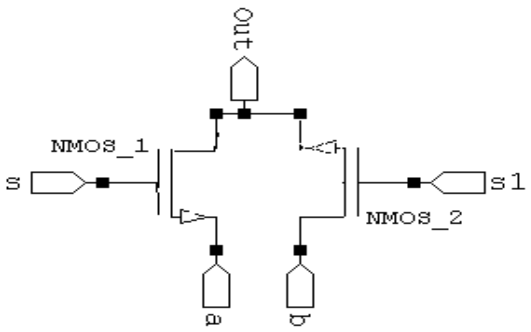
2.6 DCVSL MULTIPLEXER CIRCUIT

Schematic of DCVSL circuit is shown in the Fig. 1(f). Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. A logic function and its inverse are automatically implemented in this logic style. The pull-down network implemented by the NMOS logic tree generated complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. It can be divided it to two basic parts: a differential latching circuit and a cascaded complementary logic array [4], [5], [6].

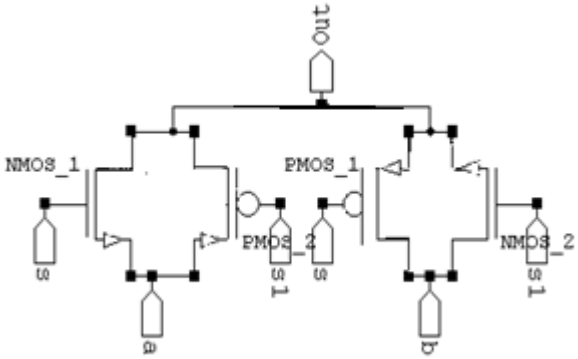
SIMULATION AND ANALYSIS

3.1 SIMULATION ENVIRONMENT

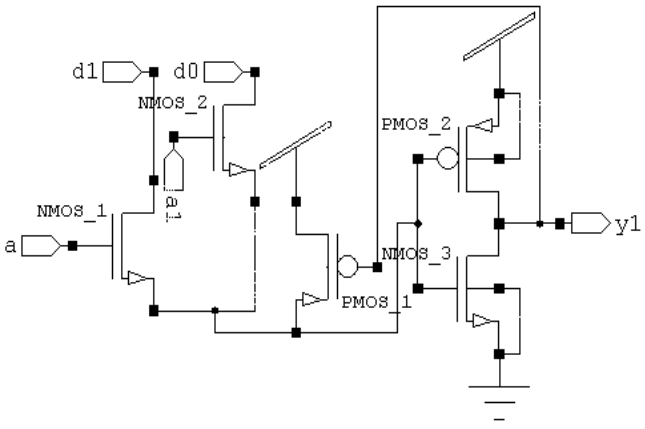
A simulation of various 2:1 multiplexer is done using Tanner EDA Tool on version 13.0. Various 2:1 multiplexer circuits simulations are performed on BSIM3v3 90nm and 45nm technologies with supply voltage ranging from 0.6V to 1.4V. In order to find out the optimized design in terms of power, delay, power-delay product, the simulation have been carried out at varying supply voltages, temperatures and operating frequencies.



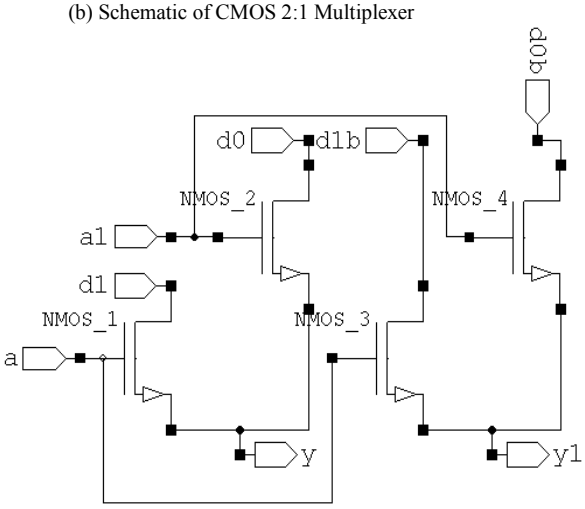
(a) Schematic of NMOS 2:1 Multiplexer



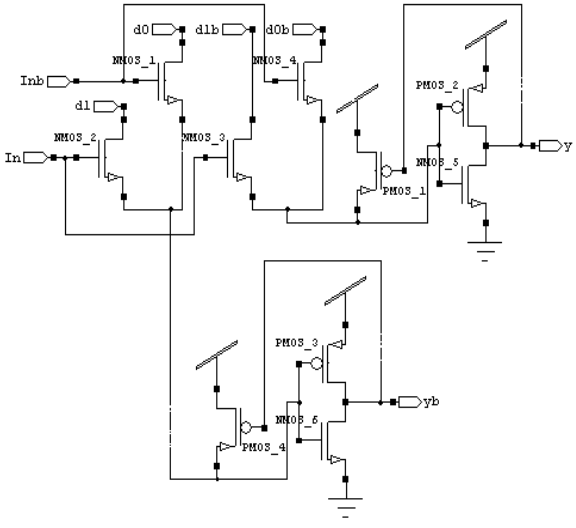
(b) Schematic of CMOS 2:1 Multiplexer



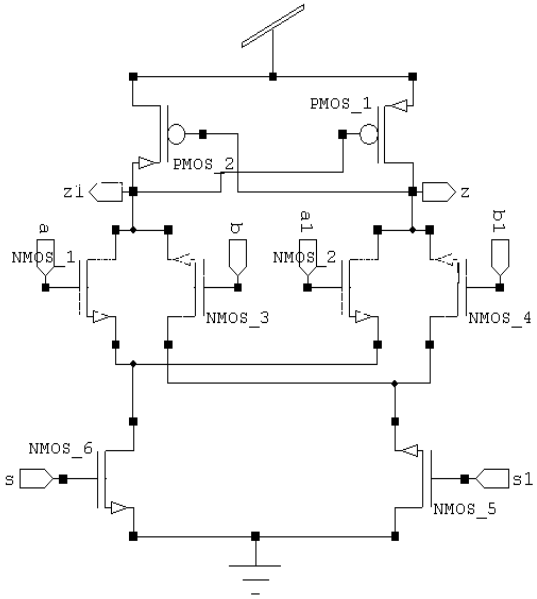
(c) Schematic of MSL circuit



(d) Schematic of MD circuit



(e) Schematic of MDL circuit



(f) Schematic of DCVSL circuit

Fig.1 Different 2:1 Multiplexer's Topologies (a) NMOS Design (b) CMOS Design (c) MSL Design (d) MD Design (e) MDL Design (f) DCVSL Design

To establish an impartial simulation circumstance, each circuit have been tested on the same input patterns which covers every possible combination of input a, b and s.

3.2 SIMULATION ANALYSIS

The graph shown in Fig.2, Fig.3, Fig.10, Fig.11 and Fig.12 reveals that the power consumption of DCVSL circuit is remarkably reduced than the other approaches at 90nm and 45nm technology. The delays of all the circuits are shown in Fig.4, Fig.5, Fig.13 and Fig.14. DCVSL approach shows slightly more delay than the delay of other design for input voltage ranging from 0.6V to 1.4V. Similar results for power consumption Vs operating frequency and power consumption Vs temperature are shown in Fig.6, Fig.7, Fig.15, Fig.8, Fig.9 and Fig.16 respectively at 90 and 45 nm technology. As it is found from the simulations DCVSL circuit shows better performance for the range of operating frequency and

A. At 90 nm technology

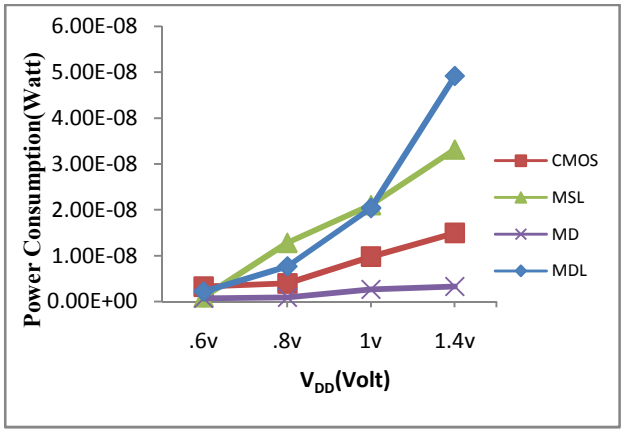


Fig.2 Power consumption comparison of various 2:1 multiplexer technologies at different supply voltages

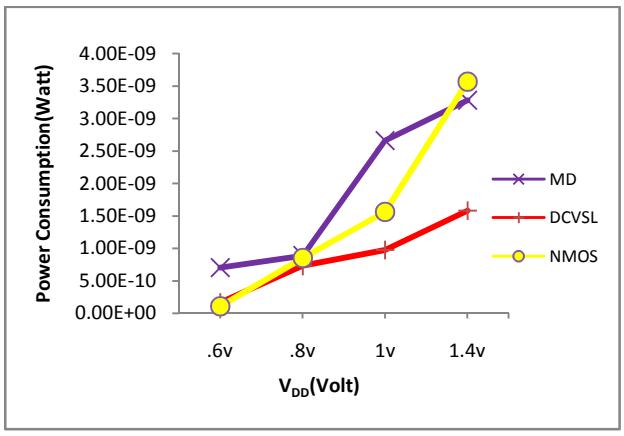


Fig.3 Power consumption comparison of various 2:1 multiplexer technologies at different supply voltages

operating temperature among all the other design approaches for 2:1 Multiplexers.

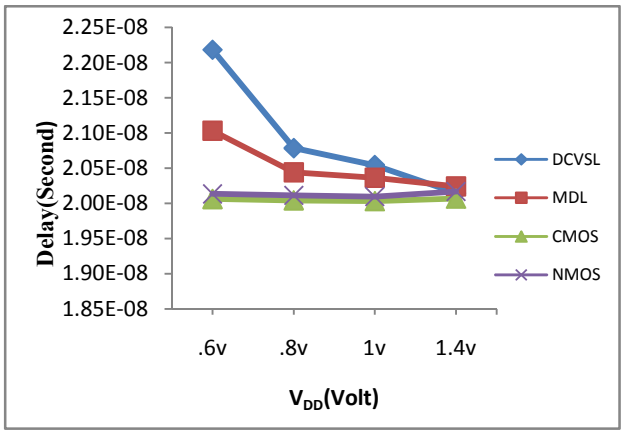


Fig.4 Delay comparison of various 2:1 multiplexer technologies at different supply voltages

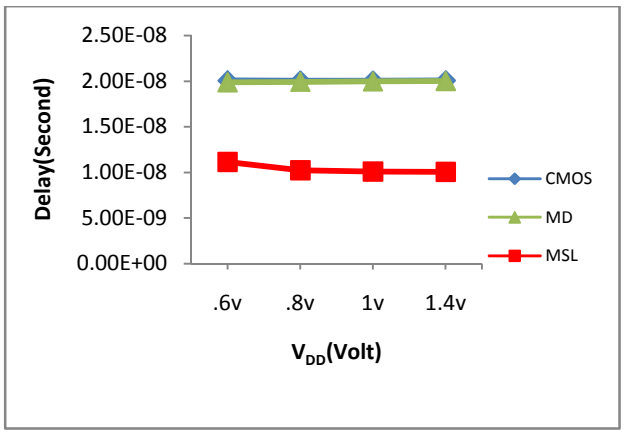


Fig.5 Delay comparison of various 2:1 multiplexer technologies at different supply voltages

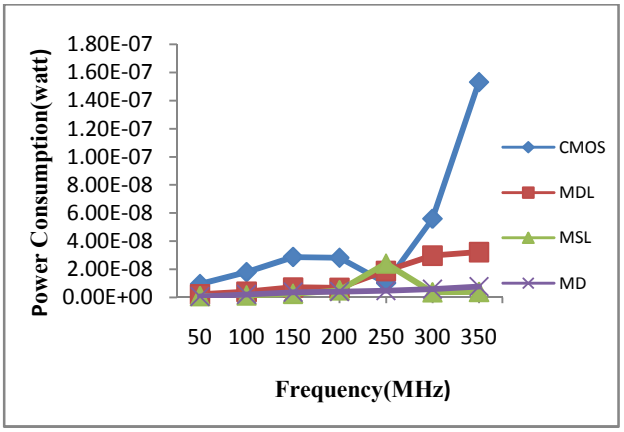


Fig.6 Power consumption comparison of various 2:1 multiplexer technologies at different operating frequencies

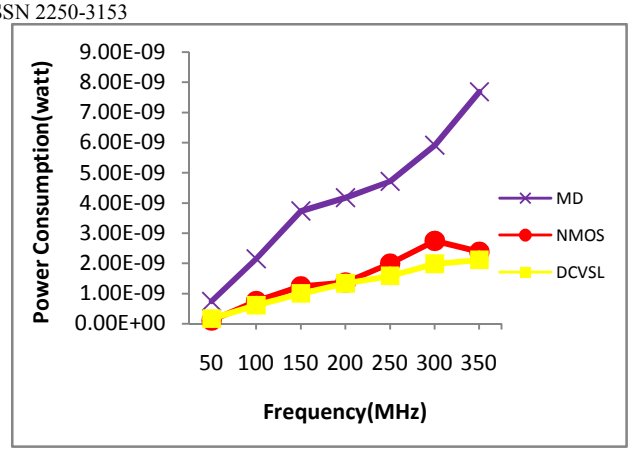


Fig.7 Power consumption comparison of various 2:1 multiplexer technologies at different operating frequencies

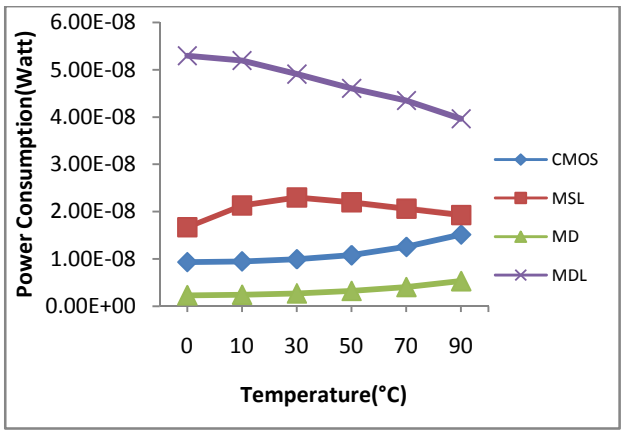


Fig.8 Power consumption comparison of various 2:1 multiplexer technologies at different temperatures

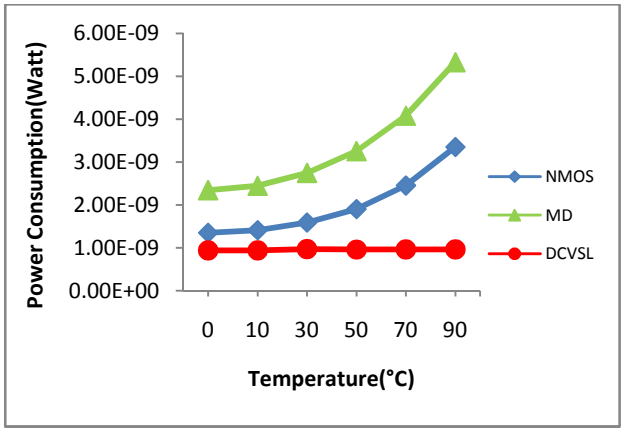


Fig.9 Power consumption comparison of various 2:1 multiplexer technologies at different temperatures

B. At 45nm technology

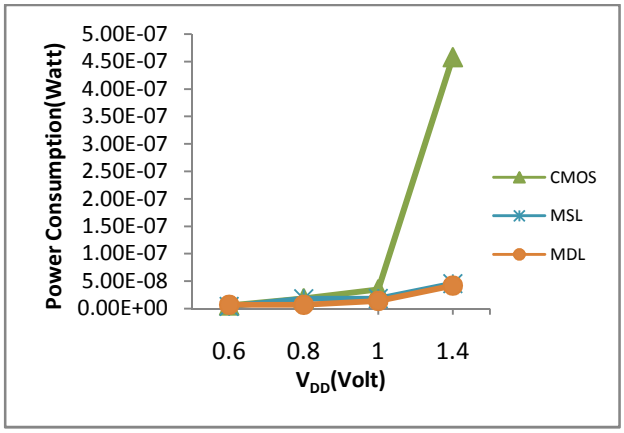


Fig.10 Power consumption comparison of various 2:1 multiplexer technologies at different supply voltages

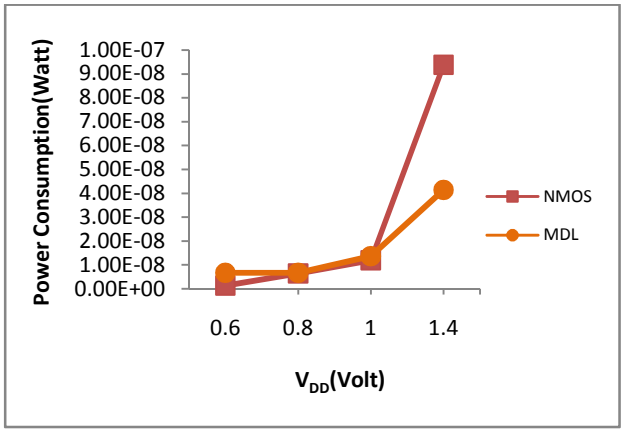


Fig.11 Power consumption comparison of various 2:1 multiplexer technologies at different supply voltages

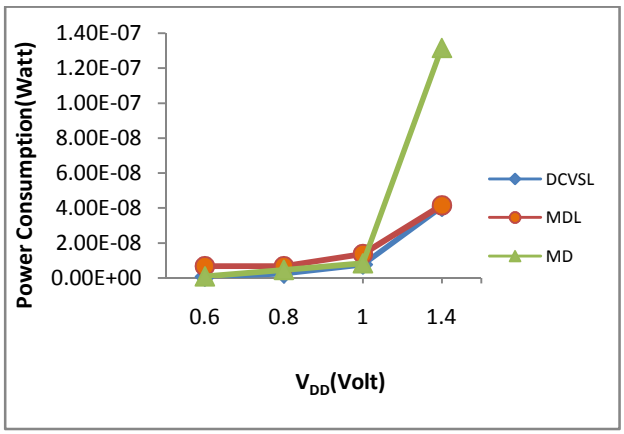


Fig.12 Power consumption comparison of various 2:1 multiplexer technologies at different supply voltages

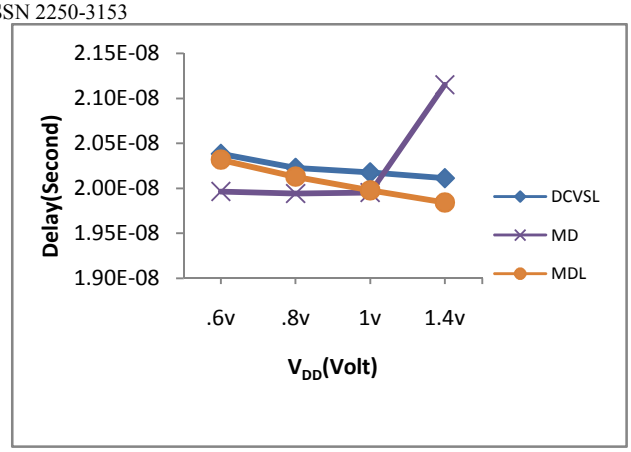


Fig.13 Delay comparison of various 2:1 multiplexer technologies at different supply voltages

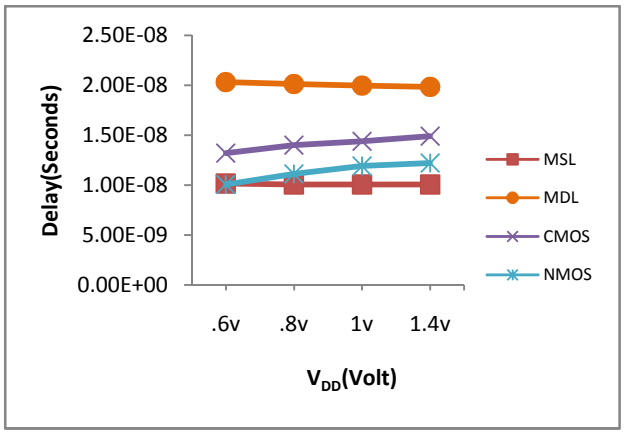


Fig.14 Delay comparison of various 2:1 multiplexer technologies at different supply voltages

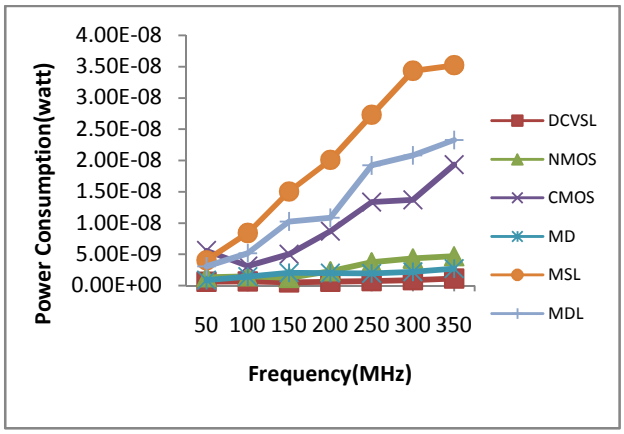


Fig.15 Power consumption comparison of various 2:1 multiplexer technologies at different operating frequencies

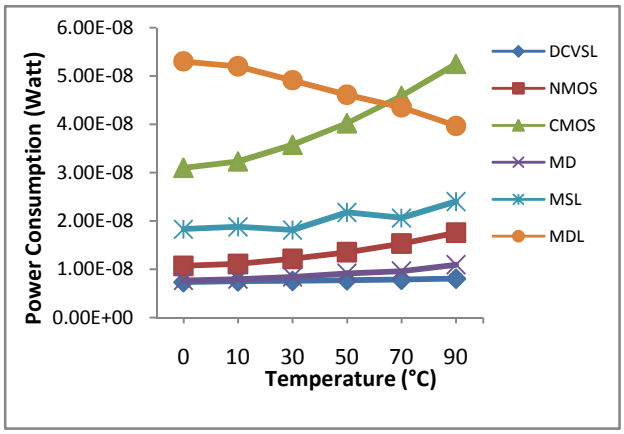


Fig.16 Power consumption comparison of various 2:1 multiplexer technologies at different temperatures

Table I and Table II show the Power delay product over a range of power supply voltages at 90nm and 45nm technology and as it is shown in the table that DCVSL circuit for 2:1 multiplexer shows minimum Power Delay Product.

Different 2:1 Mux circuits	Power Delay Product (90nm) (Watt-sec)			
	V_{DD}=.6v	V_{DD}=.8v	V_{DD}=1v	V_{DD}=1.4v
NMOS	2.17E-18	1.71E-17	3.13E-17	7.18E-17
CMOS	6.54E-17	7.94E-17	1.96E-16	3.00E-16
MSL	1.08E-17	1.31E-16	2.12E-16	3.32E-16
MD	1.39E-17	1.76E-17	5.30E-17	6.56E-17
MDL	4.61E-17	1.57E-16	4.15E-16	9.94E-16
DCVSL	**3.70E-18**	**1.52E-17**	**2.00E-17**	**3.18E-17**

Table I. Power delay product comparison of different 2:1 multiplexer circuits at 90 nm technology

Different 2:1 Mux circuits	Power Delay Product (45nm) (Watt-sec)			
	V_{DD}=.6v	V_{DD}=.8v	V_{DD}=1v	V_{DD}=1.4v
NMOS	1.34E-17	7.07E-17	1.61E-16	1.14E-15
CMOS	7.41E-17	2.59E-16	5.00E-16	6.82E-15
MSL	4.11E-17	1.78E-16	1.83E-16	8.55E-16
MD	1.73E-17	9.12E-17	1.65E-16	2.78E-15
MDL	1.38E-16	1.36E-16	2.73E-16	8.23E-16
DCVSL	**1.24E-17**	**5.10E-17**	**1.52E-16**	**8.16E-16**

Table II. Power delay product comparison of different 2:1 multiplexer circuits at 45 nm technology

CONCLUSION

For low-leakage and high-speed circuits concern should be on both the factors Speed and Power[7]. This paper concluded with the efficient approach of multiplexer at 90nm and 45nm technology. Differential Cascade Voltage Switch Logic (DCVSL) shows least Power Consumption over a range of Power Supply Voltage, Power-Delay product, operating frequency and operating temperature over other circuit design of 2:1 multiplexer.

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