

# Proposed Telescopic Op-Amp with Improved Gain

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**Abstract-** Before venturing further on the design of our operational amplifier, the first line of business is to determine the optimal topology for the given specifications. The factor that clearly stands out is the high dynamic range requirement of 85 db. Several topologies are given for this task, among these telescopic op-amp is selected. Compensation techniques are used with two stage topology of telescopic operational amplifier (op-amp). Miller compensation technique is used with null resistor to obtain such a high gain. The op-amp is designed on 0.13um technology CMOS process with 5 v power supply and achieved a dc gain of 85dB with a 177.1MHz unity gain frequency.

**Index Terms-** Op-amp, miller capacitance, unity gain frequency, dc gain

## I. INTRODUCTION

Designing high-performance analog circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The realization of a CMOS operational amplifier that combines high dc gain with high unity-gain frequency has been a difficult problem. To obtain high gain telescopic cascode op-amp is used[1].

A telescopic cascode op-amp, as shown in Fig.1, typically has higher frequency capability and consumes less power than other topologies. Its high-frequency response stems from the fact that its second pole corresponding to the source nodes of the n-channel cascode devices is determined by the transconductance of n-channel devices as opposed to p-channel devices. In the telescopic op-amp shown in Fig.1, all transistors are biased in the saturation region. M1–M2, M7–M8, and the tail current source M9 must have at least  $V_{ds, sat}$  to offer good common-mode rejection, frequency response, and gain [2].

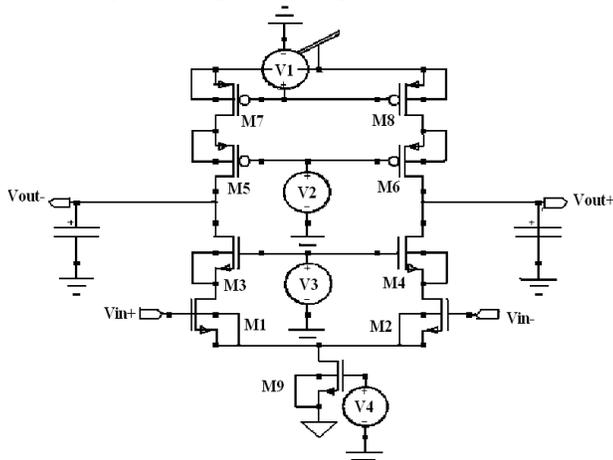


Fig.1 Telescopic cascode operational amplifier

## II. COMPENSATION TECHNIQUE

Op-amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems. However, as CMOS design scales into low-power, low-voltage and short-channel CMOS process regime, satisfying both of these aspects leads to contradictory demands, and becomes more and more difficult, since the intrinsic gain of the devices is limited [4]. Therefore, techniques for op-amp open loop gain enhancement are necessary.

To maintain stability in a two-stage amplifier, some form of compensation must be applied inside the feedback loop. Miller compensation technique with two stage topology is used with telescopic op-amp, which significantly reduces the frequency of dominant pole and moves the output pole away from the origin, this effect is called “pole splitting” is a common technique in op-amp design.

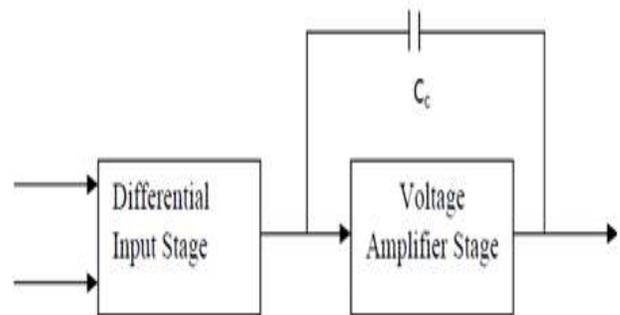


Fig.2.1 Implementaion of pole splitting (Miller Compensation)

In this method, a capacitor,  $C_c$ , is connected in parallel with a second stage. Miller’s theorem states that the impedances seen in parallel with a gain stage can be modled as an impedance connected from the input of that gain stage to the ground, and an impedance connecting from the output of that gain stage to the ground. Since the impedance in this case is purely capacitive and second stage has inverting gain, the first capacitor has a reflected capacitance of  $C_c(1+A)$ , where  $A$  is the gain of the second stage. When a large capacitance is needed to reduce the pole of the first stage, it can be generated by a smaller capacitor and described Miller multiplication[5][6].The second capacitor has a value much closer to the compensation capacitor  $C_c$ , especially for large gains. Compensation capacitor ( $C_c$ ) between the output of the gain stages causes pole-splitting and achieves dominant pole compensation [8][9].

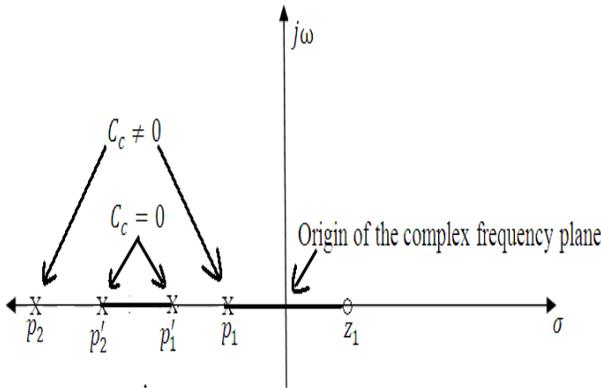


Fig.2.2 Pole splitting

### III. PROPOSED STRUCTURE

To achieve higher dc-gain in the simple Telescopic op-amp, Miller compensation method can be used. Fig.3.1 shows the complete structure of the proposed op-amp[4].

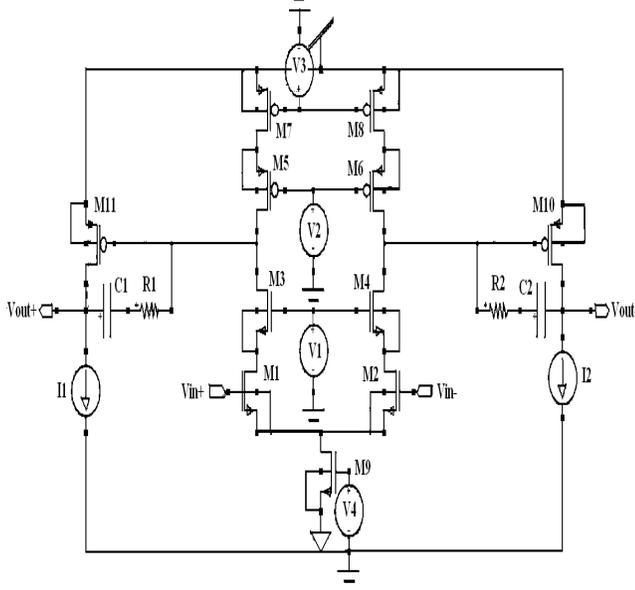


Fig.3.1 Schematic of proposed telescopic operational amplifier

Capacitors C1 and C2 are used as miller capacitors and resistors R1 and R2 are null resistors. All devices are assumed to operate in saturation region using the simplified square law drain current model given by:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

### IV. DC GAIN

As we can see, the total current injected to the output node is

$$I_{out} = \alpha(g_{m1,2} V_{in} + g_{mM7,8} V_{out})$$

The differential dc-gain of this op-amp can be written as:

$$A_{vo} = \alpha \times g_{mM7,8} \times R_{out}$$

By using miller compensation technique, gain of two stage telescopic operational amplifier rises up to 85db. Proposed Telescopic op-amp shows better performance when circuit area is

not a major concern. To get better stability, RC compensation network is used, R was set to be 1 KΩ and capacitor to be 0.2pf.

### V. SIMULATION RESULTS

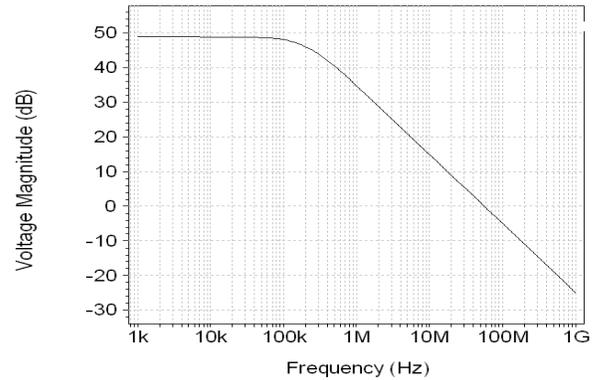


Fig.5.1 Frequency v/s gain response of Conventional telescopic op-amp

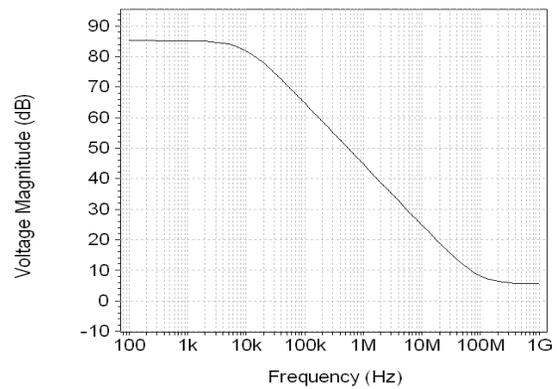


Fig.5.2 Frequency v/s gain response of proposed telescopic op-amp

Simulation result shows that the proposed telescopic op-amp achieves unity gain band width of 177.1 MHz, which is about 3.18 times that of the conventional Telescopic op-amp.

Table 1: (Design Specifications with simulation results)

Parameter	Conventional Telescopic op-amp	Proposed telescopic op-amp
Technology	130 μm	130 μm
Power Supply(v)	5v	5v
Compensating Resistance(Ω)	.....	1K
Compensating Capacitance(p.f.)	.....	0.2
Gain(dB)	49	85
Unity gain bandwidth	55.67MHz	177.1MHz

Simulation results shows that the proposed circuit improves the parameters such as the unity gain frequency (GBW), phase margin, gain, stability. The obtained gain is large enough for practical applications. This approach is efficient and viable to improve the gain, bandwidth and the phase margin.

## VI. CONCLUSION

In this work a 0.13  $\mu\text{m}$  telescopic operational amplifier, using compensation technique, has been presented and simulated with a supply voltage of 5 V. Telescopic op- amp is selected as it suits best for the purpose.

## REFERENCES

- [1] P. Gray and R. Meyer, "Recent advances in monolithic operational amplifier design," IEEE Transactions on Circuits and Systems, vol. CAS-21, no. 3, pp. 317–327, May 1974.
- [2] D. Johns and K. Martin, Analog Integrated Circuit Design. New York: John Wiley & Sons, Inc., 1996.
- [3] J. Huijsing, R. Hogervorst, and K.-J. de Langen, "Low-power low-voltage vlsi operational amplifier cells," IEEE Transactions on Circuits and Systems, vol. 42, no. 11, pp. 841–852, Nov. 1995
- [4] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd Ed. New York: Oxford University Press, 2002.
- [5] B. Razavi, Design of analog CMOS integrated circuits. New York: McGraw-Hill, 2001.
- [6] R. Eschauzier, L. Kerklaan, and J. Huijsing, "A 100-mhz 100-db operational amplifier with multipath nested miller compensation structure," IEEE J. Solid- State Circuits, vol. 27, no. 12, pp. 1709–1717, Dec. 1992.
- [7] R. Eschauzier and J. Huijsing, Frequency compensation techniques for low-power operational amplifiers. Boston, MA: Kluwer, 1995.
- [8] K. N. Leung and P. Mok, "Analysis of multistage amplifier-frequency compensation," IEEE Transactions on Circuits and Systems, vol. 48, no. 9, pp. 1041–1056, Sep. 2001.
- [9] P. Chan and Y. Chen, "Gain-enhanced feedforward path compensation technique for pole-zero cancellation at heavy capacitive loads," IEEE Transactions on Circuits and Systems, vol. 50, no. 12, pp. 933–941, Dec. 2003.

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