ISSN 2250-3153

Area efficient 0.18um Cmos phase frequency detector for high speed Pll

Ms. Vaijayanti Lule [1], Prof. (Ms.) Vrushali Nasre [2]

B.D.C.O.E. Sewagram,
Wardha – 442001, India

Abstract- Two phase frequency detectors (PFDs) are proposed in this paper that can overcome the speed and area limitations of conventional PFD. The AND gate based PFD uses 22 transistors. It consumes 161.41uW power when operating at 50MHz clock frequency with 1.8V supply voltage. The NOR gate based PFD uses 20 transistors and preserves the main characteristics of conventional PFD. It consumes 96.67uW power at 50MHZ with 1.8V supply. The designs are implemented using 0.18um cmos process in Tanner 13.0v and can operate up to 1GHz frequency. These can be used in PLL for high speed applications.

Index Terms – phase frequency detector, phase locked loop, CMOS integrated circuits, tanner

I. INTRODUCTION

The phase-locked loop (PLL) plays the role of generating a clock signal that is usually a multiple of a reference clock and synchronized with the reference clock in phase. The PLL is widely used in many applications such as frequency synthesis, phase modulation, phase/frequency demodulation, and clock data recovery. In most cases, the charge pump PLL (CP-PLL) is used due to its high frequency range and simple structure. The basic block diagram of the PLL is shown in the Fig.1. In general a PLL consists of five main blocks:

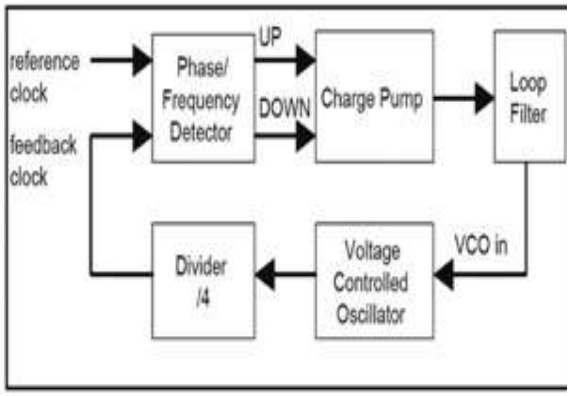

Fig.1 PLL Block Diagram

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

In the PLL, the phase frequency detector (PFD) compares the rising edges of the reference clock and the voltage-controlled oscillator (VCO) clock, and generates a lead signal when the reference phase is leading or a lag signal when the reference phase is lagging. The phase difference detected in the PFD passes through the loop filer to control the VCO. As the phase difference critically affects the overall characteristics of the PLL such as lock-in time and jitter performance, the PFD should be designed to work accurately for any phase difference.

II. CONVENTIONAL PFD

An ideal phase detector produces an output signal whose dc value is linearly proportional to the differences between the phases of two periodic inputs.

$V = Kpd * \Delta\text{ø}$ (1)

Where K_{pd} is the gain of the phase detector and ΔØ is the phase difference between the input signals. PFD generates an output pulse whose width is equal to the time difference between consecutive zero crossings of the input signals. The block diagram of the conventional PFD is shown in Fig.2 and Fig.3 shows the waveform for PFD.

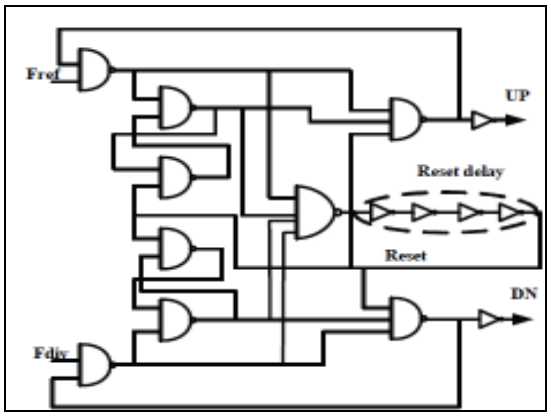

Fig.2 Conventional PFD

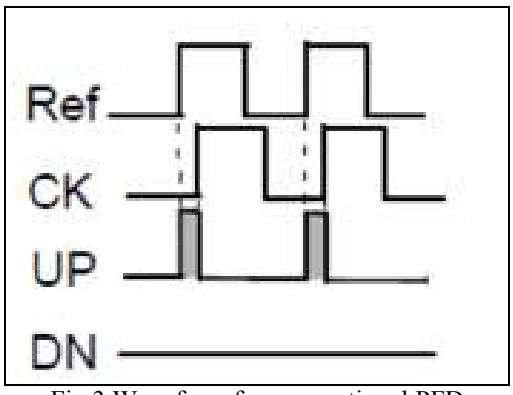

Fig.3 Waveform for conventional PFD

The con-PFD has large dead zone in phase characteristics at the steady state, which generates a large jitter in locked state in PLL. Also, a large amount of power consumption cannot be avoided in high frequency operations because internal nodes of the con-PFD are not completely pull up or pull down. Furthermore, the maximum speed of the con-PFD is limited and uses 48 transistors hence the area is also increased.

III. CIRCUIT DESCRIPTION

A. PFD using AND Gate

This paper presents two PFD architectures having low area and can work on higher frequencies. Fig.4 shows the phase frequency detector using AND gate. The circuit consists of two resettable, edge triggered

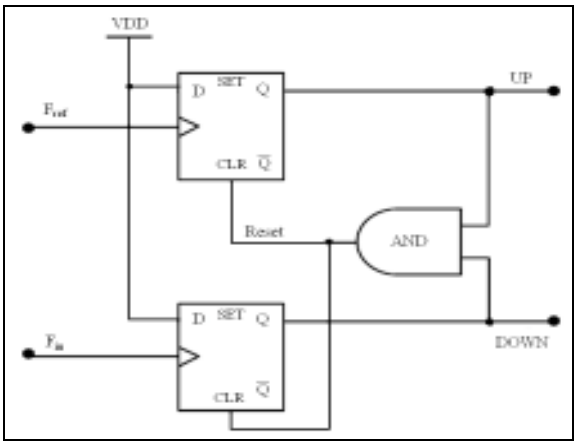

Fig.4 AND gate based PFD

D flip flops with their D inputs tied to logic 1. The Ref and Clk serve as clocks of the flipflops. Suppose the rising edge of REF leads that of CLK, then UP goes to logic high. UP keeps high until the rising edge of CLK makes DN on high level. Because UP and DN, are ANDed, so RESET goes to logic high and resets the PFD into the initial state.The schematic of AND gate based PFD circuit consisting of only 22 transistors is as given in Fig.5.

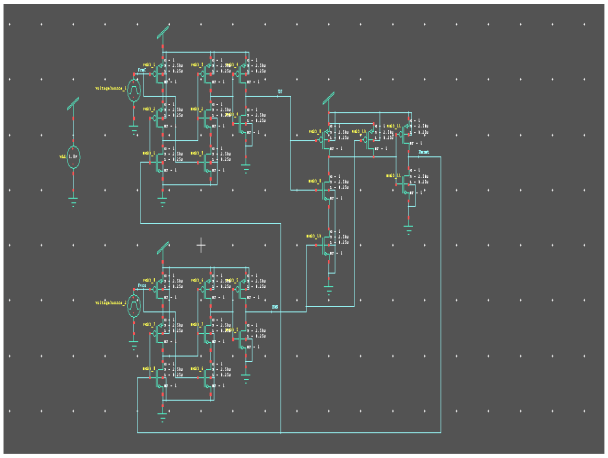

Fig.5 Schematic of AND gate based PFD

B. PFD using NOR Gate

Fig.6 shows the phase frequency detector using NOR gate. The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1. The Ref and Clk serve as clocks of the flip flops. The UPb and DNb signals are given as input to the NOR gate. Suppose the rising edge of REF leads that of CLK, then UPb goes to logic low i.e. UP keeps high until the rising edge of CLK makes DNb on low level. Because UPb and DNb, are NORed, so RESET goes to logic high and resets the PFD into the initial state.

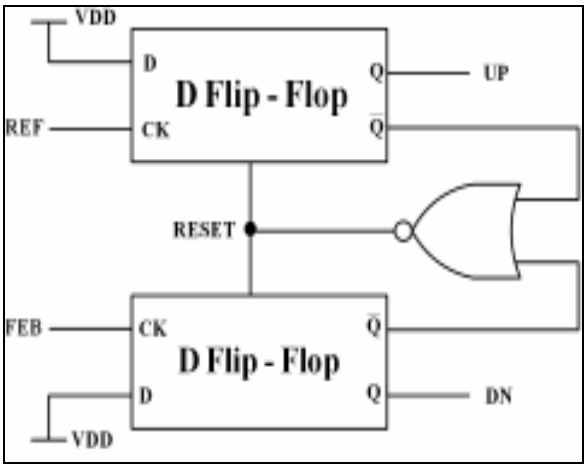

Fig.6 PFD using NOR gate

The circuit is implemented in Tanner 13.0v with only 20 transistors. The schematic of the NOR based PFD is as shown in Fig.7.

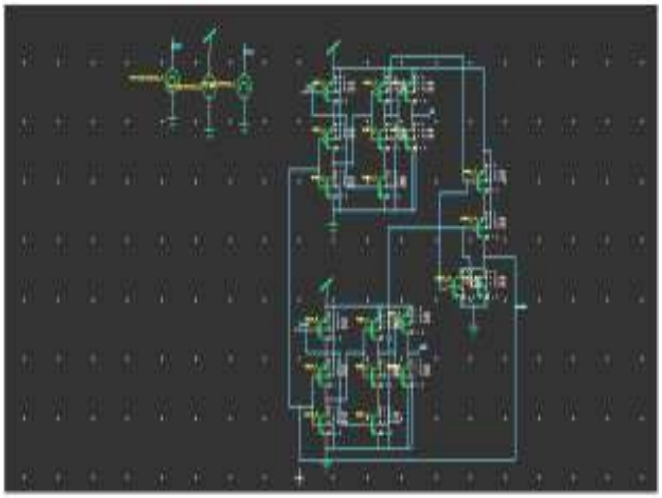

Fig.7 Schematic of NOR based PFD

IV. SIMULATION RESULTS

The AND gate based PFD circuit is simulated on Tanner 13.0 at 1.8V to obtain the results with the input frequency of 1GHz and the two inputs are 90° out of phase.

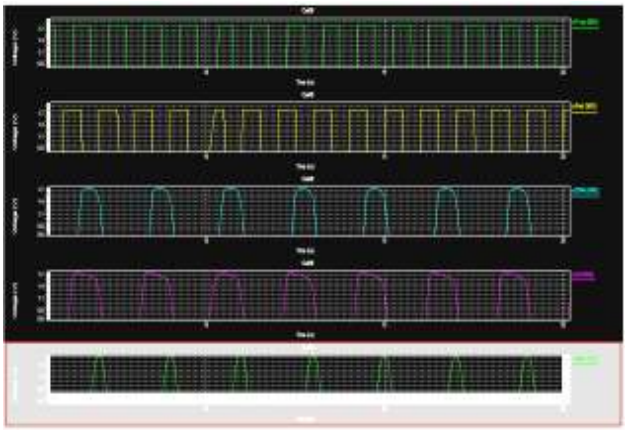

Fig.8 The waveforms of the AND gate based PFD when the input frequency is 1GHz and the two inputs are 90° out of phase.

The NOR gate based PFD circuit is simulated on Tanner at 1.8V to obtain the results with the input frequency of 1GHz and the two inputs are 90° out of phase.

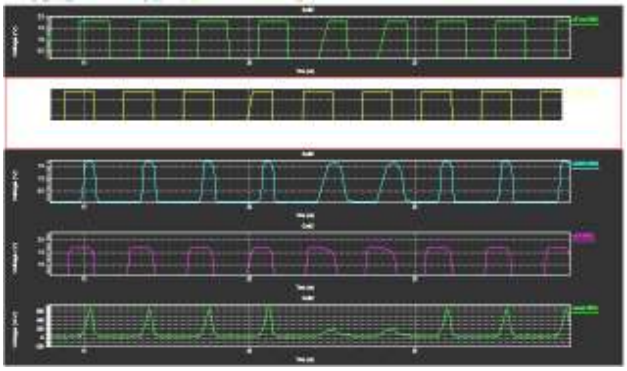

Fig.9 The waveforms of the NOR gate based PFD when the input frequency is 1GHz and the two inputs are 90° out of phase.

The two circuits can be simulated when Fref and Fvco have different frequencies. Fig.10 shows the waveform for NOR based PFD when Fref is greater than Fvco. The UP signal goes high at the rising edge of Fref and the DN signal goes high at the rising edge of Fvco. When both UP and DN signals become logic high the circuit is reset to initial state. The pulse width of UP and DN signal is proportional to the frequency difference between the two inputs.

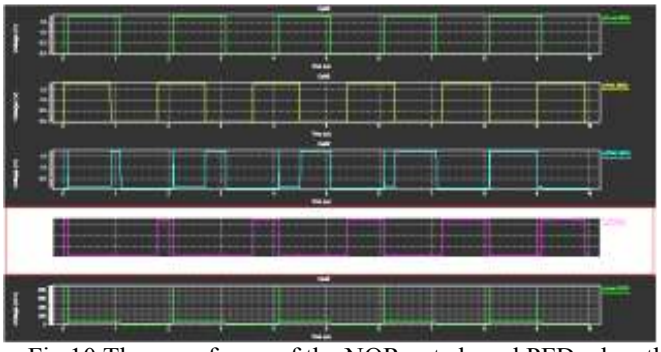

Fig.10 The waveforms of the NOR gate based PFD when the Fref is greater than Fvco

V. PERFORMANCE COMPARISON

TABLE 1

PFD TYPE	MAXIMUM OPERATING FREQUENCY	POWER CONSM-PTION AT 50MHZ	NO. OF TRANSI-STORS	DEAD ZONE
Con-PFD	500MHz	335uW	48	-
AND gate based PFD	1GHz	161.4uW	22	50ps
NOR gate based PFD	1GHz	96.67uW	20	40ps

VI. CONCLUSION

This paper presents two PFD designs implemented in 0.18um CMOS process. The AND gate PFD consists of 22 transistors and the NOR gate PFD consists of only 20 transistors. Both the PFDs can operate upto 1GHz frequency and preserves the main functionality of conventional PFD with low power consumption. The performance of the two PFDs is compared against the conventional PFD in table 1.

REFERENCES

[1] D. H. Kim, et al, "Clock and data recovery circuit with two exclusive OR phase frequency detector", in IEEE Electronics Letters, vol. 36, no. 16, Aug. 2000, pp 1347 – 1349.

[2] W. Hu, et al, "Fast frequency acquisition phase frequency detector with zero blind zone in PLL", in IEEE Electronics Letters, vol. 43, no. 19, Sep. 2007.

[3] H. O. Johansson, "A simple precharged CMOS phase frequency detector", in IEEE Journal of Solid State Circuits, vol. 33, no. 2, Feb. 1998, pp 295 - 299.

[4] R. Y. Chen, et al, "A high speed fast acquisition CMOS phase frequency detector for MB-OFDM UWB", in IEEE Transaction on Consumer Electronics, vol. 53, no. 1, Feb. 2007, pp 23 - 26.

[5] N. M. H. Ismail, et al, "CMOS phase frequency detector for high speed application", in 4th International Design and Test Workshop, Nov 2009.

[6] K. Park, et al, "Fast frequency acquisition phase frequency detector with prediction based edge blocking", in IEEE International Symposium on Circuits and Systems, 2009, pp 1891 - 1894.

[7] B. Razavi, "Design of Analog CMOS Integrated Circuits" , Prentice Hall, 1998.

[8] R.Jacob Baker, CMOS Circuit Design, Layout and Simulation.

[9] Weste, CMOS VLSI Design

First Author – Vaijayanti Lule, B.D.C.O.E,Sevagram,Wardha, Addr-Opp.Indira Market, Wardha-442001, (MH), India
vaiju_lule@yahoo.co.in

Second Author – Prof (Ms).Vrushali G Nasre, Asst. Prof. P. G. Department of Engineering,B.D.C.O.E. Sevagram, Wardha, (MH), India, vrushnasre@gmail.com