Low Power Low Voltage Bulk Driven Balanced OTA

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Abstract- The last few decades, a great deal of attention has been paid to low-voltage (LV) low-power (LP) integrated circuits design since the power consumption has become a critical issue. Among many techniques used for the design of LV LP analog circuits, the Bulk-driven principle offers a promising route towards this design for many aspects mainly the simplicity and using the conventional MOS technology to implement these designs. This paper is devoted to the Bulk-driven (BD) principle and utilizing this principle to design LV LP building block of Operational Transconductance Amplifier (OTA) in standard CMOS processes and supply voltage 0.9V. The simulation results have been carried out by the Spice simulator using the 130nm CMOS technology from TSMC.

Index Terms- Bulk-driven Metal Oxide Semiconductor, Operational Transconductance Amplifier, Balanced Operational Transconductance Amplifier, and Body effect.

I. INTRODUCTION

Integrated circuits design has recently gone in the direction of LV and LP design, especially in the environment of portable systems where a low supply voltage, given even by a single cell battery, is used. An important factor concerning analog circuits is that; the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. Though the MOS transistor is a four terminal device, it is most often used as a three terminal device since the bulk terminal is tied either to the source terminal, to VDD or to VSS. Therefore, a large number of possible MOS circuits are overlooked; hence a good solution to overcome the threshold voltage is to use the Bulk-driven principle [1-3]. The principle of the Bulk-driven method is that; the gate-source voltage is set to a value sufficient to form an inversion layer, and an input signal is applied to the bulk terminal. In this manner, the threshold voltage can be either reduced or removed from the signal path. The operation of the Bulk-driven MOS transistor is much like a JFET i.e. a depletion type device, it can work under negative, zero, or even slightly positive biasing condition. Since the bulk voltage affects the thickness of the depletion region associated with the inversion layer i.e. the conduction channel, the drain current can be modulated by varying the bulk voltage through the body.

II. BULK-DRIVEN DIFFERENTIAL STAGE

When the input devices of the bulk-driven differential pair in Fig. 1 operate in the strong inversion saturated region, their drain current is given by

$$I_D = \frac{1}{2} k'_p \left(\frac{W}{L}\right) (V_{SG} - |V_{TH}|)^2 \quad (1)$$

where the symbols have their usual meaning and the channel length modulation effect has been neglected. The behavior of the threshold voltage as a function of the bulk-to-source voltage VBS of the input devices can be expressed as

$$|V_{TH}| = |V_{TH0}| + |\gamma| \left[\sqrt{2|\Phi_F| + V_{BS}} - \sqrt{2|\Phi_F|}\right] \quad (2)$$

where V_{TH0} is the value of the threshold voltage V_{TH} when V_{BS} is zero, γ is the body effect parameter, and Φ_F is Fermi potential. The operation of bulk-driven devices is based on the body effect, that is, on the dependence of V_{TH} on V_{BS}. Indeed, from (1) and (2), I_D changes when changing V_{BS} and, hence, a transconductance function between the bulk voltage and the drain current is achieved. The transconductance of a bulk-driven MOS transistor may be obtained from (1) and (2) as

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}} = \frac{|\gamma| g_m}{2\sqrt{2|\Phi_F| + V_{BS}}} = \frac{|\gamma|}{2\sqrt{2|\Phi_F| + V_{BS}}} \sqrt{2\beta I_D} \quad (3)$$

where g_m is the gate transconductance of the device. If typical values for γ and Φ_F are considered, the value of g_{mb} ranges from 20% to 50% the value of g_m.

III. BULK DRIVEN BALANCED OTA

The Bulk-driven OTA was presented in [4-6]. The two-stage OTA is shown in Fig. 1. It consists of two stages, the first which is combined of the Bulk-driven differential stage with NMOS input devices M1 and M2 and the current mirror M3 and M4 acting as an active load. By setting the gate-source voltage to a value sufficient to turn on the transistor, then the operation of the Bulk-driven MOS transistor becomes a depletion type. Input voltage is applied to the bulk-terminal of the transistor to modulate the current flow through the transistor. OTA with Bulk-driven input transistors has been designed. The design is depicted in Fig 1 and the simulation results are shown in Table 1.

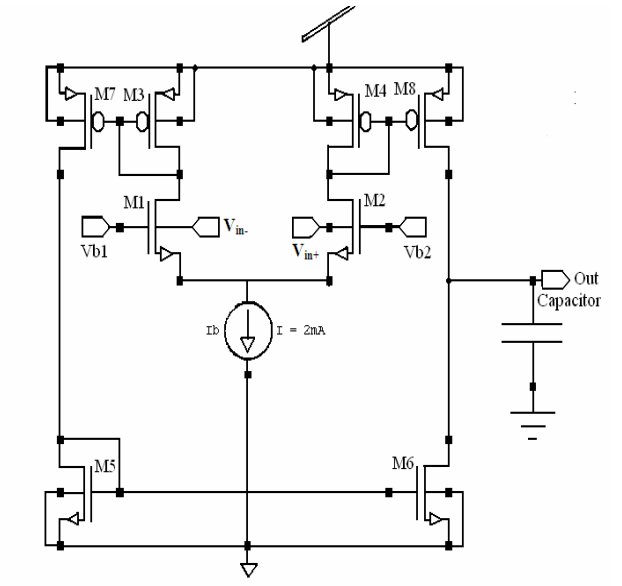

Fig 1 Bulk Driven Balanced OTA

IV. SIMULATION RESULTS FOR BULK DRIVEN BALANCED OTA

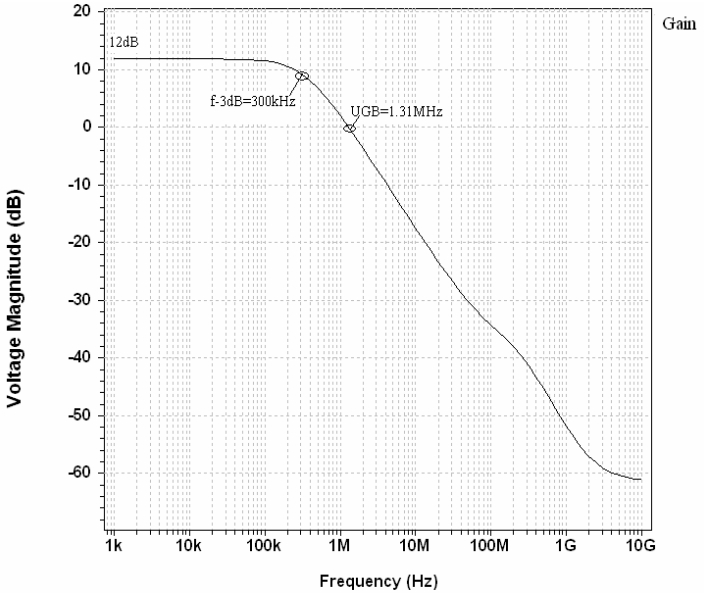

Fig 2 Voltage Gain of Bulk Driven Balanced OTA

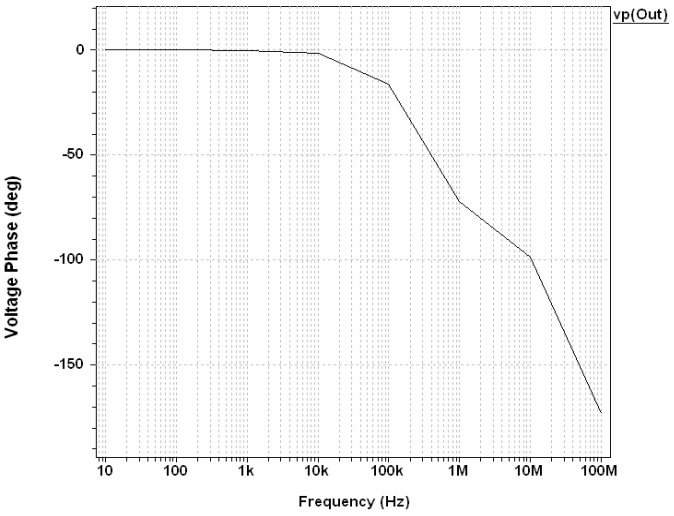

Fig 3 Voltage Phase of Bulk Driven Balanced OTA

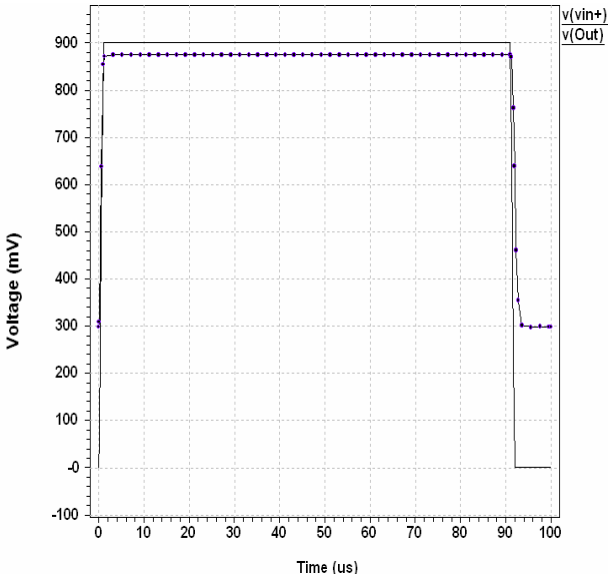

Fig 4 Slew rate of Bulk Driven Balanced OTA

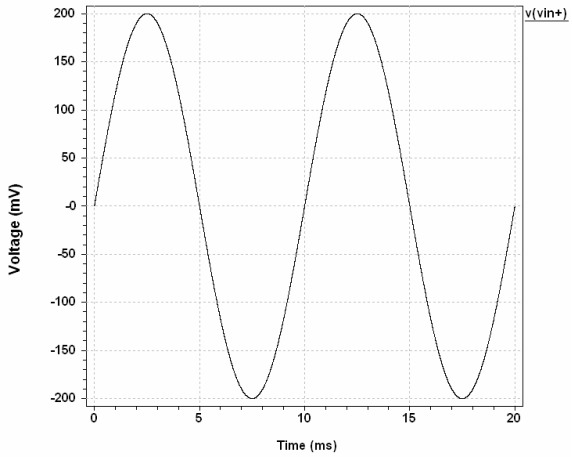

Fig 5(a) Input Voltage Swing of Bulk Driven Balanced OTA

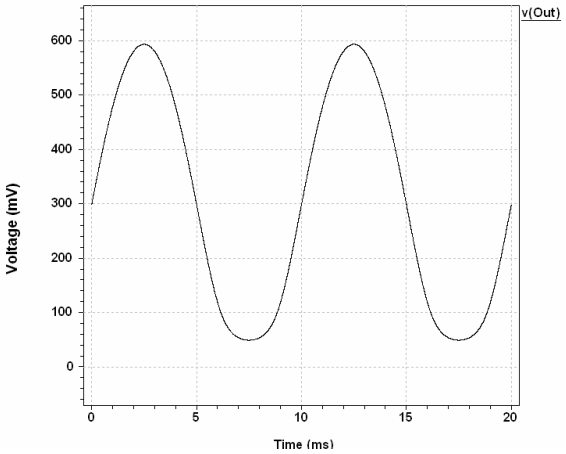

Fig 5(b) Output Voltage Swing of Bulk Driven Balanced OTA

The characteristics of Bulk Driven balanced OTA are shown in Fig 2 to Fig 5. The gain of Bulk Driven Balanced OTA is 12 dB and phase margin is 107º. The slew rate is shown in Fig 3, we are obtaining positive slew rate of 543mV/ µs and negative slew rate of 226mV/ µs. The input and output voltage swings are shown in Fig 5(a) and Fig 5(b). It is observed that for an input swing of 200mV we are getting a output swing of 550 mV.

The above simulations are done with Capacitor load 1pF and constant current source of 2µA and 0.9 V power supply. The simulations are done with the help of Tanner EDA tool T-SPICE and waveforms are analyzed on W-Edit. All designs are done using 130nm TSMC MOSIS Level-49 model file.

Table 1 Simulated Results of Bulk Driven Balanced OTA

Characteristics	**Simulated results**
Power consumption	3.9µW
Open loop gain	12 dB
Phase Margin	107º
3 dB Bandwidth	300kHz
Unity Gain Bandwidth	1.31MHz
Positive Slew Rate Negative Slew Rate	543mV/µs 226mV/ µs
Maximum voltage swing	550mV

V. CONCLUSION

This paper demonstrates the principle of Bulk-driven MOS transistor and the way of employing this principle in LV LP analog circuit design. Furthermore, this principle is used to design LV LP Bulk-driven OTA Balanced OTA.

Based on the results we could summarize the following *desirable characteristics* of Bulk-driven transistors:

- Low-voltage low-power consumption of the circuits.
- Design simplicity and the acceptable features of the circuits.
- Depletion characteristics avoid VT requirement in the signal path.
- The conventional front gate could be used to modulate the Bulk-driven MOS transistor.

Based on the results we could summarize the following *undesirable characteristics* of Bulk-driven transistors:

- The transconductance of a Bulk-driven MOST is smaller than that of a conventional Gate-driven, which may result in lower GBW in OTA
- The polarity of the Bulk-driven MOST is technology related. For a P (N) well CMOS process, only N (P) channels Bulk-driven MOSTs are available. This may limit its applications. For example a rail-to-rail Bulk-driven op-amp needs a dual well process to realize it, this process is more expensive, bigger chip area needed and it has worst matching comparing with one well process.
- Prone to turn on the bulk-channel PN junction, which may result in a latch-up problem.

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