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Analysis and Simulation of New Seven Level Inverter Topology

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Abstract- This paper demonstrates how the reduced harmonic distortion can be achieved for a new topology of multilevel inverters. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels. The modes of operation are outlined for 5-level inverter, as similar modes will be realized for higher levels. Simulations of seven level of the proposed inverter topology along with corroborative experimental results are presented. This paper deals with the analysis and simulation of the seven level inverter. This paper presents the seven level inverter with harmonics reduction along with the reduction.. The harmonic reduction is achieved by selecting appropriate switching angles. The functionality verification of the seven level inverter is done using MATLAB.

Index Terms- New topology of MlI, Fundamental Switching Frequency, PWM, THD

I. INTRODUCTION

The multi level inverter was first introduced in 1975. The three level converters was the first multi level inverter introduced. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multi level inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic computability, and lower switching losses. [1][2] While many different multilevel inverter topologies have been proposed, the two most common topologies are the cascaded H-bridge inverter and its derivatives [3], and the Diode-clamped inverter [4]. The main advantage of both topologies is that the rating of the switching devices is highly reduced to the rating of each cell. However, they have the drawback of the required large number of switching devices which equals 2(*k*-1) where *k* is the number of levels. This number is quite high and may increase the circuit complexity, and reduce its reliability and efficiency.

Cascaded H-bridge inverter has a modularized layout and the problem of the dc link voltage unbalancing does not occur, thus easily expanded to multilevel. Due to these advantages, cascaded H-bridge inverter has been widely applied to such applications as HVDC, SVC, stabilizers, and high power motor drives. Diode-clamped inverter needs only one dc-bus and the voltage levels are produced by several capacitors in series that divide the dc bus voltage into a set of capacitor voltages. Balancing of the capacitors is very complicated especially at large number of levels. Moreover, three-phase version of this topology is difficult to implement due to the neutral-point balancing problems.

The output waveforms of multilevel inverters are in a stepped form; therefore they have reduced harmonics compared to a square wave inverter. To reduce the harmonics further, carrier-based PWM methods are suggested in the literature [5].

This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed PWM technique. This new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. It can also be extended to any number of levels. The modes of operation of a 5-level inverter are presented, where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on PWM with help of pulse generator. These angles are obtained from solving the waveform equations using the theory of resultants. Simulation of higher levels of the proposed inverter topology is carried out using MATLAB The validity of the proposed topology and the harmonic elimination method are verified experimentally for 7 level inverters

II. MULTILEVEL INVERTER NEW TOPOLOGY

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The circuit configuration of the new 5-level inverter is shown in Fig.1. It has four main switches in H-bridge configuration Q1~Q4, and two auxiliary switches Q5 and Q6. The number of dc sources (*two*) is kept unchanged as in similar 5-level conventional cascaded H-bridge multilevel inverter. Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Fig.2. The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, and for the sake of simplicity, the modes of operation will be illustrated for 5-level inverter, these modes are

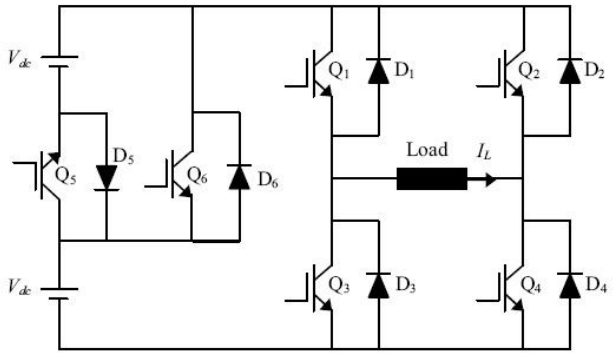

Fig 1: The 5-level inverter of the new topology

Powering Mode This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is *Vdc*, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is *2Vdc*, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively.

Free-Wheeling Mode Free-wheeling modes exist when one of the main witches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.

Regenerating Mode In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4

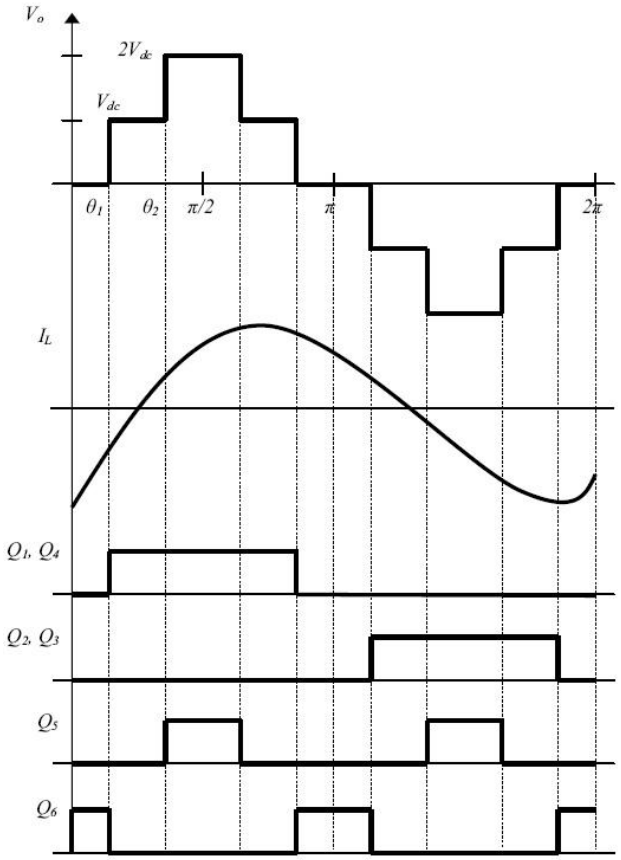

Fig 2: Waveforms of the proposed 5-level inverter

The 7-level version of the proposed topology is shown in Fig.3, where another dc supply, and two auxiliary switches, Q7 and Q8, are added while keeping the four main switches, Q1~Q4, unchanged. The corresponding output voltage waveform, load current, and gating signals are shown in Fig.4, where the abovementioned modes of operation can also be realized.

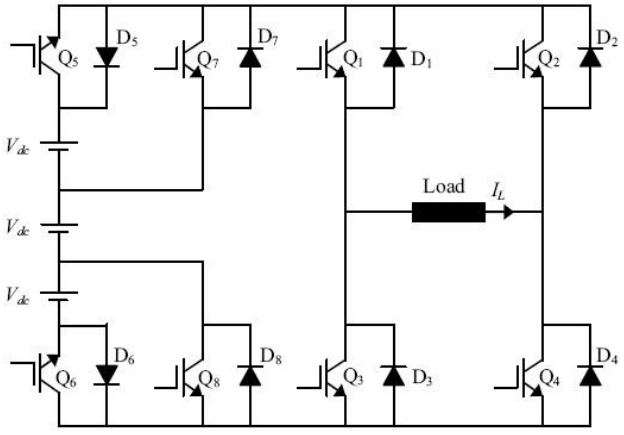

Fig 3: The 7-level inverter of the new topology

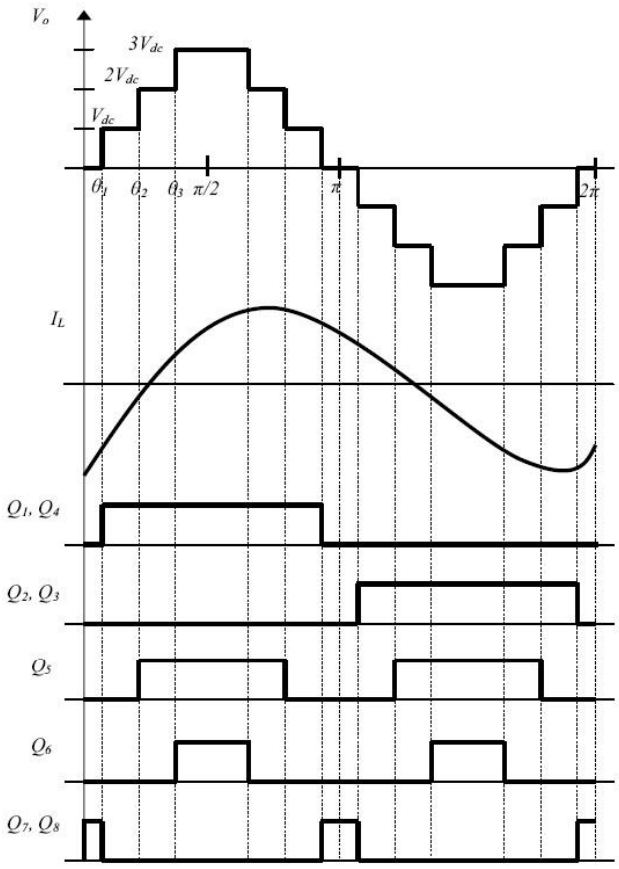

Fig. 4: Waveforms of the proposed 7-level inverter

A generalized circuit configuration of the new topology is shown in Fig.5. The proposed topology has the advantage of the reduced number of power switching devices, but on the expense of the high rating of the main four switches. Therefore, it is recommended for medium power applications

The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1.

Table 1: Percentage reduction in switching devices

	Number of Switches			
Inverter Type	5- level	7- level	9- level	11- level
Cascaded H Bridge	8	12	16	20
Proposed Topology	6	8	10	12
% Reduction	25 %	33.3%	37.5%	40%

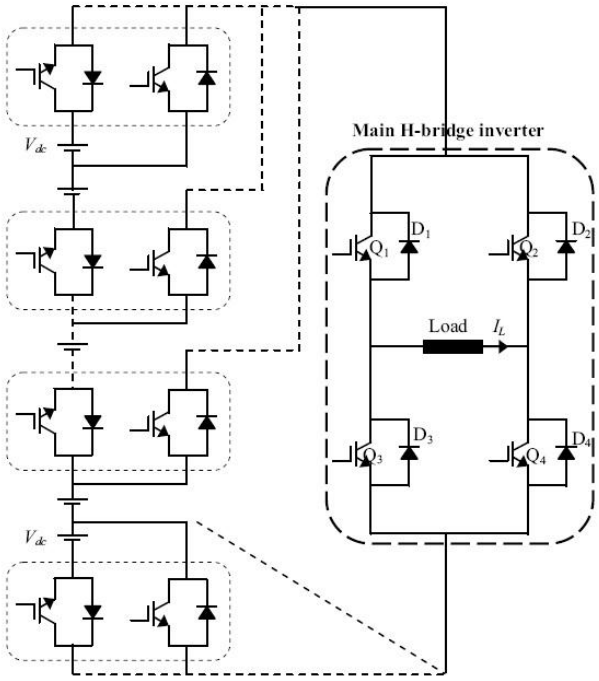

Fig. 5: Generalized multilevel inverter configuration of the new topology

III. MATHEMATICAL METHOD OF SWITCHING

In order to verify the ability of the proposed multilevel inverter topology to synthesize an output voltage with a desired amplitude and better harmonic spectrum, programmed PWM technique is applied to determine the required switching angles. It has been proved that in order to control the fundamental output voltage and eliminate n harmonics, therefore n+1 equations are needed. Therefore, 7-level inverter, for example, can provide the control of the fundamental component beside the ability to eliminate or control the amplitudes of two harmonics, not necessarily to be consecutive. The method of elimination will be presented for 7-level inverter such that the solution for three angles is achieved.The Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme shown in Fig.2 is as follows:

$$V(\omega t) = \left(\frac{4VDC}{\pi}\right) \Sigma [\cos(n\theta_1) + \cos(n\theta_2) + \ldots\ldots\ldots + \cos(n\theta_s)] \sin(n\omega t)$$

where n = 1, 3, 5, 7, ...

…… (4)

Where s is the number of dc sources in the multilevel inverter. Ideally, given a desired fundamental voltage V1, one wants to determine the switching angles $\theta_1, \theta_2, \theta_3, \ldots$ θ_s so that Vo(_t)=V1sin(_t), and a specific higher harmonics of Vn(n_t) are equal to zero.

To eliminate 5th, 7th, and 9th order harmonics, the firing angles for each level is found by solving the following equations

The switching angles can be found by solving the following equations:

$$\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4) = 3m_a$$

$$\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4) = 0$$

$$\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4) = 0$$

Where $m=V1/(4Vdc/\pi)$, and the modulation index ma is given by ma=m/s, where $0 \leq m_a \leq 1$

Where $\theta_1, \theta_2, \theta_3, \theta_4$ are the firing angles in degrees.
The switching pulses are obtained by carrying out the above calculation.

Polynomial systems were considered to compute the solutions of the harmonic elimination equations by iterative numerical methods which give only one solution [8]. In contrast, this system of polynomial equations will be solved using resultant such that all possible solution of (4) can be found. A systematic procedure to do this is known as elimination theory and uses the notion of
resultants. The details of this procedure can be found in [9]. One approach to solving the set of nonlinear transcendental equations (4), is to use an iterative method such as the Newton-Raphson method [6]. In contrast to
iterative methods, the approach here is based on solving polynomial equations using the theory of resultants which produces all possible solutions [7]. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. Then the resultant method is employed to find the solutions when they exist. These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11th and 13th harmonics). These sets of solutions have to be examined for its corresponding total harmonic distortion (THD) in order to select the set which generate the lowest harmonic distortion (mostly due to the 11th and 13th harmonics).

IV. SIMULATION RESULTS

The feasibility of the proposed approach is verified using computer simulations. A model of the seven-level inverter is constructed in MATLAB-Simulink software. **A** new strategy with reduced number of switches is employed. For cascaded H bridge 7 level inverter requires 12 switches to get seven level output voltage and with the proposed topology requires 8 switches. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels The schematic of the cascaded H bridge seven level inverter and proposed new seven level topology built in MATLAB-Simulink is illustrated in Fig. 6 and Fig. 7 respectively

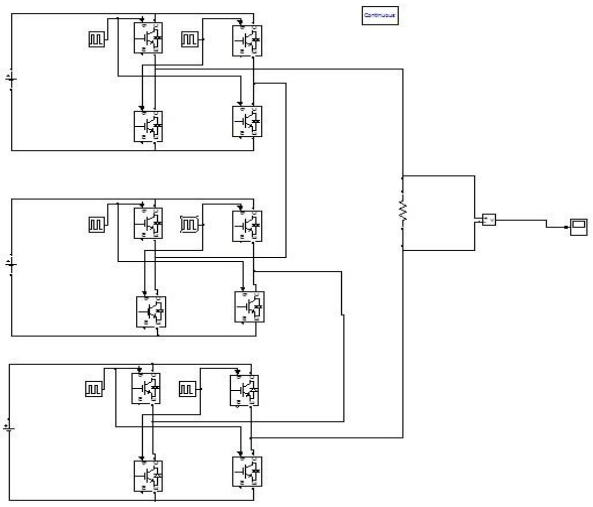

Fig 6: Schematic of Conventional Seven Level Inverter

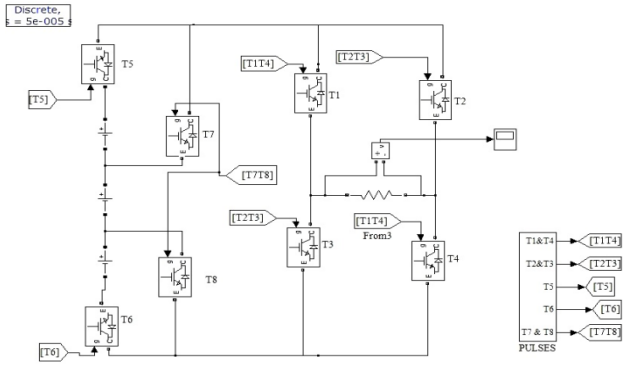

Fig.7 Schematic of Conventional Seven Level Inverter

And similarly for three phase seven level inverter is built as illustrated in the Fig.8. The switching patterns adopted are applied for the proposed topology and switches to generate seven output voltage levels at 0.9 modulation index and the switching pattern are shown in the Fig.9 Simulation results for 7-level inverter at Vdc=50Vs, ma=0.9 where s=3 and corresponding output voltages for proposed seven level inverter are shown in Figs. 10 and similarly for three phase to ground and phase to phase voltages are shown in Fig 11 and Fig.12 respectively.

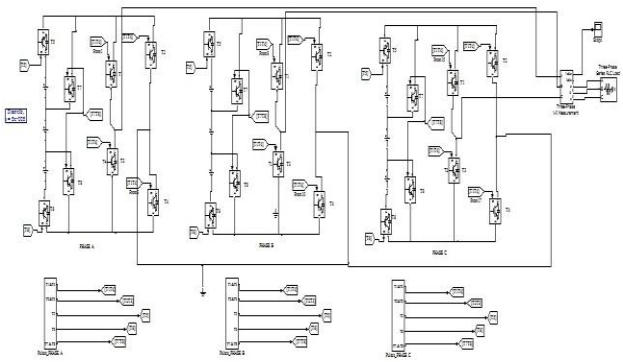

Fig. 8 Schematic of Three Phase Seven Level Inverter

Fig. 9 switching pattern of Single Phase Seven Level Inverter topology

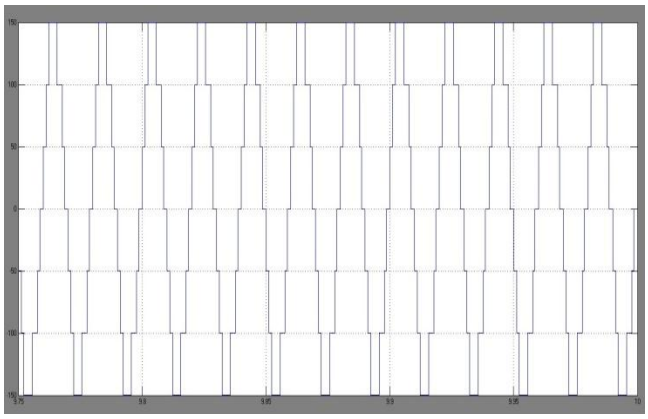

Fig. 10 Output Voltage for Single Phase Seven Level Inverter

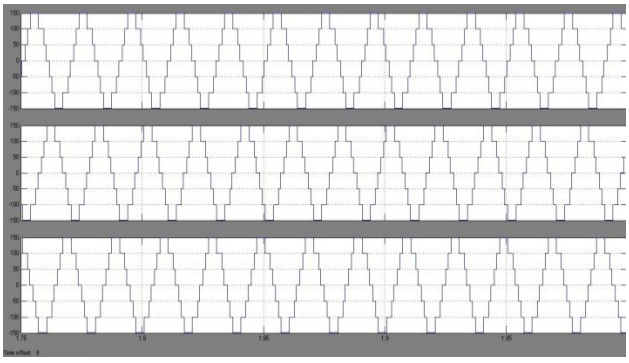

Fig. 11 Phase to ground voltage for Three Phase Seven Level Inverter

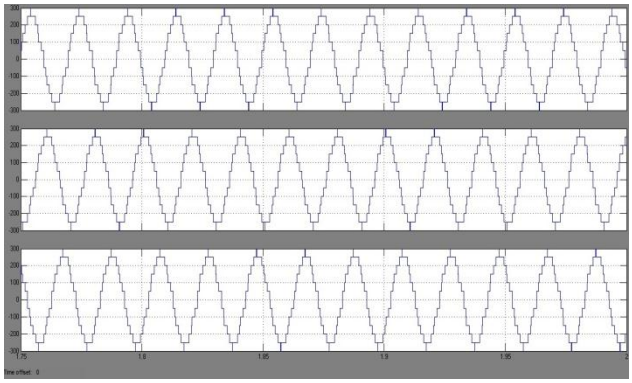

Fig. 12 Phase to Phase voltage for Three Phase Seven Level Inverter

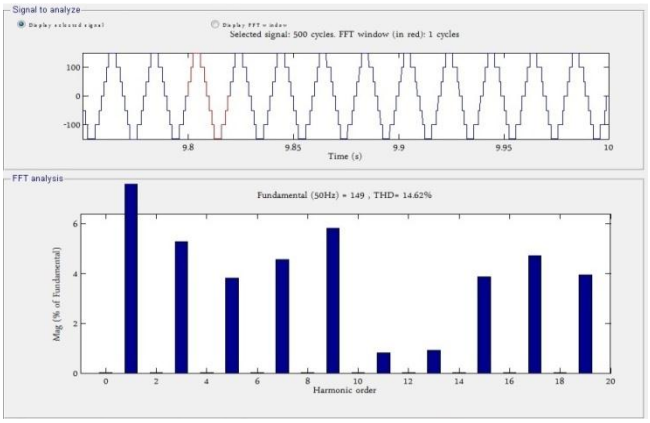

Fig.13 FFT Analysis

The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 14.62 at 149V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.13, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

V. CONCLUSION

A new family of multilevel inverters has been presented and built in MATLAB-Simulink. It has the advantage of its reduced number of switching switches compared to conventional similar inverters. However, the high rating of its four main switches limits its usage to the medium voltage range. The modes of operation and switching strategy of the new topology are presented. A PWM algorithm is applied with the help of pulse generator and based on the theory of resultant has been applied for harmonic elimination of the new topology. Since the solution algorithm is based on solving polynomial equations, it has the advantage of finding all existed solutions, where the solution produces the lowest THD is selected. Other PWM methods and techniques are also expected to be successively applied to the proposed topology. The simulation results show that the

algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

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