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Low Power Different Sense Amplifier Based Flip-flop Configurations implemented using GDI Technique

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Abstract- In this paper, Sense Amplifier based Flip-flop (SAFF) is implemented in three different configurations using Gate Diffusion Input (GDI) Technique. Experimental Results verified that proposed designs have reduced power consumption, reduced area & Temperature sustainability. Both singe edge triggered SAFF (SET-SAFF) & double edge triggered SAFF (DET-SAFF) are presented here. Considerable reduction in power consumption is observed in DET-SAFF design as compared to SET-SAFF. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm technology.

Index Terms- CMOS digital integrated circuits, double edge triggered, flip-flops, GDI Technique, latch topology, low power sense amplifier based flip-flop, single edge triggered, Tanner EDA.

I. INTRODUCTION

Traditional CMOS logics had been modified using different low power techniques to achieve reduced power consumption[1]. A new technique known as Gate diffusion input (GDI) technique for low-power digital circuit design is described in this paper. This technique allows reduced power consumption, reduced area of digital circuits while maintaining low complexity of logic design. In this paper we focus on a sense-amplifier flip-flop (SAFF) that has lower power consumption compared to other conventional flip-flops. SAFF incorporates a precharged sense amplifier in the first stage to generate a negative pulse, and a Set-Reset (SR) latch in the second stage to capture the pulse and hold the results. Since our proposed design is based on SAFF, let us first consider the operation of sense-amplifier flip-flop in more detail. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. Data dependent SAFF (DD-SAFF) utilizes data dependency to lower power consumption. Dual edge triggering results in halving the clock frequency, so again reducing power consumption [2][3][4][5].

II. SENSE AMPLIFIER BASED FLIP-FLOP

In general, a flip-flop consists of two stages: a pulse generator (PG) and a slave latch (SL). The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage as shown in Figure1.Sense Amplifier based Flip-flop (SAFF) is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch, depending whether the output is to be set or reset[6]. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge[7]. Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the transition and holds the state until the next leading edge of the clock arrives [8]. After the clock returns to inactive state, both outputs of the SA stage assume logic one value [9]. Therefore, the whole structure acts as a flip-flop. This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic [10].

III. SAFF TOPOLOGIES

A. Conventional SAFF with CMOS NAND Latch Design

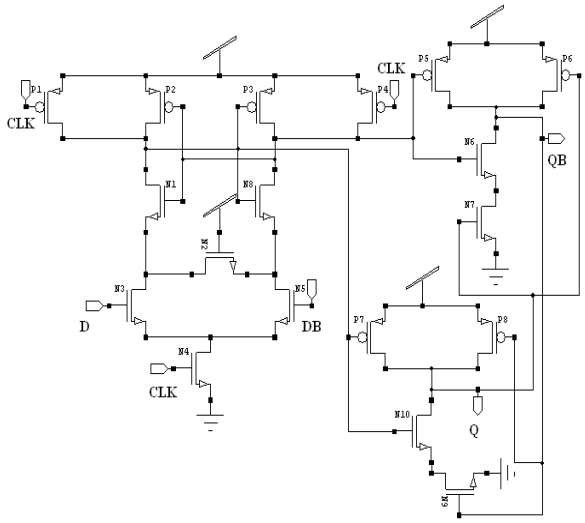

Figure 1: SAFF with CMOS-NAND Latch Design

B. Conventional SAFF with CMOS Symmetric Latch Design

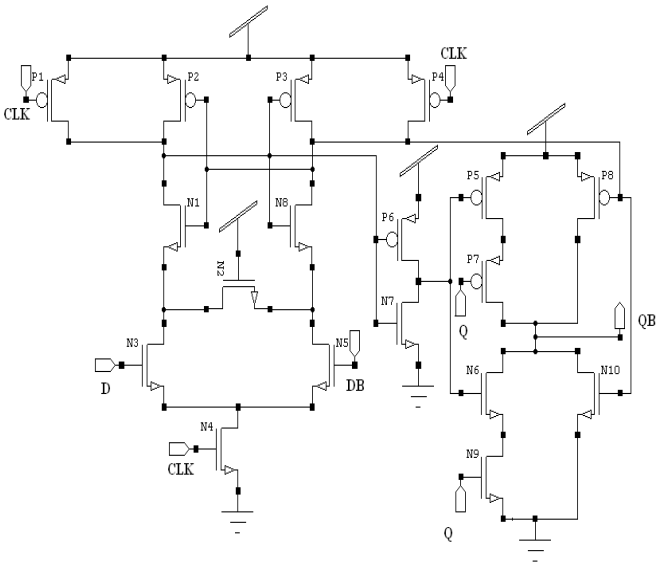

Figure 2: SAFF with CMOS-Symmetric Latch

C. Proposed SAFF with Latch using GDI Technique Design

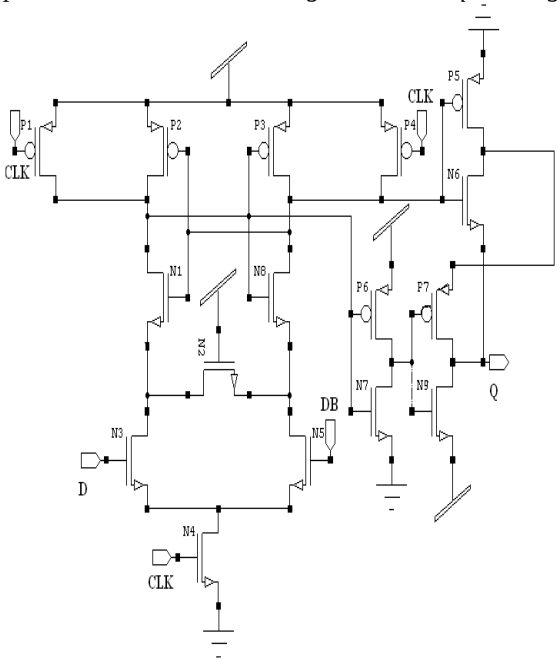

Figure 3: SAFF with latch implemented with GDI Technique

D. *Conventional Data-Dependent SAFF with CMOS-NAND Latch Design*

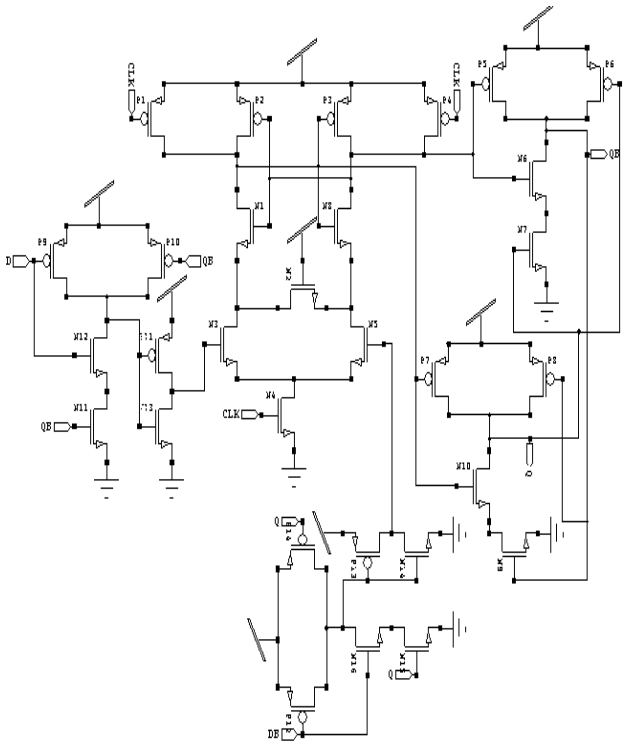

Figure 4: Data-Dependent SAFF with CMOS-NAND Latch Design

E. Proposed Data-Dependent SAFF with Latch implemented with GDI Technique

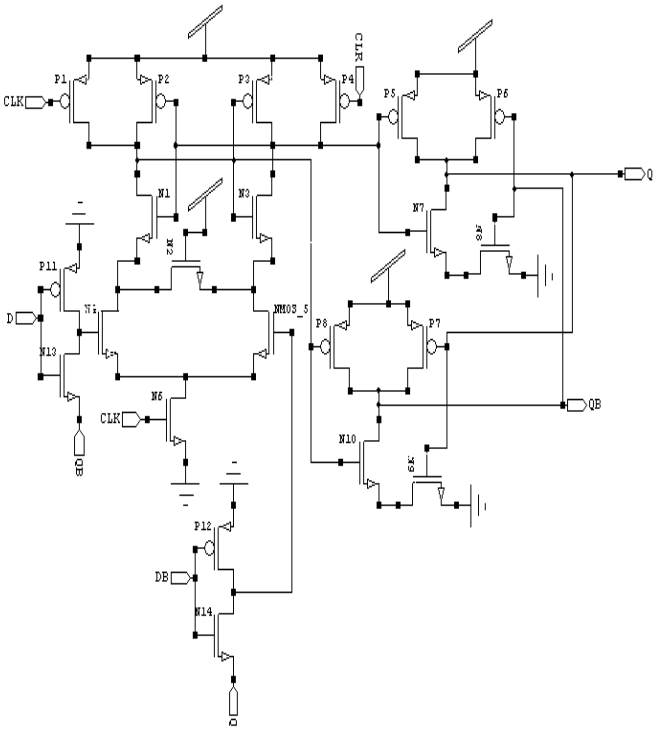

Figure 5: Data-Dependent SAFF with Latch implemented with GDI Technique

F. Conventional Dual Edge Triggered SAFF with CMOS-NAND Latch Design

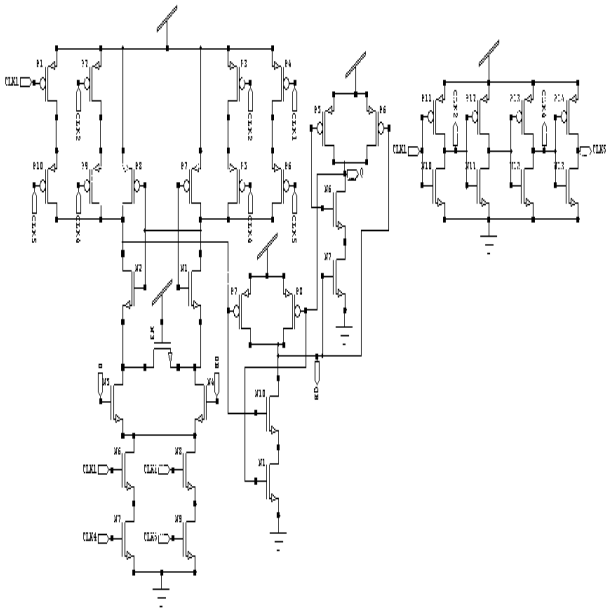

Figure 6: Dual Edge Triggered SAFF with CMOS-NAND Latch Design

G. Proposed Dual Edge Triggered SAFF with Latch implemented with GDI Technique

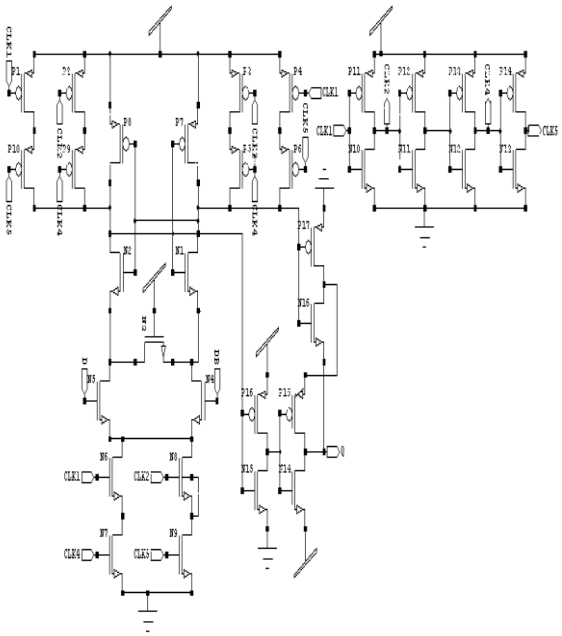

Figure 8: Dual Edge Triggered SAFF with implemented with GDI Technique

IV. SIMULATIONS AND ANALYSIS

A. Simulation Environment

All the circuits have been simulated using BSIM3V3 90nm technology on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns**.**

B. Simulation Comparison

In this section, proposed designs using low power technique is consuming low power and has high performance as compared with conventional SAFF topologies in terms of power, delay and temperature at varying supply voltages. All the circuits have been simulated with supply voltage ranging .8 V to 1.6 V. Following graphs are shown between Power Consumption Vs Operating Temperature, Delay Vs V_{DD}, Power Consumption Vs V_{DD} for different SAFF topologies. Power consumption variation with different operating range of temperatures is shown at V_{DD}=1V**.**Following tables represent the quantitative approach showing the variation of power consumption for all topologies given above over different operating range of temperature, $V_{DD,}$ and delay variation with V_{DD}. Finally, power-delay product comparison is shown in tabular form which reflects that our proposed circuit has least PDP and hence it is more efficient for low power VLSI designs.

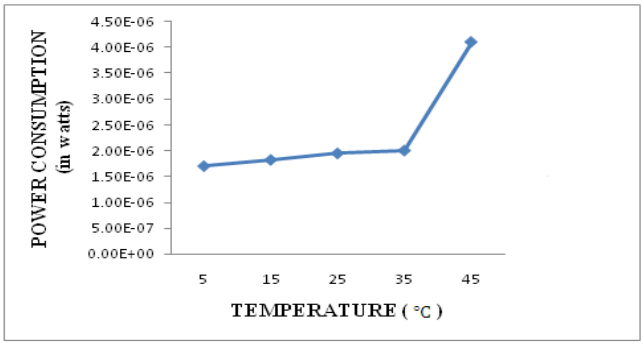

Figure 9: Power consumption variation of SAFF with CMOS-NAND latch over different operating range of temperatures at V_{DD}=1V

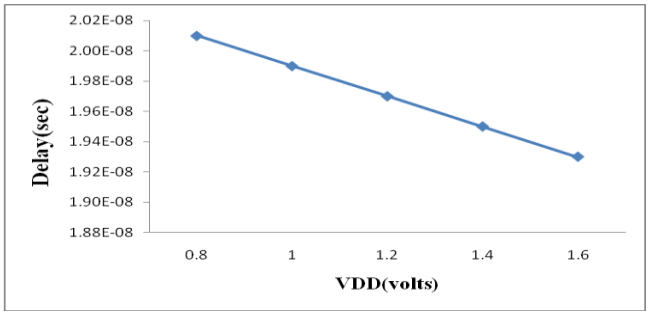

Figure 10: Delay Variation of SAFF with CMOS-NAND latch, SAFF with CMOS-Symmetric Latch & SAFF with Latch implemented with GDI technique over different operating range of V_{DD}

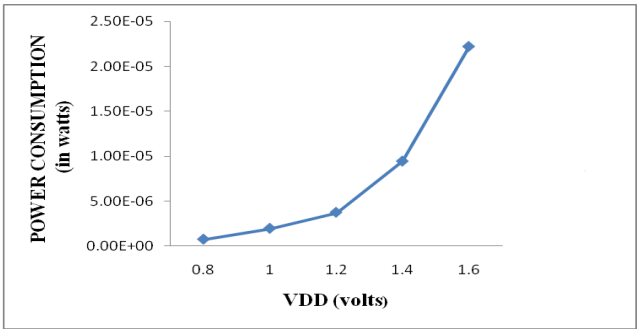

Figure 11: Power consumption variation of SAFF with CMOS-NAND latch over different operating range of V_{DD}

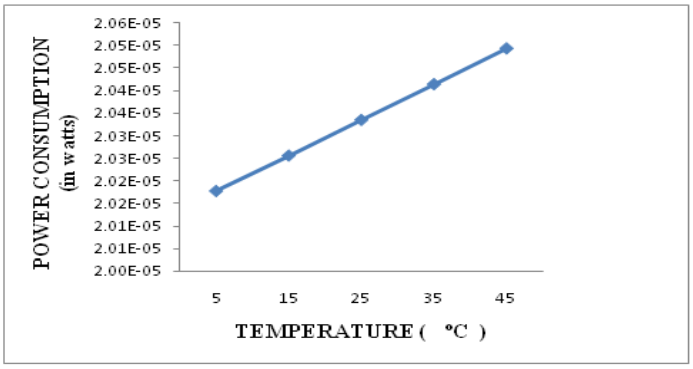

Figure 12: Power consumption variation of SAFF with CMOS-Symmetric Latch over different operating range of temperature at V_{DD}=1V

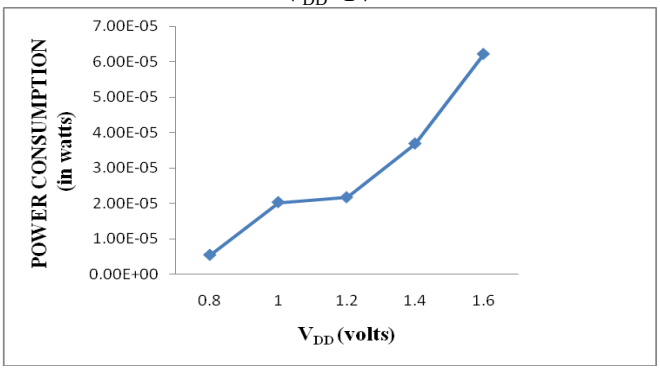

Figure 13: Power consumption variation of SAFF with CMOS-Symmetric Latch over different operating range of V_{DD}

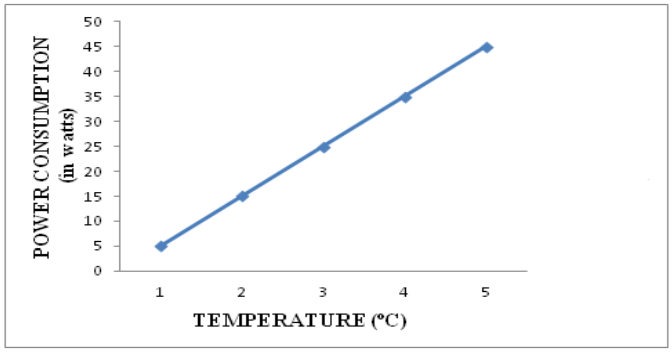

Figure 14: Power consumption variation of SAFF with Latch implemented with GDI technique over different operating range of temperature at V_{DD}=1V

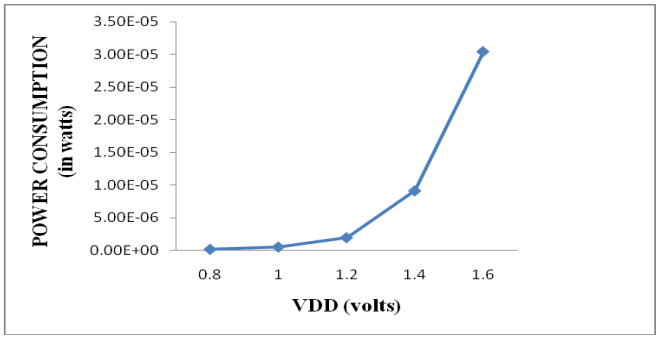

Figure 15: Power consumption variation of SAFF with Latch implemented with GDI technique over different operating range of V_{DD}

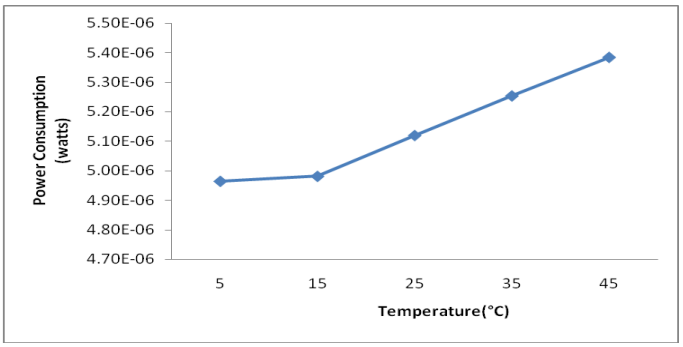

Figure 16: Power consumption variation of DD-SAFF with CMOS-NAND Latch over different operating range of temperature at V_{DD}=1V

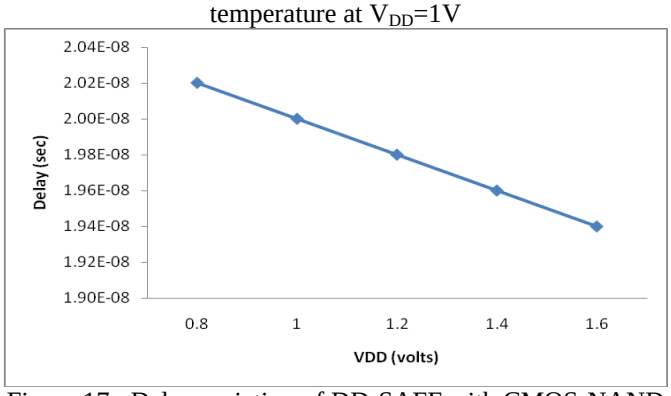

Figure 17: Delay variation of DD-SAFF with CMOS-NAND Latch & DD-SAFF with Latch implemented with GDI Technique over different operating range of V_{DD}

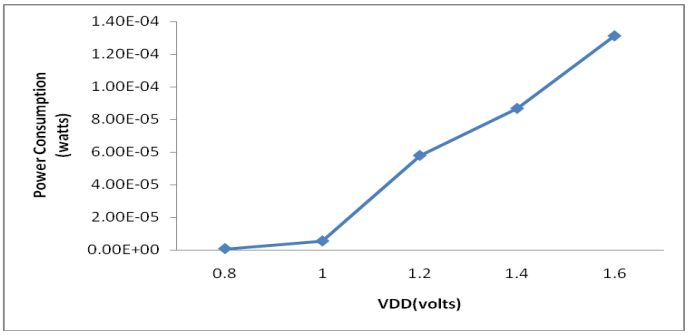

Figure 18: Power consumption variation of DD-SAFF with CMOS-NAND Latch over different operating range of V_{DD}

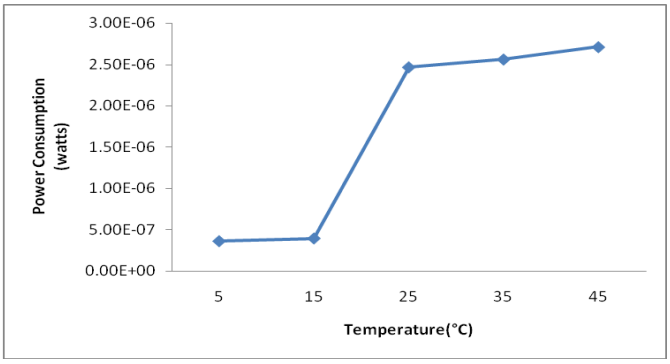

Figure 19: Power consumption variation of DD-SAFF with Latch implemented with GDI Technique over different operating range of temperature at V_{DD}=1V

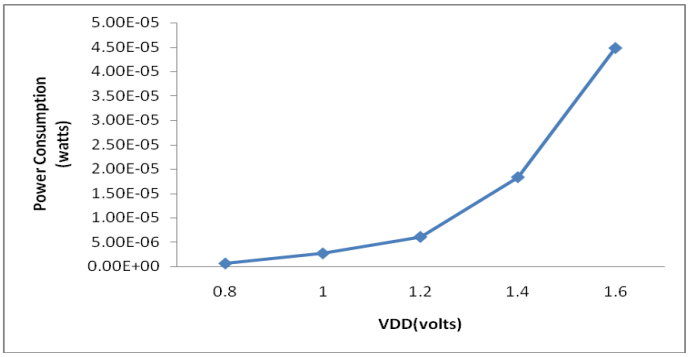

Figure 20: Power consumption variation of DD-SAFF with Latch implemented with GDI Technique over different operating range of V_{DD}

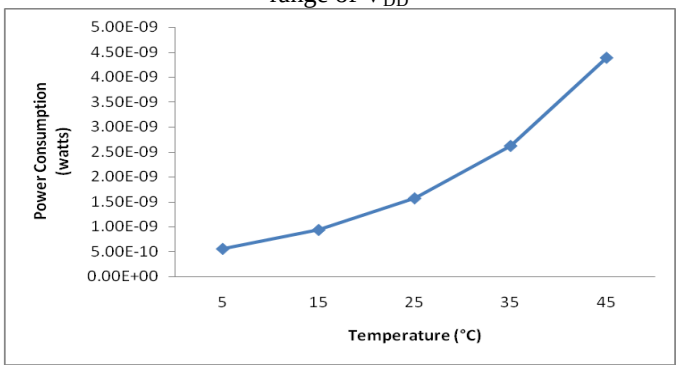

Figure 21: Power consumption variation of DET-SAFF with CMOS-NAND Latch over different operating range of temperature at V_{DD}=1V

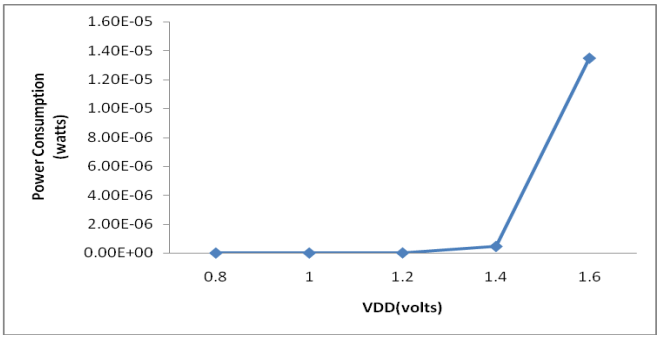

Figure 22: Power consumption variation of DET-SAFF with CMOS-NAND Latch over different operating range of V_{DD}

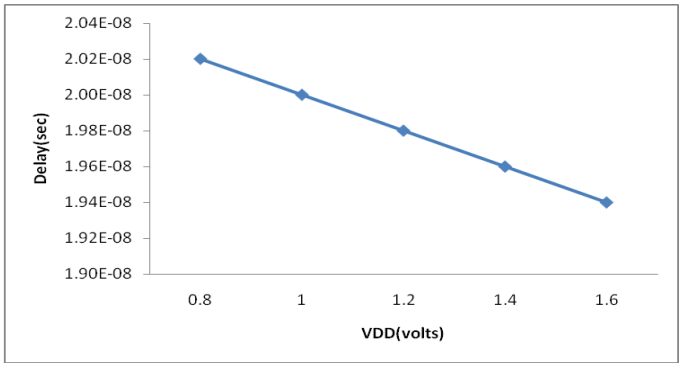

Figure 23: Delay variation of DET-SAFF with CMOS-NAND& DET-SAFF with Latch implemented with GDI Technique Latch over different operating range of V_{DD}

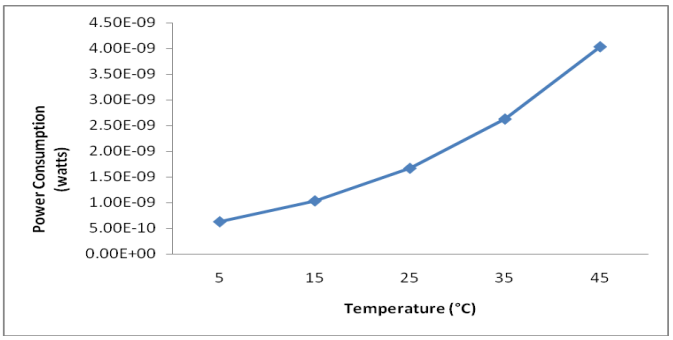

Figure 24: Power consumption variation of DET-SAFF with Latch using GDI Technique over different operating range of temperature at V_{DD}=1V

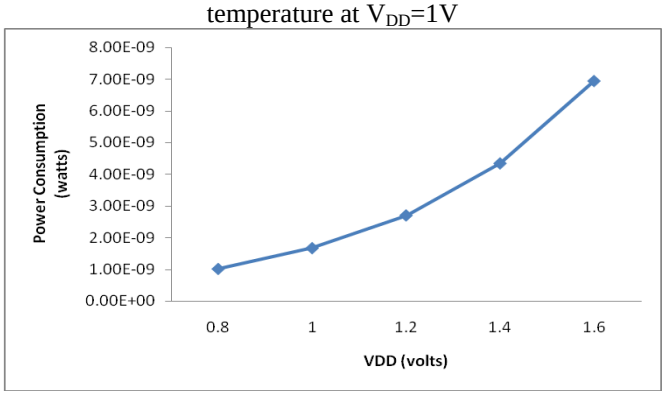

Figure 25: Power consumption variation of DET-SAFF with Latch using GDI Technique over different operating range of V_{DD}

Table I: Power consumption variation of SAFF with CMOS-NAND latch over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power consumption (watts)
5	1.703004e-006
15	1.825101e-006
25	1.951543e-006
35	2.005288e-006
45	4.109265e-006

Table II: Delay Variation of SAFF with CMOS-NAND latch, SAFF with CMOS-Symmetric Latch & SAFF with Latch using GDI technique over different operating range of V_{DD}

V_{DD} (volts)	Delay (sec)
.8	2.0100e-008
1	1.9900e-008
1.2	1.9700e-008
1.4	1.9500e-008
1.6	1.9300e-008

Table III : Power consumption variation of SAFF with CMOS-NAND latch over different operating range of V_{DD}

V_{DD} (volts)	Power consumption(watts)
.8	7.440419e-007
1	1.951543e-006
1.2	3.737754e-006
1.4	9.428828e-006
1.6	2.219050e-005

Table IV: Power consumption variation of SAFF with CMOS-Symmetric Latch over different operating range of temperature at V_{DD}=1V

Temperature(°C)	Power consumption (watts)
5	2.017781e-005
15	2.025651e-005
25	2.033558e-005
35	2.041484e-005
45	2.049415e-005

Table V: Power consumption variation of SAFF with CMOS-Symmetric Latch over different operating range of V_{DD}

V_{DD} (volts)	Power consumption (watts)
.8	5.448861e-006
1	2.033558e-005
1.2	2.172743e-005
1.4	3.689852e-005
1.6	6.221658e-005

Table VI: Power consumption variation of SAFF with Latch implemented with GDI technique over different operating range of temperature at V_{DD}=1V

Temperature(°C)	Power consumption (watts)
5	4.965438e-007
15	5.258306e-007
25	5.685602e-007
35	6.184802e-007
45	6.823192e-007

Table VII: Power consumption variation of SAFF with Latch implemented with GDI technique over different operating range of V_{DD}

V_{DD} (volts)	Power consumption (watts)
.8	2.222364e-007
1	5.685602e-007
1.2	2.008319e-006
1.4	9.164612e-006
1.6	3.044173e-005

Table VIII: Power consumption variation of DD-SAFF with CMOS-NAND Latch over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power consumption (watts)
5	4.964329e-006
15	4.981085e-006
25	5.119591e-006
35	5.253684e-006
45	5.384218e-006

Table IX: Delay variation of DD-SAFF with CMOS-NAND Latch & DD-SAFF with Latch implemented with GDI Technique over different operating range of V_{DD}

V_{DD}(volts)	Delay(sec)
.8	2.0200e-008
1	2.0000e-008
1.2	1.9800e-008
1.4	1.9600e-008
1.6	1.9400e-008

Table X: Power consumption variation of DD-SAFF with CMOS-NAND Latch over different operating range of V_{DD}

V_{DD} (volts)	Power consumption (watts)
.8	7.032634e-007
1	5.384218e-006
1.2	5.784314e-005
1.4	8.666246e-005
1.6	1.311404e-004

Table XI: Power consumption variation of DD-SAFF with Latch implemented with GDI Technique over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power consumption (watts)
5	3.615623e-006
15	3.947903e-006
25	2.467942e-006
35	2.562132e-006
45	2.711823e-006

Table XII: Power consumption variation of DD-SAFF with Latch implemented with GDI Technique over different operating range of V_{DD}

V_{DD} (volts)	Power consumption (watts)
.8	6.390936e-007
1	2.711823e-006
1.2	6.082062e-006
1.4	1.831317e-005
1.6	4.477793e-005

Table XIII: Power consumption variation of DET-SAFF with Latch implemented with GDI technique over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power Consumption (watts)
5	5.513358e-010
15	9.325290e-010
25	1.566601e-009
35	2.619674e-009
45	4.388632e-009

Table XIV: Delay variation of DET-SAFF with Latch using GDI technique over different operating range of V_{DD}

V_{DD}(volts)	Delay(sec)
.8	2.0200e-008
1	2.0000e-008
1.2	1.9800e-008
1.4	1.9600e-008
1.6	1.9400e-008

Table XV: Power consumption variation of DET-SAFF with Latch implemented with GDI technique over different operating range of V_{DD}

V_{DD}(volts)	Power Consumption (watts)
.8	8.775947e-010
1	9.325290e-010
1.2	1.046875e-008
1.4	4.564270e-007
1.6	1.346978e-005

Table XVI: Power consumption variation of DET-SAFF with CMOS-NAND Latch over different operating range of temperature at V_{DD}=1V

Temperature(°C)	Power Consumption (watts)
5	6.269663e-010
15	1.032274e-009
25	1.666052e-009
35	2.624420e-009
45	4.030583e-009

Table XVII: Power consumption variation of DET-SAFF with CMOS-NAND Latch over different operating range of V_{DD}

V_{DD}(volts)	Power Consumption (watts)
.8	1.009834e-009
1	1.032274e-009
1.2	2.701417e-009
1.4	4.345485e-009
1.6	6.947572e-009

Table XVIII: PDP comparison of all above mentioned configurations

SAFF latch configurations	VDD(volts)	PDP(volts-sec)	No. of transistors
NAND - CMOS	1	$3.388*10^{-14}$	18
CMOS-Symmetric	1	$2.039*10^{-13}$	18
SAFF with GDI Technique	1	$9.870*10^{-15}$	16
DD-SAFF	1	$1.076*10^{-13}$	30
DD-SAFF with GDI Technique	1	$5.422*10^{-14}$	22
DET-SAFF	1	$2.064*10^{-17}$	35
DET-SAFF with GDI Technique	1	$1.865*10^{-17}$	33

V. CONCLUSION

This paper proposes three new configurations of SAFF with latch using GDI Technique, which resulted in better performance in terms of power consumption, number of transistors and, temperature sustainability. Above all the configurations ,double edge triggered SAFF have least power consumption due to low frequency of output .The differential input signal nature of the flip-flop makes it compatible with the logic utilizing reduced signal swing.GDI Technique contributed in improved PDP of new design also. Hence, the proposed design can be used for other complex designs. All the simulations are carried out at Tanner EDA tool at BSIM3v3 90nm technology.

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