Characterization of High-K Gate Dielectrics using MOS Capacitors

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Abstract- In today's world, life without electronics is unthinkable. It has been studied that for electronic devices to provide better efficiency and reliability in terms of speed, power-loss and cost, the fundamental component of each Integrated Circuit (IC) chip, namely the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) needs to be reduced or 'scaled' down in size. Device scaling has produced remarkable results until further scaling beyond the 22-nm technology node has resulted in undesirable leakage currents in the MOS device by means of direct tunneling of electrons through the gate dielectric. Due to this leakage, the battery of any electronic gadget can be drained in minutes and the excessive heat produced by all the MOSFETs will reduce the efficiency. In order to solve this problem, materials like the oxides of hafnium and zirconium with a higher value of dielectric constant K are being used to replace the previously used silicon dioxide, so as to facilitate more device scaling with negligible leakages.

This paper presents the characterization of High-K dielectric materials by three depositional processes: As-Deposited, DSDS and DADA on basic two-terminal MOS Capacitors (MOSCAPs) located on silicon wafers. The Equivalent Oxide Thickness (EOT), trapped oxide charge, presence of defects within the High-K materials and gate leakage currents were investigated and As-Deposited sample was found to be superior as compared to the other two types of processing.

Index Terms- EOT, Gate tunneling, High-K Dielectrics, Leakage Current, MOS Capacitor.

I. Introduction and Basic Theory

Microelectronics is much needed for better lifestyle standards and hence it must be developed for better performance of electronic devices in future. The fundamental component of any Integrated Circuit (IC) chip is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It has been studied that with the reduction of the device size (mainly by 'scaling' down the size of the MOSFETs), its efficiency increases. With the scaling of the MOSFETs, more number of transistors can now be accommodated within the same IC and this has resulted in the dramatic decrease in the cost of electronic devices on the whole.

Device scaling has other benefits too. With smaller sized transistors, the size of the interconnects have got smaller and this has reduced the path length for electrons to travel, thereby decreasing the resistance offered by the path, circuit delays, power consumption and increasing the speed of device operation. With smaller devices, the gate oxide thickness is also small, so from the relation:

$$C = K\varepsilon_0 A/d$$

[where, C= capacitance, K= relative permittivity of the dielectric, ε_0= permittivity of free space (8.854×10^{-12} F/m), A= area & d= oxide thickness] the capacitance C is large and hence the device current is also large. This is essential for maximizing circuit speed.

However, the disadvantage lies in the fact that with continuous scaling of the device channel length and the thinning of the gate oxide (SiO_2) beyond 20 Å, undesirable gate tunneling current and subthreshold leakage currents are observed. The electric field in the MOS device can be large enough to result to a dielectric breakdown at high temperatures. At 1.2 nm device channel, the leakage through SiO_2 has been found to be as high as 10^3 A/cm^2. If an IC chip contains a total of 1mm^2 area of the thin dielectric SiO_2, then the chip oxide leakage current is 10 A and this large leakage can discharge the battery of any cellular phone in minutes. This leakage current is a therefore a big challenge to continued scaling. The figure below represents the increase in the leakage current with the reduction of the oxide thickness.

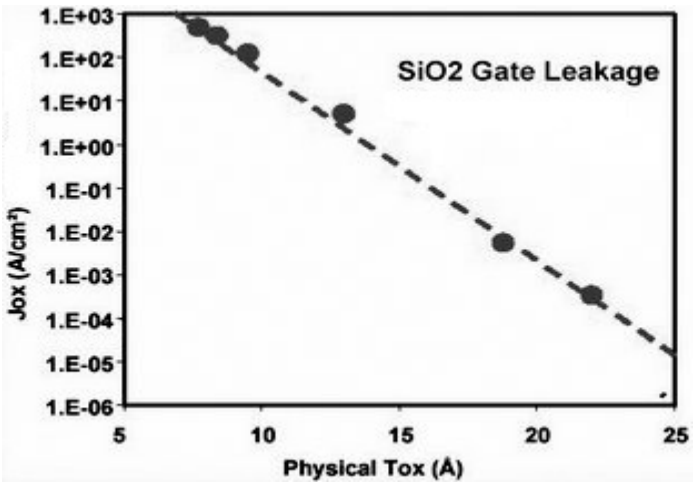

Figure 1: A plot of the Leakage Current Density at the insulating oxide (J_{ox}) against the Thickness of the Gate Oxide (t_{ox})

As a result of this, it becomes necessary to find an alternative gate dielectric with higher values of the relative permittivities 'K' (around 25-30) which will be suitable for reducing the leakage (K of SiO_2 is only 3.9) and can thus afford larger physical thickness to minimize leakage while maintaining similar

capacitance values. The equivalent oxide thickness (EOT) of a high-K gate dielectric with relative permittivity K and physical thickness t_{phy} can be written as:

$$EOT = \frac{K_{SiO2}.t_{phy}}{K}$$

[where K_{SiO2} is the relative permittivity of SiO_2]. For a particular EOT using a high-K gate dielectric with a t_{phy} larger by a factor K/K_{SiO2} results in reduced power loss. The following figure is a schematic of easy tunneling through the thin SiO_2 layer and difficult tunneling through the thicker layer of the High-K material.

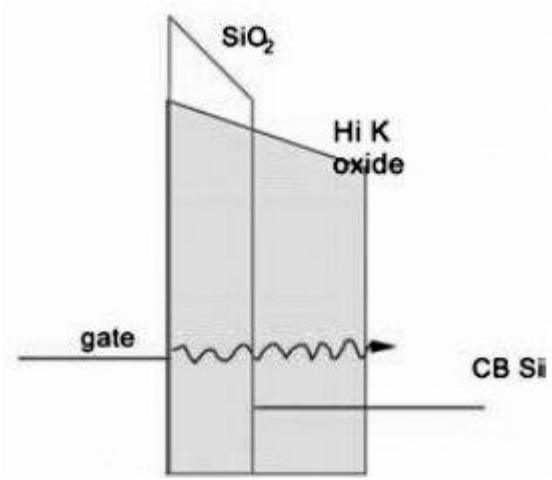

Figure 2: Tunneling, which is easy through the thin SiO_2 but difficult through the High-K dielectric

II. REQUISITES FOR GOOD HIGH-K MATERIALS

1) It must have a high enough *K*-value of around 25-30.
2) The oxide is in direct contact with the Si substrate so it must be thermodynamically stable with it, i.e. it should not react with silicon to form silicates.
3) It must be kinetically stable i.e. it should not dissociate with processing to 1000 ˚C for 5 seconds.
4) It must form a good electrical bonding interface with Si.
5) It must have a large bandgap to avoid tunneling.
6) It must have few defects (sites of excess or deficit of oxygen or impurities) in its structure.
7) Examples of standard High-K oxides are: HfO_2, ZrO_2, HfZrO and so on.

III. METHODS AND MATERIALS

A. Basic Element of Deposition

In this experiment, HfZrO was used as the High-K gate dielectric material which had a K-value of 15 at room temperature and 35 at high temperatures. This material was deposited by three types of depositional processes on MOS Capacitors placed on Si wafers, as High-K materials cannot be directly placed on Si due to lattice mismatch.

A MOS Capacitor (MOSCAP) is a simplified form of a MOSFET having only two terminals, namely, the gate and the substrate and has been used in this study for simplicity and better results. The following figure shows a MOSCAP deposited with a High-k layer.

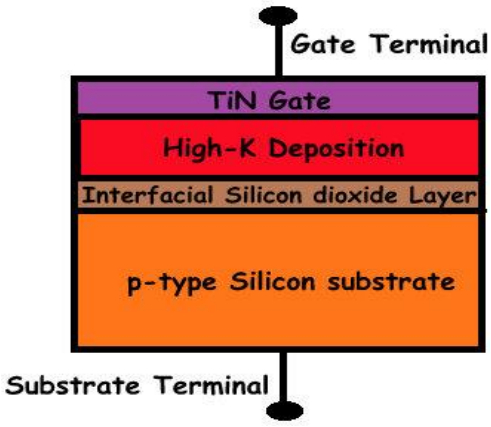

Figure 3: Basic structure of a 2-terminal MOSCAP with a High-K deposited layer

B. Regions of Operation of a MOSCAP

A MOSFET or a MOSCAP has three regions of operation: Accumulation, Depletion and Inversion.

Considering a MOS Capacitor having a p-type doped substrate, if a negative gate voltage V_G is applied (lesser than the flatband voltage V_{FB}), a negative charge is effectively deposited on the metal. In response, an equal net positive charge is observed to accumulate on the surface of the semiconductor. Since the formation of the charge-cluster is of the same type as that of the majority carriers in the substrate, carriers are said to be "accumulated" at the surface. Hence this region is known as the Accumulation Region.

Now if the previously applied negative gate voltage is decreased and a slight positive voltage is applied, i.e. greater than flatband voltage but lesser than the threshold voltage V_T, a positive charge gets deposited on the metal. This attracts a corresponding net negative charge at the surface of the semiconductor. Such a negative charge in p-type material arises from the depletion of holes from the region near the surface, leaving behind uncompensated ionized acceptors. This region is known as the Depletion Region.

Next, if the positive gate voltage is continued to be increased (greater than threshold voltage), the majority holes in the substrate is repelled downward direction, while minority electrons from the p-type substrate get attracted towards the surface. This forms an "inversion layer" at the surface, inverting the conductivity type. This is known as the Inversion Region.

Flatband Voltage (V_{FB}): The voltage at which there is no electrical charge in the semiconductor and therefore, no voltage drop across it; in band diagram the energy bands of the semiconductor are horizontal (flat).

Threshold Voltage (V_T): The minimum voltage in which the channel formation initializes.

C. Three types of Depositional Processes

The three types of depositional processes used are:
1) DADA (Deposition-Anneal-Deposition-Anneal) in which the silicon wafer samples were subjected to the deposition of the dielectric followed by a thermal annealing in a cyclical manner until 44 such cycles were obtained for a given test wafer.

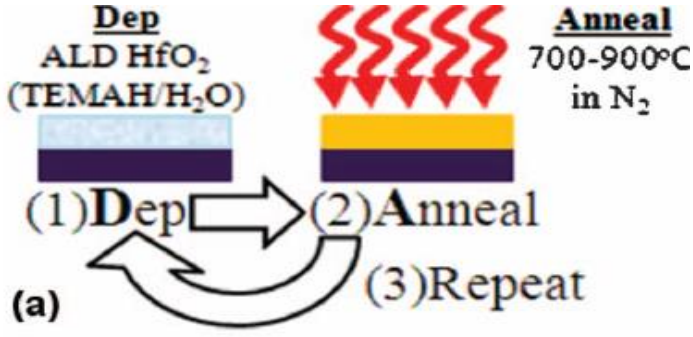

Figure 4: The DADA Process

2) DSDS (Deposition-Plasma-Deposition-Plasma) in which the samples were subjected to a similar cyclical process as that of DADA with the deposition of the dielectric and Ar plasma.
3) As-Dep (As-Deposited) in which the dielectric for the samples was deposited without any other intermediate step.

D. Equipments & Components

1) Semi-automatic probe station (micromanipulator)
2) Precision LCR Meter (4284A) for Capacitance-Voltage measurements
3) Software used: Cascade Microtech, LabVIEW simulator
4) Wafers containing MOSCAPs, manufactured by TEL

E. The Experimental Method

The experiment was performed in the following few steps:
Proper connections with the LCR meter, probe station and the computers were carefully made.
Initially, a silicon wafer is cut into a sector and different die locations on it are seen. An image of a wafer can be given as follows:

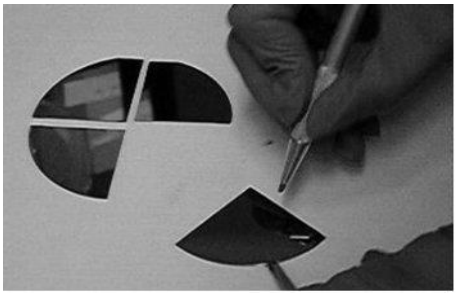

Figure 5: Wafers being cut out into smaller pieces

The required wafer was carefully placed on the chuck of the Semi-automatic probe station and the vacuum was switched on.
By operating icons on the Cascade Microtech software, the chuck was taken to the center of the probe-station and by proper focusing, the MOSCAP Layout was viewed on the eyepiece and the live video. The probe was carefully touched on a particular MOSCAP till it slid a bit.
The light was turned off, the simulation was run on the LabVIEW software via the LCR Meter and the necessary data and C-V graphs were obtained .
Within a particular layout, there were MOSCAPs of different areas ranging from 10 square microns to 100 square microns. C-V readings for a number of areas were obtained from the simulator that gave the nature of the the capacitance with respect to the applied voltage for different regions of operations of the MOSCAPs.

F. The Experimental Setup

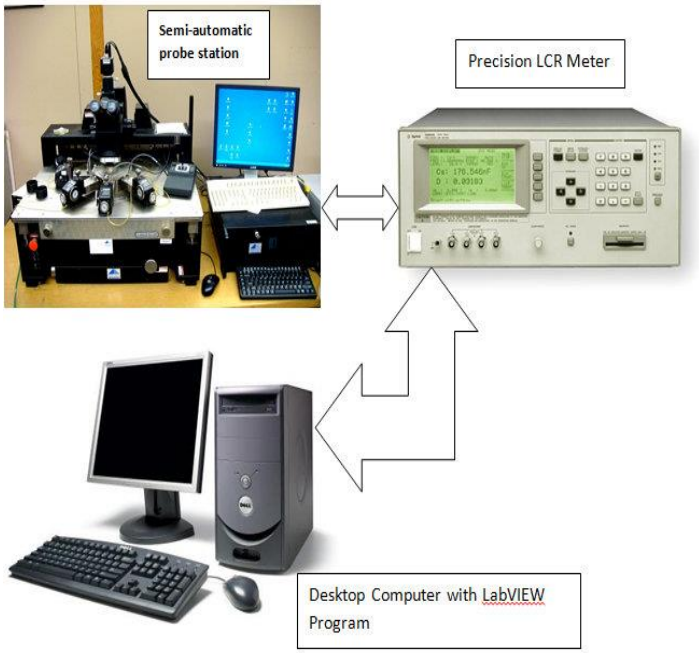

Figure 6: The Experimental Apparatus

IV. RESULTS

The following curves were obtained from the experiment.

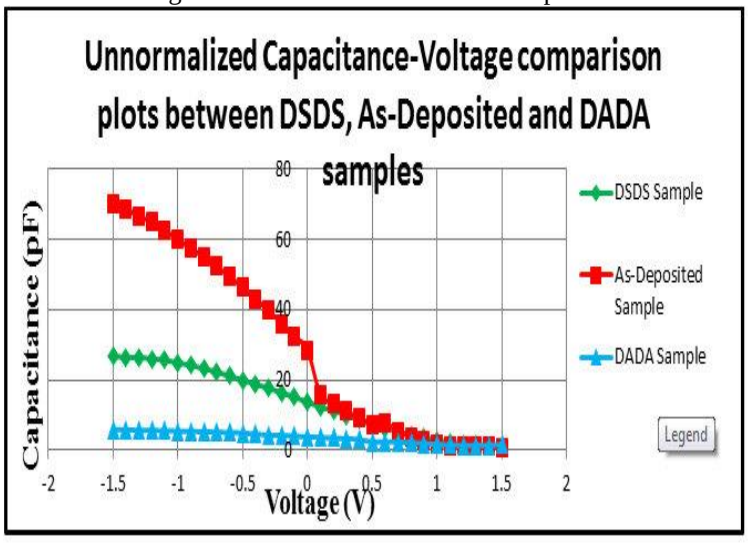

Figure 7: C-V curves for the 3 depositional processes

Table I: The Equivalent Oxide Thickness (EOT) Table for the 3 depositional processes

As-Dep	DSDS	DADA
4.9 nm	12.92 nm	58.37 nm

From the table, it can be seen that the EOT is the least for the As-Deposited Sample and hence, it gives the best results out of the other two processes.

The trapped oxide charge within the gate dielectric was also studied and a plot was obtained as follows.

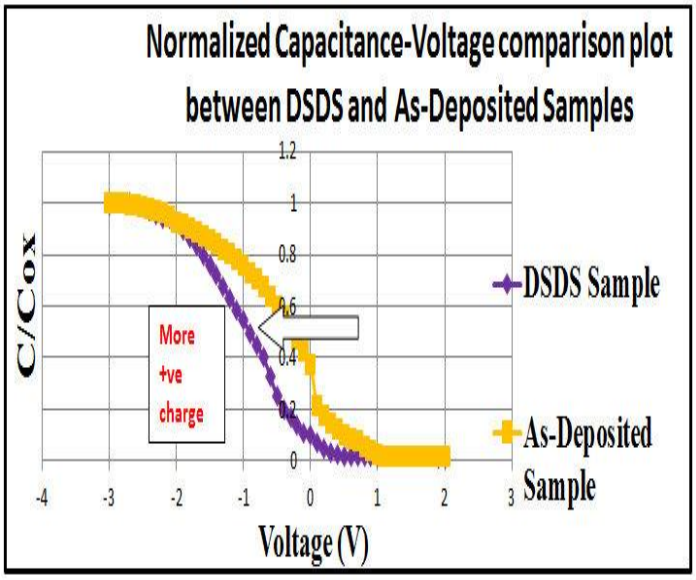

Figure 8: C-V curves depicting more trapped positive oxide charge accumulation for DSDS sample as compared to As-Deposited

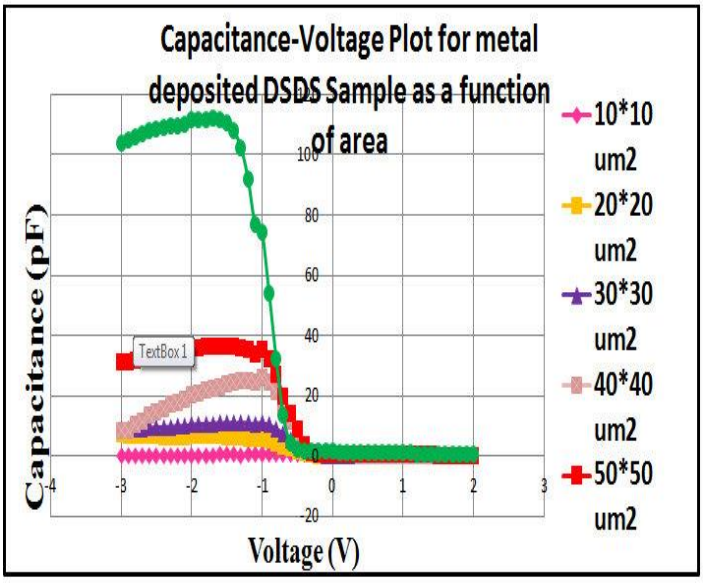

Figure 9: C-V curves showing the different values for MOSCAPs of different area ranging from 10 to 50 square microns

Table II: The Equivalent Oxide Thickness (EOT) Table for the MOSCAPs of different area

Area (in μm^2)	Maximum Capacitance (in pF)	Obtained EOT (in nm)
10 x10	0.065	6.499
20 x 20	7.072	1.95
30 x 30	8.759	3.55
40 x 40	10.43	5.297
50 x 50	31.331	2.755
100 x 100	103.85	3.32

V. CONCLUSION & DISCUSSIONS

Characterization of High-K gate dielectrics was done and deposited in three different methods.

From the MOS capacitor characteristics it was observed that As-Deposited High-K is superior as compared to DSDS or DADA samples.

The DSDS and DADA devices seem to have more positive oxide charge in the dielectric as compared to As-Deposited device.

Hence from the given test wafers, it can be concluded that the As-Deposited sample is the most suitable depositional process of High-K materials on MOSCAPs and hence, can also be applied on MOSFETs for good results. In this way, a High-K will be deposited efficiently (as its direct deposition on Si causes mismatch of the different crystal lattices) by this process and in doing so, further device scaling will also be possible without adverse leakage effects.

ACKNOWLEDGMENT

I would like to thank my professor, Dr. Durga Misra for his continuous support, encouragement and guidance at New Jersey Institute of Technology, Newark, USA and to my college, Heritage Institute of Technology, Kolkata who has given me an opportunity to work successfully in the United States.

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