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Error Tolerant Adder

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Abstract- The addition of two binary numbers is the most fundamental and widely used arithmetic operation. This operation is used in microprocessors, digital signal processors, data processing application specific integrated circuits and many more. There are many adders designed till now. ETA is one such efficient adder which speeds up binary addition. ETA is the Error Tolerant Adder which consumes less power and delay. Design of ETA is done using backend tool under real time simulation conditions. This paper compares the performance of the ETA in terms of accuracy, delay and power consumption with that of conventional adders.

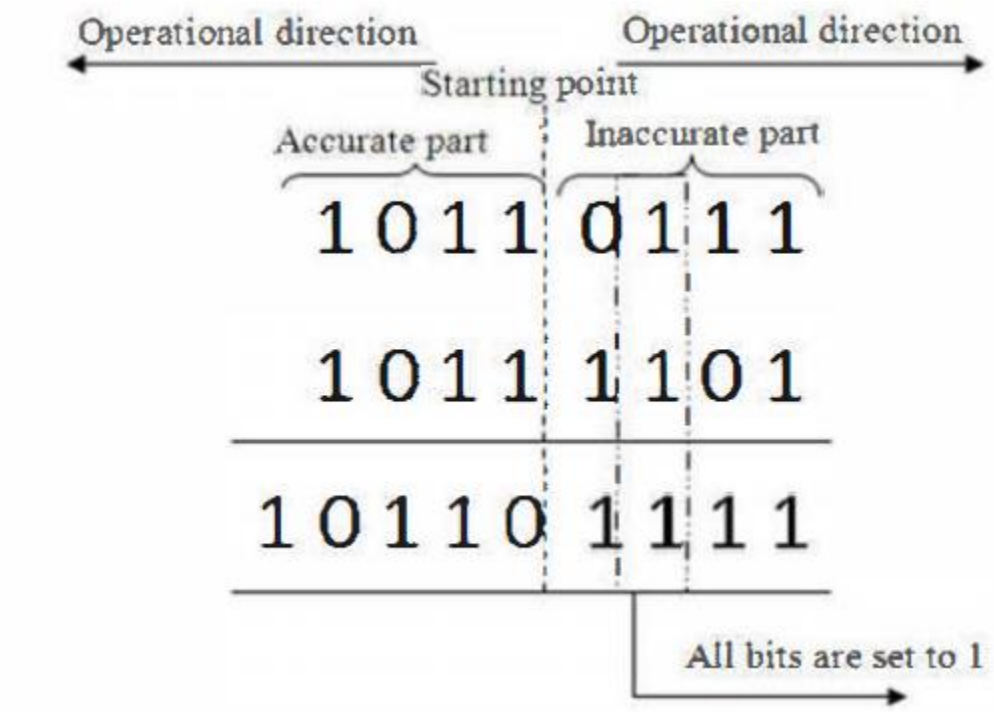
Index Terms- Error Tolerant Adder (ETA), Accuracy, Power dissipation, Speed, Power Delay Product

I. INTRODUCTION

Arithmetic operations are performed frequently in microelectronics. Addition is the most basic operation from which other operations like subtraction, division and multiplication can be derived. So adders are considered as the most important part. Power is the most significant resource that should be saved while designing an adder. Speed also plays an important role in the performance of adder so it should be on the higher side. Designing a low power and high speed adder is the goal of many industries. Many different types of fast adders have been developed so far, such as the, carry-select adder (CSL) [6], carry-skip adder (CSK) [5] and carry-look-ahead adder (CLA) [7]. Also, there are many low-power adder design techniques that have been proposed [19]. However, there are always trade-offs between speed and power. In order to achieve that a special kind of adder called the Error Tolerant Adder (ETA) has come into the picture which sacrifices the accuracy for speed and low power dissipation. The power delay product which is the average of power consumed and worst case delay is improved by more than 65%. By reducing the power consumed, the battery life of any portable device can also be improved.

II. MATERIALS AND METHODS

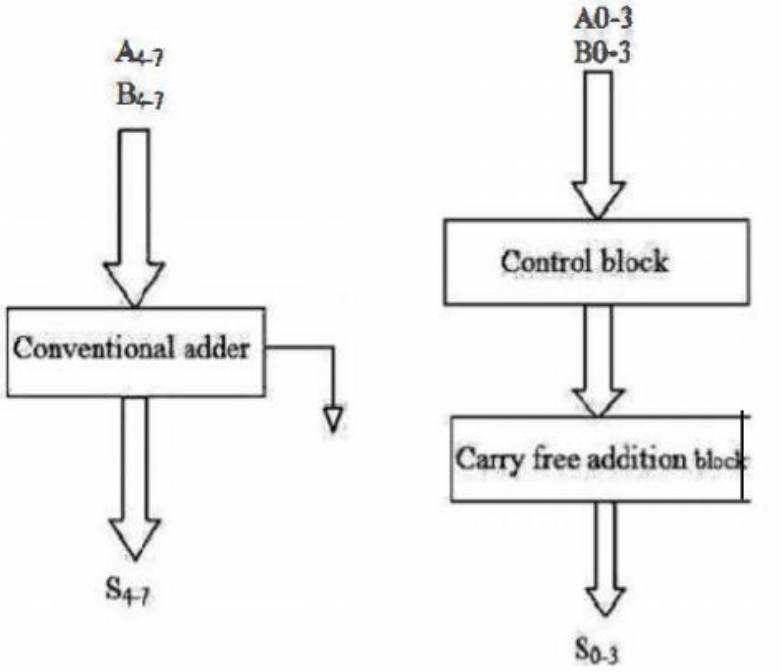
There is a huge improvement in the power and speed when we use an ETA. For increasing the speed and decreasing the power dissipation, we use the logic that in an adder circuit the delay appears mainly because of the carry propagation and also there is a lot of power dissipation. So we try to eliminate this carry propagation by dividing the addition of two binary numbers into two parts namely accurate part and inaccurate part as shown below. The 4 MSB bits of both the numbers are the accurate part and the 4 LSB bits are the inaccurate part. In the accurate part the addition is performed in a conventional way from right to left starting from the demarcation line because the higher order bits play a greater role in the accuracy. In the inaccurate part, the addition is performed from left to right strarting from the demarcation line. When two 0s are there or a 0 and a 1 is there, the addition proceeds conventionally. As soon as two 1s in the input bits are seen, the checking stops and from this point onwards all the bits are set to 1 as shown below. This method is adopted in order to eliminate the time required for carry propagation and also to reduce the power consumption.



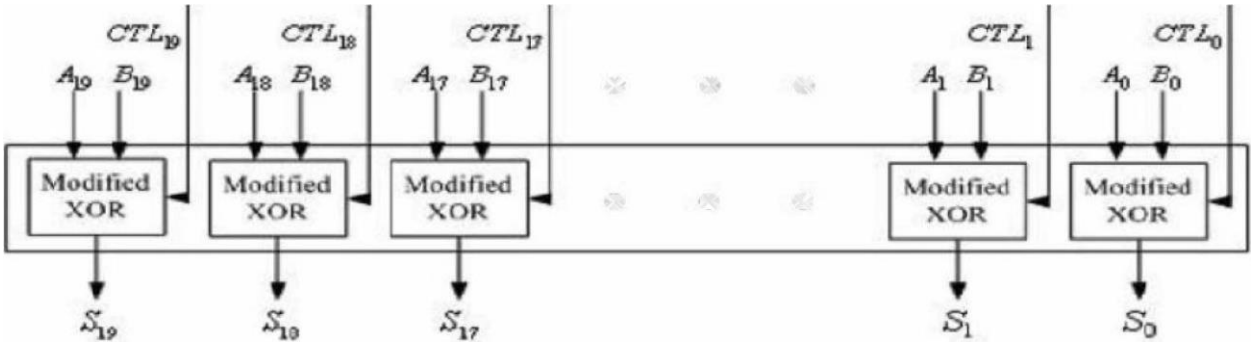
III. ARCHITECTURE

The accurate part consists of a conventional adder which performs normal addition. The inaccurate part consists of two parts namely the control block and carry free addition block. Bit B0 serves as the control bit for both accurate and inaccurate parts. If B0 is 1 adder performs the normal addition and if B0 is zero, the line from supply to ground is cut off and hence reducing the power dissipation.

A 10T conventional full adder is used in the accurate part. It is the inaccurate part that decides the speed, accuracy and the power consumption of the adder. The carry free addition block has 4 modified XOR gates to give sum bits for LSBs. The inaccurate part has a CTL which controls the output of carry free addition block. When both or one of the inputs is zero, CTL is off and as soon as both the inputs are '1' it goes to logic '1'. Hence after this at least one of the inputs is always '1' so we get '1' as the output for any input that comes after this.

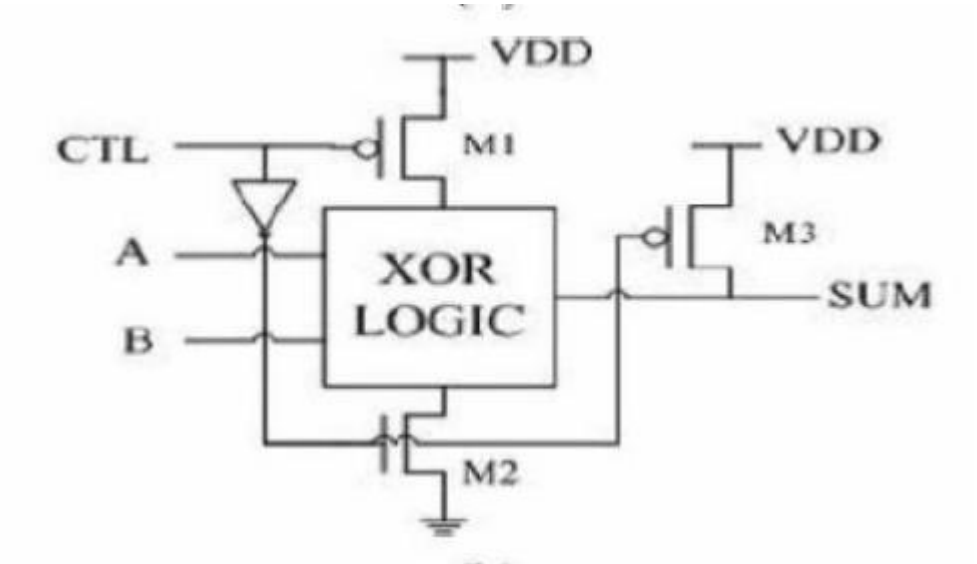


Accurate Part Inaccurate Part



Block diagram of carry free addition of ETA

Modified XOR Gate



Modified XOR with control

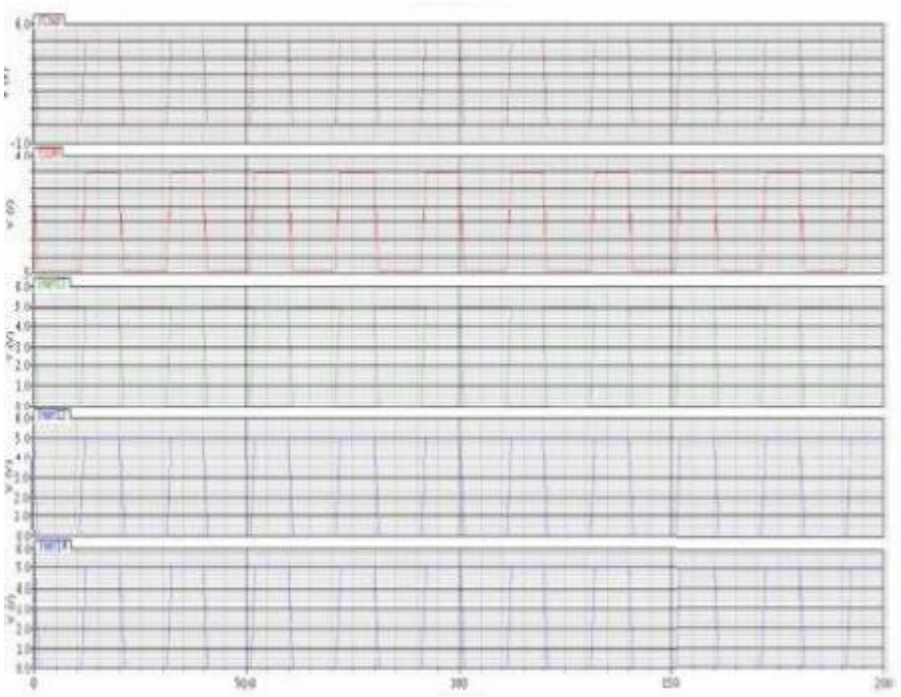
Error Tolerant Adder is designed for the addition of two 8 bit inputs using the above logic with backend tools that use real time conditions.

IV. RESULT

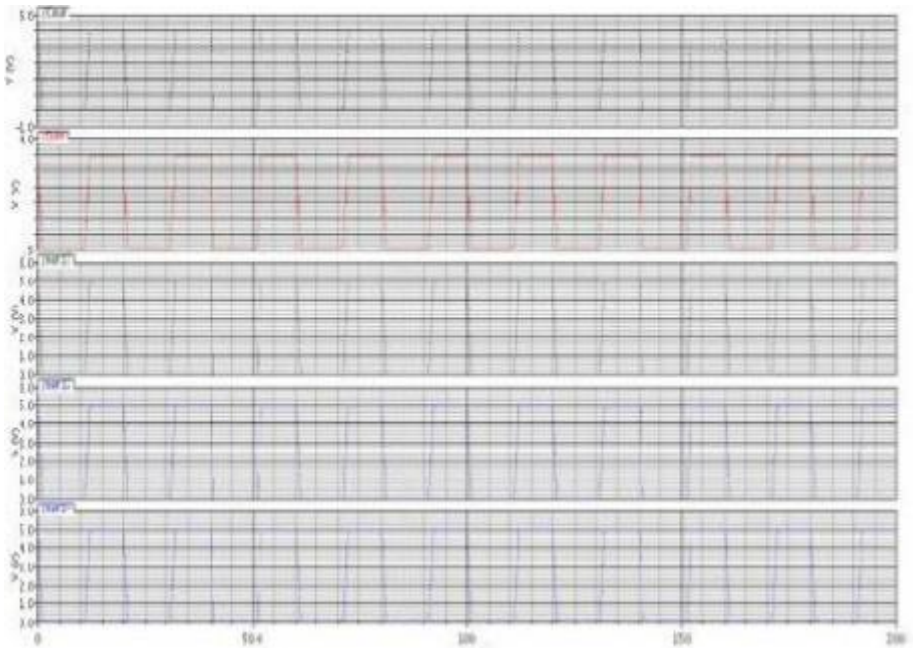
The characteristics such as power consumption, power delay product and speed are studied and compared with other adders and it is observed that all the parameters are considerably improved while using an Error Tolerant Adder.

Type of Adder	Power (mW)	Delay (ns)	PDP (pJ)	PDP saving (%)	Transistor Count
RCA	0.22	4.04	0.89	66.29	896
CSK	0.46	2.90	1.33	77.44	1728
CSL	0.60	3.06	1.84	83.70	2176
CLA	0.51	2.37	1.21	75.21	2208
ETA	0.13	1.81	0.28	N.A.	996

Table comparing the characteristics of different adders



Output of the accurate part of the adder



Output of the XOR Gate

V. Conclusion

From the above results following conclusions can be made:

- The Error Tolerant Adder has lower power consumption than any other adder.
- The delay is the least in ETA because of the elimination of carry propagation.
- The power delay product is also the least.

With the advent of portable gadgets, it is the need of the hour to design devices of smaller size, low power consumption and high speed. ETA is the answer to this. With high speed and low power consumption, the battery life of a device can be prolonged extensively.

This logic has the potential to be used in the multipliers as well in the future.

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