# Power Optimization Techniques in VLSI Backend Design

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DOI: 10.29322/IJSRP.9.09.2019.p9334
http://dx.doi.org/10.29322/IJSRP.9.09.2019.p9334

**Abstract:** Power is a key parameter in VLSI design. In this age of portable computers, battery life is very important. Power convergence is an important factor from a designer perspective. All applications demand chip level power reduction. Power and timing convergence goes hand in hand. One cannot be compromised for other, here comes the challenge for a designer. This paper focuses on understanding of various power sources and solutions for power reduction in a physical design. Enhanced quality rules are proposed for the high quality performance of the design. The enhanced power reduction techniques for both Data path power reduction and Clock path power reduction are mainly focused.

**Keywords**: *Power optimization, Physical design, Multi-bit, High AF net,Dynamic power*

## I. INTRODUCTION

VLSI Technology has advanced a lot, the performance is very high but at the same time the design is becoming more challenging. In the VLSI design flow each stage is challenging right from the net list generation to layout model. Lot of parameters have to be considered in each stage such as speed, power, and area. Power is one of the important parameter in design. In VLSI design we can see four different type of power dissipation. Firstly Dynamic power dissipation, due to switching activity of the transistor, Static power dissipation due to leakage currents, Short-circuit power dissipation due time short circuit between NMOS and PMOS, Leakage power dissipation.

In this paper we focus on reducing the dynamic power dissipation. Dynamic power dissipation is further classified into switched power dissipation and glitch power dissipation .Based on the activity of the cell, output load and supply voltage with which circuit operates .Power dissipation is due to the charging and discharging of output load capacitance. We use three different techniques to reduce the dynamic power dissipation without much compromise on the timing of the design.

**Power calculation:** In a CMOS technology the total power consumption will due to dynamic power consumption plus the static power consumption. Power equation can be written as the

$$P_{total} = P_{dyn} + P_{leak} \quad (1)$$

The static power is because of the leakage current of the device while the dynamic power is due to the switching activity of the transistor. Dynamic power depends mainly on clock frequency with which circuit works and the supply voltage also.

In this paper our main focus will be on the dynamic power loss of the circuit .Dynamic power of a cell is result of both initial power and switching power .The dynamic power equation can be written as

$$P_{dynamic} = P_{initial} + P_{switching} \quad (2)$$

$$P_{initial} = 1/2 \, ( E_{rise} + E_{fall} ) \, \alpha \quad (3)$$

Where E rise and E fall are rise and fall energy levels and the alpha is the toggle rate, is the number of times signal switch from zero to one per time unit.

$$P_{switching} = 1/2 \, CV^2 \, \alpha \quad (4)$$

Where ‘C’ is wire capacitance and the ‘V’ is supply voltage ,alpha is the toggle rate.

For the inter connects there will be no initial power, there is only switching power which is given by equation (4).From the same equation it is clear that power can be reduced by either reducing the frequency of the design or the supply voltage but for a modern digital design speed is the most important concern so the main parameter to gain power is the capacitance. Since we are talking with respect to the dynamic power we call it as dynamic capacitance.

In physical design we can reduce the dynamic capacitance using multiple techniques. Keeping in mind the other important

parameters like speed area we propose three different techniques to reduce the dynamic capacitance there by reducing the dynamic power.

**Power trends in physical design stage**: In the advanced technology nodes, the power consumption because of static power is about 10% and internal circuit power is about 20%. Dynamic power contributes almost 80% of the circuit total power this is shown in the chart below

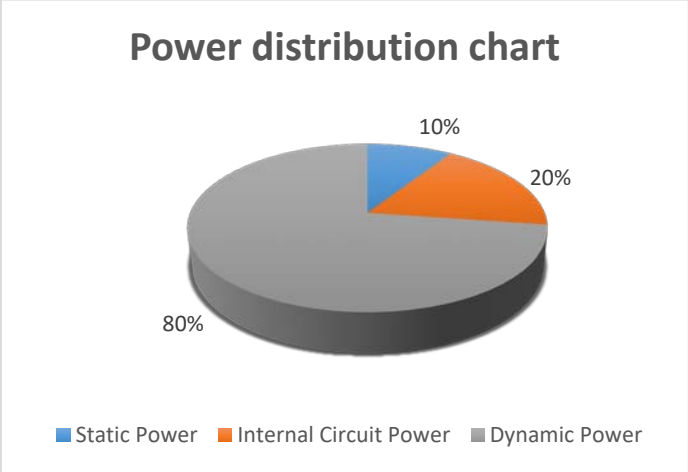


Figure 1: Total Power distribution chart

Since dynamic power contributes almost 80% of the total power it is the key factor for reducing the overall power loss of the circuit.

Dynamic power consists of internal power, switching power ,leakage power..Dynamic power distribution chart is shown below

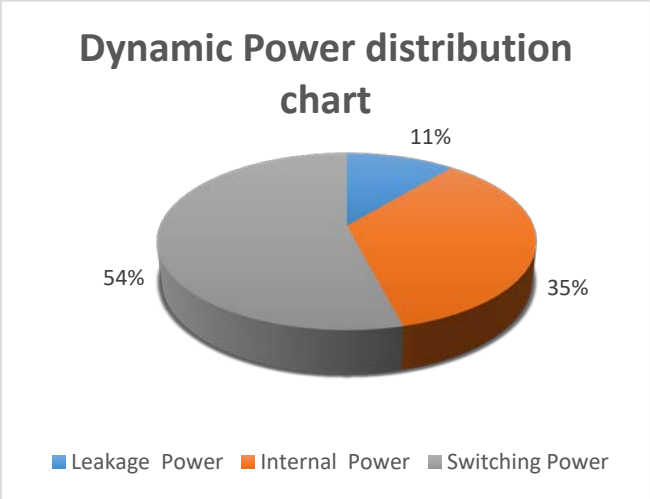


Figure 2: Dynamic Power distribution chart

From the above pie chart it is clear that major portion of the dynamic power consumption is because of switching activity of the cell or a net .In order to scale down the switching power we have to reduce the capacitance of the nets or cells which have high activity factor. In a typical digital design the clock nets will contribute more to the dynamic power since the activity of the clock nets will be high.

With these key parameters and deep understanding of the different types of the power consumptions and there contribution to the total power we propose three different power reduction techniques that help to reduce power at i physical design stage

## II. PROPOSED WORK

This paper details three different types of dynamic power reduction techniques in physical design flow namely power aware placement, multi-bit based on TNS, multi vt synthesis.

**Power aware placement:**

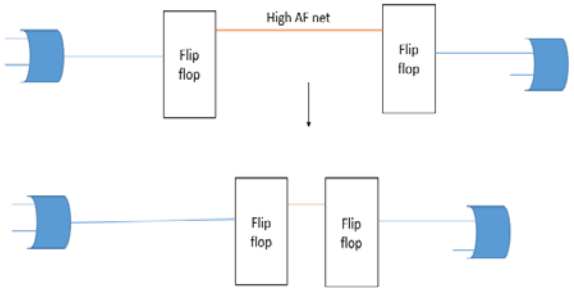


Figure 3: Power aware placement

Power aware placement feature reduces net switching power using switching activity based power-aware placement technology. In order to scale down the total switching power, power aware placement reduces the wire-length of higher activity nets so that the capacitance of higher activity nets get reduces, leading to smaller total switching power. But we have to take care about the timing as well since it may degrade the slope on the other nets. Its a trade of between the timing and power.

**Multi-bit conversion of sequential cells:** In multi-bit conversion is to reduce the clock inverters and buffers so has to scale down the switching power of the clock network.

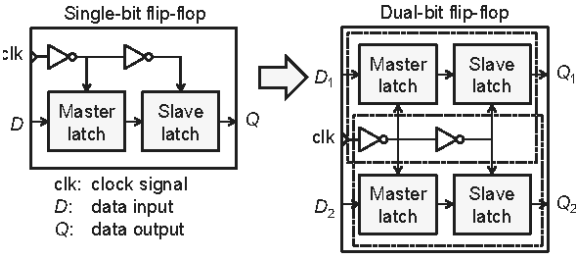


Figure 4: Single and Multi-bit flip-flops

Multi-bit conversion may be from single to dual or quad–bit flip-flops. Here multi –bit is done based on the TNS value. The flops which have nearly same TNS value are combined. This helps in less degradation in terms of timing. . Merging one bit flop into multi-bit flop can reduce number of clock inverter cells, and lower the dynamic power consumption due to clock network.

**Multi vth cell usage:** Cells power consumption vary with their threshold voltage. The cells which have high vth value have less leakage power but the delay is high and the low vth value cells have the low delay but the leakage power is high. In order to have good timing number and to reduce the leakage power we constrain the design to use nominal or low vt cells for sequential cells and all data path cells should be low vth cells in order to compensate the timing degradation.

## III. RESULT AND ANALYSIS

The result we obtained by applying the power reduction techniques are giving us good gain in terms of power .We applied all the power reduction techniques mentioned in the previous section one by one to a design with below number of cells

| | |
|---|---|
| Total devices | 580745 |
| clock cells | 1969 |
| Data cells | 43613 |
| Single bit cells | 6420 |

Figure 3: List of number of cells in the design

After applying the power aware placement technique we saw an improvement of 8% in power and timing degradation of 6ps.In multi-bit out of 6420 single bit cells 2505 cells were converted to dual cells and we gained 11% of power improvement when compared to the reference design. With the use of multi threshold voltage cells there was gain of 4% gain in power. Since the switching power contributes large part of the Total power, 11% of total power saving in today's submicron technology is a considerably a good number.

## IV. CONCLUSION AND FUTURE WORK

Power is one of the key parameter in physical design flow. Power reduction with degrading timing and quality of the design is challenge. With the right use of cell libraries and with the proper understanding of the design we can reduce the power. In future , combination of the different power reduction techniques can be tested based on the design, to reduce the switching power.

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