# Speedy Convolution Using Reversible Vedic Multiplier

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***Abstract-*** This paper presents a novel method for convolution of two finite length sequences using hardware description language(VHDL). Convolution is widely used in digital signal processing. The proposed design replaces conventional multiplier with reversible Vedic multiplier. The proposed design consumes only less area and have higher speed than existing method. Vedic mathematics is world renowned for its quicker mental calculation approach. Urdhva Tiryakbhyam Vedic multiplier is efficient in terms of both power and speed. The comparison of existing method with conventional is done using XILINX software.

***Index Terms***- Urdhva Tiryakbhyam Vedic multiplier, XILINX, reversible

## I. INTRODUCTION

Convolution is said to be the fundamental operation used in most of the signal processing applications. Convolution is a mathematical operation performed on two functions, producing a third function that is typically viewed as an effectively modified version of one of the two original functions. It has applications that include probability, statistics, computer vision, language processing, image and signal processing, engineering, and differential equations. So it is necessary to develop a method which improves the speed of convolution operation.

Vedic mathematics is an ancient form of mathematics used by Aryans. It improves the speed of operation, and the algorithms are based on mind calculations. The calculations are based on 16 sutras, of which Urdhva Tiryakbhyam sutra is used for Vedic multiplication. The proposed design uses reversible logic, therefore the power dissipation and delay reduces even more. In this paper, the delay and area of existing design is compared with proposed design.

## II. RESESRCH ELABORATIONS

### 1. Vedic Mathematics

Vedic mathematics is an Indian system of mathematics and is used by Aryans. Sixteen Sutras are used by this system for the mathematic calculations. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhyam sutra which means vertical and crosswise. Vedic mathematics is part of four Vedas [1]. It is part of Sthapatya Veda, which is an upa veda (supplement) of Atharva Veda [2].

The word “Veda” has the derivational meaning i.e., the fountainhead and illimitable storehouse of all knowledge [3]. Vedic mathematics is the name given to the ancient system of mathematics or, to be a unique technique of calculations based on some simple rules and principles with which many mathematical problems can be solved, it can be arithmetic, algebra, geometry or trigonometry.

The system of Vedic mathematics is based on sixteen Vedic sutras, which are actually formulae describing the natural ways of solving the whole range of mathematical problems. The highlights of Vedic mathematics lies in the fact that it reduces the complex, time consuming calculations in conventional mathematics to be a very simple one. This is so because the Vedic formulae works on the same way as that of how human mind works. This is a very interesting field of mathematics and presents effective algorithms which can be applied to various branches of engineering.

1.1. Vedic multiplier

Urdhva Tiryakbhayam (UT) multiplier is a multiplier based on Vedic mathematical algorithms. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications namely, Binary, Hex and also Decimals. It is based on the concept that generation of all partial products and then the parallel addition of these partial products can be performed [4]. The parallelism for generating the partial products and their summation is obtained using Urdhva Tiryakbhayam Sutra. Unlike other multipliers, the time delay in computation of the product does not increase proportionately with the increase in the number of bits of the multiplicand or multiplier, because of this the time of computation is independent of clock frequency of the processor. Therefore one can limit the clock frequency to a lower value. In addition, since the processors using lower clock frequency, it dissipate lower energy and is economical in terms of power factor to use low frequency processors employing fast algorithms. The advantage of using this Urdhva Tiryagbhyam Sutra is that, as the number of bits increases, the rate of increase of gate delay and area is slow[5] as compared to other conventional multipliers.

The block diagram of a conventional 2 x 2 Urdhva Tiryakbhyam multiplier is shown in Figure 1. The conventional Vedic multiplier uses conventional logic gates such as AND, XOR, etc. Using reversible logic the speed of the multiplier can be improved.

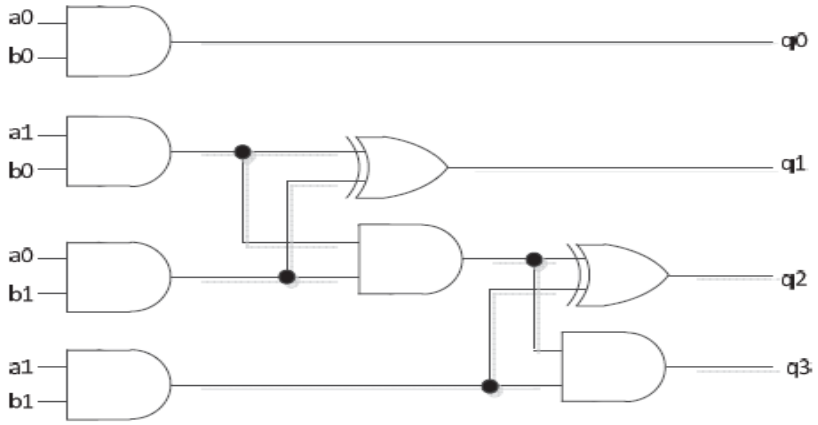


Figure 1: Conventional 2x2 Urdhva Tiryakbhyam multiplier

So the 2x2 Urdhva Tiryakbhyam multiplier is designed using reversible logic and is shown in Figure 2. 4x4 multiplier is designed using four 2x2 Urdhva Tiryakbhyam multipliers and is shown in Figure 3.

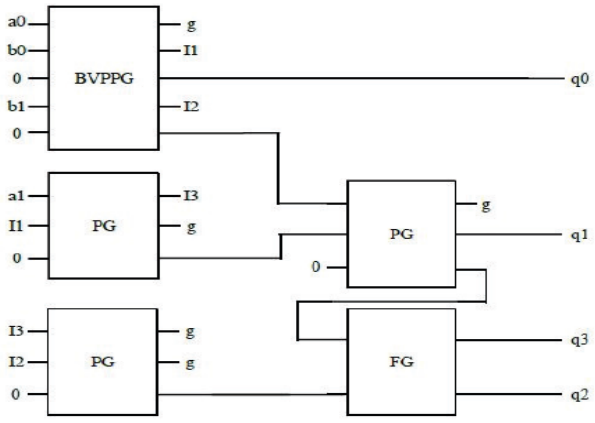


Figure 2 : Reversible 2x2 Urdhva Tiryakbhyam multiplier

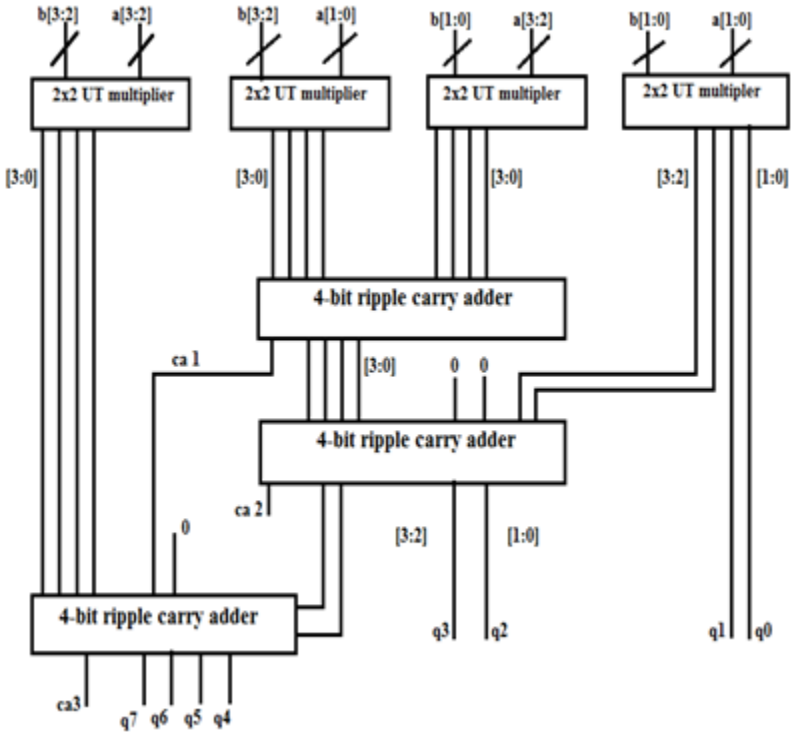


Figure 3 : Block diagram of Vedic multiplier

## 2. Reversible Logic

The information loss is associated with laws of physics requiring that one bit of information lost dissipates kT ln 2 Joules of energy, where k is Boltzmann's constant and T is the temperature of the system. For every single bit of information that being lost in the conventional combinational circuits are known to dissipate heat. This is also evident from the second law of thermodynamics , that any irreversible process leads to loss of energy. Landauer [5] showed that any irreversible gate, necessarily dissipates energy, and each irreversible bit generates k*T ln2 joules of heat where k is the Boltzmann's constant and its value is 1.38 x 10-23 joules/Kelvin and T is temperature in Kelvin. Inorder to reduce the energy consumption of any logical operation, the widely used methods are lowering the threshold voltage and management of the power supply. However these technologies of lowering the energy consumption will hit a barrier of kT. In order to alleviate this, techniques such as reducing the temperature of computer and constructing a thermodynamically reversible computer can be used. It has been analyzed that the second option was a better choice.

When the temperature of the system reduces to absolute zero, the energy gets reduced by two orders of magnitude. But using reversible computing there can be further more reduction in temperature that matches with the theoretical value. The cardinal feature of reversible computing is that electric charge stored on the storage cell consists of transistors are not permitted to flow away during transistor switching. This can be reused through reversible computing and thereby decreasing the energy dissipation. In 1973 Bennett showed that an irreversible computing can always be made reversible. Reversible logic circuits can naturally take care of heating. Since in a reversible logic, every input vector can be uniquely recovered from its output vectors and therefore no loss of information.

## 3. Convolution

The linear convolution is a basic operation in DSP which relates input signal and impulse response to obtain desired output [2]. Convolution is considered to be heart of the digital signal processing. It is the mathematical way of combining two signals to obtain a third signal, that is a modified form of one of the two signals. Convolution helps to estimate the output of a system with an arbitrary input, with knowing the impulse response of the system. The characteristics of linear systems are completely specified by the

impulse response of the systems , as governed by the mathematics of convolution. Convolution takes two functions as input, and produces a single output. The linear convolution of f (n) and g (n) is y (n) = f (n) * g (n) [6].

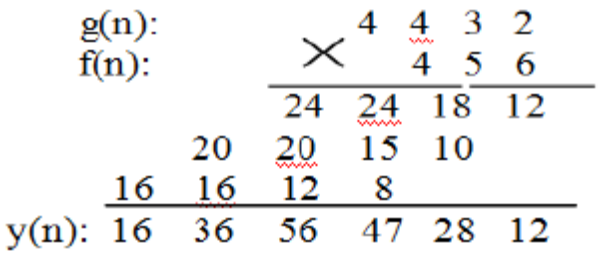


Figure 4.: Example of convolution

## 4. Proposed Design

The convolution of two 4-bit numbers is designed and implemented using reversible logic. The multiplier and multiplicand are selected using two 4:1 multiplexers. Then the multiplication operation, that is, the Vedic multiplication is performed and is stored using 1:16 demultiplexer [7]. The first two bit of four bit select line of demultiplexer is the select line of first 4:1 multiplexer. And the last two bits are the select line of second 4:1 multiplexer. Then the corresponding products are added in the adder section. The block diagram of the proposed design is shown in Figure 5.

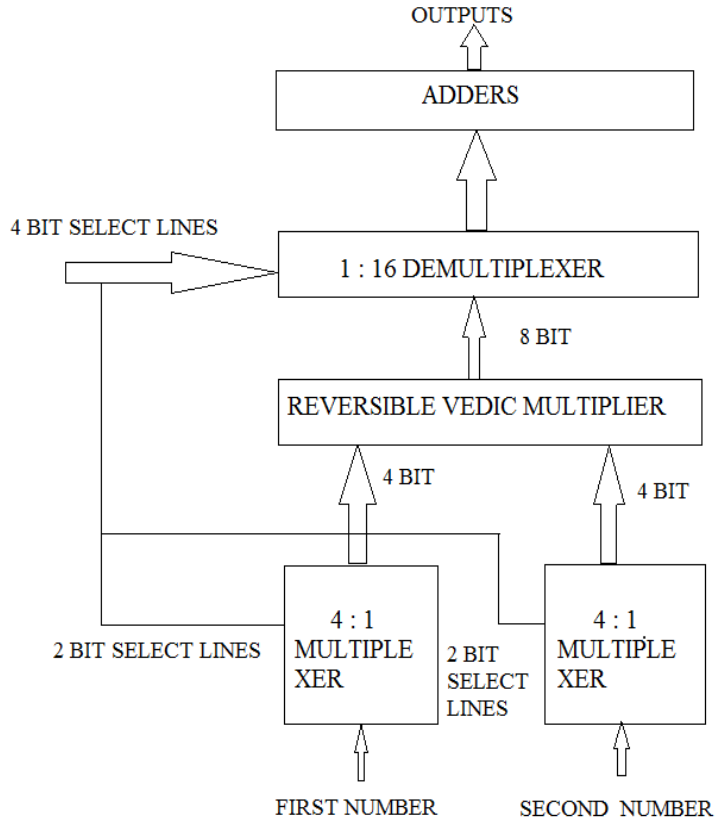


Figure 5: Block diagram of convolver

For the addition of two 8 bit numbers carry look ahead adder is selected. And for the addition of three and four 8 bit numbers carry save adder with last stage built by ripple carry adder is selected. The Vedic multiplier using reversible logic is then compared with conventional method.

## III. RESULTS

In this paper, the conventional design, i.e., Vedic multiplier using conventional logic gates is compared with the proposed design, i.e., the Vedic multiplier using reversible logic. The proposed design is compared with conventional design in terms of area and delay. The two designs were simulated using ISim. The area and speed of convolver is compared using Xilinx ISE design suite 12.1.

Table 1. Comparison of two designs

| Design | Delay(ns) | No. of LUTs |
|---|---|---|
| Proposed Design | 21.279 | 277 |
| Conventional Design | 23.569 | 298 |

From the obtained results it is evident that the convolution using reversible Vedic multiplier is more efficient than that of conventional Vedic multiplier in terms of both speed and area.

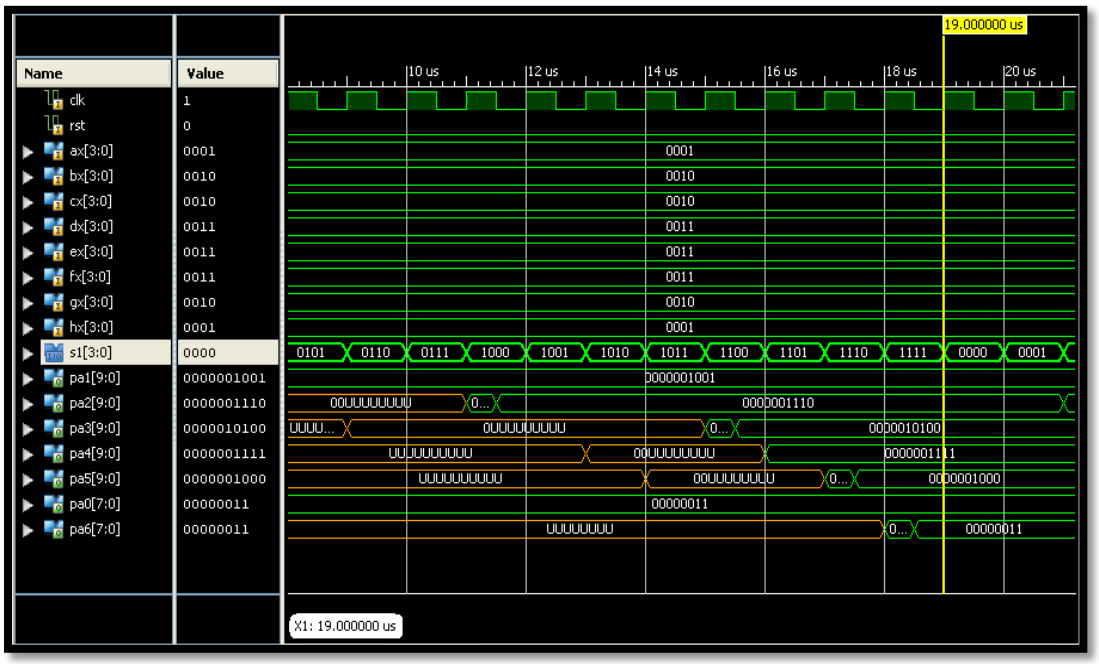


Figure 6: Simulation of proposed design

## IV. CONCLUSION

In this paper, convolution of two finite length sequence is performed using reversible Vedic multiplier and also using conventional method. By comparing these two designs, it is obtained that the convolution using reversible logic is efficient in terms of both area and speed.

**References**

[1] Karishma P Dighorikar, S. L. Haridas, "Area Efficient Architecture for Convolution Using Vedic Mathematics", *IJSR* , Volume 3 Issue 3, March 2014

[2] Madhura Tilak, "An Area Efficient, High Speed Novel VHDL Implementation of Linear Convolution of Two Finite Length Sequences Using Vedic Mathematics" , *International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075*, Volume-2, Issue-1, December 2012

[3] N. R. Punwantwar, Dr. P. N. Chatur, "Convolution and Deconvolution Using Vedic Mathematics", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 4, Issue 6, June 2015

[4] Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H, "Implementation of Multiplier using Vedic Algorithm, *International Journal of Innovative Technology and Exploring Engineering (IJITEE)* , Volume-2, Issue-6, May 2013

[5] Rakshith Saligram, Rakshith T.R ," Optimized Reversible Vedic Multipliers for High Speed Low Power Operations", *Proceedings of IEEE Conference on Information and Communication Technologies*, 2013

[6] Rashmi Lomte, Bhaskar P.C, "Speed Convolution using Vedic mathematics " , *Int. J. on Recent Trends in Engineering & Technology*, Vol. 05, No. 01, Mar 2011

[7] Khader Mohammad, Sos Agaian, "Efficient FPGA implementation of convolution", *Proceedings of the 2009 IEEE International Conference on Systems, Man, and Cybernetics San Antonio, TX, USA* , October 2009

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