A Comparative Study of Π and Split R-Π Model for the CMOS Driver Receiver Pair for Low Energy On-Chip Interconnects

Dr. Meghana Kulkarni, Shubha B Baravani

Dept. of Electronics and Communication, Gogte Institute of Technology, Belgaum
Dept. of Electronics and Communication, Gogte Institute of Technology, Belgaum

ABSTRACT - Ever increasing fraction of the energy consumption of an Integrated circuit is due to the interconnect wires (and the associated driver and receiver circuits). Power dissipation from the interconnect wires amounts to up to 40% of the total on-chip power dissipation in some gate array design styles. When compared with other techniques a diode-connected driver circuit has the best attributes over other low-swing signaling techniques in terms of power, and delay. The proposed signaling schemes of symmetric low-swing driver-receiver pairs (MJ-SIB) and (MJDB) for driving signals on the global interconnect lines, which are implemented using split R-π model for an interconnect line, provides best results.

I. INTRODUCTION

Market is continuously demanding devices with increased functionality/unit area; these demands have been satisfied through technology scaling which, has impacted greatly on the global interconnect delay subsequently reducing system performance. Use of lower supply voltages would be one of the solutions to reduce the power dissipation of the drivers. The performance of the line drivers for global interconnects is impaired unless low-swing signaling techniques are implemented. Low-swing signaling techniques provide high speed signaling with low power consumption and therefore can be used to drive global on-chip interconnects.

The most efficient way to achieve power reduction and Power -delay product efficiency on the global interconnects is reducing the voltage swing of the signal on the wire.

Various architectures for the interconnect driver and receiver have been proposed in this report.

When compared with other techniques a diode-connected driver circuit has the best attributes over other low-swing signaling techniques in terms of power, and delay. Incorporating a diode-connected configuration connected in split R-π model provides high speed signaling due to its high driving capability.

The conventional interconnect model usually employs a lumped RC segment however this model lacks the accuracy to model high-performance interconnect significantly with the increase in circuit operating frequency. An alternative to the lumped RC model is a distributed RC model. As the number of segments approaches infinity, the lumped approximation will converge with the true distributed circuit.

II. LITERATURE REVIEW

Not only the interconnect wires but also the associated driver and receiver circuits are responsible for an ever increasing fraction of the energy consumption of an integrated circuit. In some gate array design styles power dissipation from the interconnect wires amounts to up to 40% of the total on-chip power dissipation [1].

Measured over a wide range of applications, more than 90% of the power dissipation of traditional FPGA devices have been reported to be due to the interconnect [6]. As technology scales down, on-chip wires become increasingly important compared with devices in terms of power, delay and density [4].Most low-swing voltage techniques to-date rely on extra power supply, or reference voltage, multiple threshold process technology, large area penalty, and multiple wire interconnects when differential signaling is employed [5].Low swing interconnection techniques provide an efficient way to overcome full-swing signaling in terms of delay, power and noise immunity. A high performance, adaptive low/high swing CMOS driver circuit (mj-driver), which is suitable for driving the global, interconnects with large capacitive loads is designed. When implemented, mj-driver performs 16% faster, and reduces the power consumption by 3% [9].

The Low- swing signaling circuits which are implemented using π-model of the interconnect [10], are now in this paper implemented using the Split R-π model.

III. PROPOSED CIRCUITS

The split R-π model is the approximation of the distributed RC model. Equation for delay is given as

Delay=(R C L^2)/2

Where R= resistance of the interconnect,
C= capacitance and L= length of the interconnect
Hence, when R and C are reduced to half the original values, the delay gets reduced. Thus this concept of splitting the value of resistor and capacitor is used to reduce the delay.
Using this concept, the circuits mentioned in [10] are now modeled with split R-π model, which has proved to be better than interconnect implemented with nominal π-model. All the four circuits designed below (Fig 3.1, Fig 3.2, Fig 3.3 and Fig 3.4) are implemented using split R-π model for an interconnect

ASFLC (Asynchronous Source Follower with Level Converter)

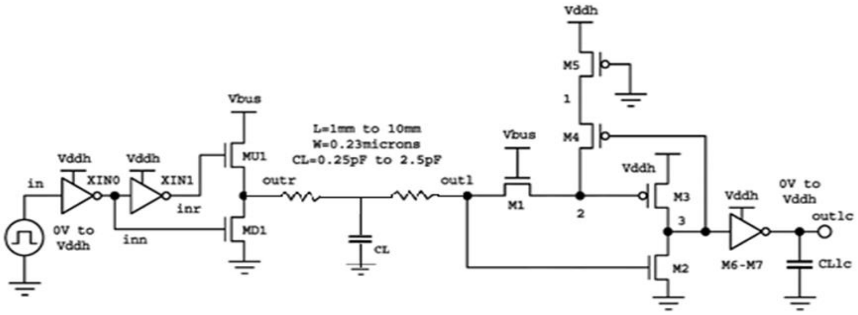

Fig 3.1 Circuit structure for the HOA CMOS driver-receiver ASF-LC, with Vddh =1.0 V, Vbus=2 V, Vtn=0.21 V, and |Vtp|=0.25 V.

In this circuit the driver is designed using a source follower. The receiver may be a simple inverter or level converter circuit. PMOS conducts when at point X1 when the value is zero, and the above PMOS is always on as it is connected to ground, and this particular operation makes the output to pass through lower transistors if the value is 1 the output follows the same direction .So the working principle behind level converter is to get the output at different time scale.

DDCD (Dynamically Diode Connected Driver Circuit)

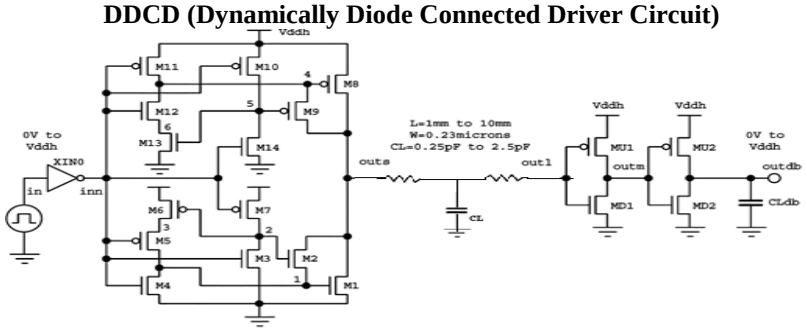

Fig 3.2 Circuit structure for the low-high offset symmetric (LHOS) CMOS driver-receiver DDC–DB, with Vdd =1.0 V, Vtn =0.21 V and Vtp=0.25 V

In the above circuit before driver circuit, a set of inverters, buffers and NAND gate is connected. The concept of merging and splitting of inverter is used, to split the current in the circuit and to increase fan-out of the circuit. The input from the previous inverter is used by the NAND gate. Basically the NAND gate sends a specific output to the next stage. The concept of dynamic diode is used to design the driver circuit (Diodes are realized using CMOS). Here we are using two dynamic diodes. In order to drive the input to output side efficiently the driver circuit is used, which is the next stage. The set of CMOS transistors are used so as to control the current in the diode, i.e his circuit is used to split the current in the diode to make it immune to excess current.

Driver circuit

The driving output transistor switches among three different modes: First, it is fully active, providing high drive capacity to quickly charge/discharge the line. Then, the driving transistor becomes diode-connected, limiting the line's voltage swing and offering lower

impedance then the source follower to better fight noise. The transistor finally turns off when the line is driven in the opposite direction

The working of the driver circuit is explained in there different modes,

Input is high: Transistors M3, M4 and M6 are on and M1 (the N driver), M2, M5and M7 are off (M1 off).

Input transition from high to low: Transistors M4, M3 and the P driver (M8) are turned off, M5 and M6 fully charges the gate of the N driver (M1), which fully activates the output transistor (active mode). As the line is driven towards ground, M7which is now active, turns M6 off and enables M2 to turn on. At this point of time, the gate of the N driver (M1) "holds" the charge while the line is discharging but not yet low enough to activate M2.When M2 is active, the voltage at the gate of M1 is driven to match the line ("diode-connected" mode).

Input transition from low to high: The same sequence as explained above is applied to the P driver (M8) side. The Dynamic Diode-Connected Driver has non-linear behavior of the energy and delay ratios with respect to Vdd mainly because, when Vdd is low, M9 and M2 may take longer to activate (to have enough Vgs), allowing the drivers to stay active longer, increasing the voltage swing despite the reduction of Vdd.

MJSIB (Multi Junction Single Band)

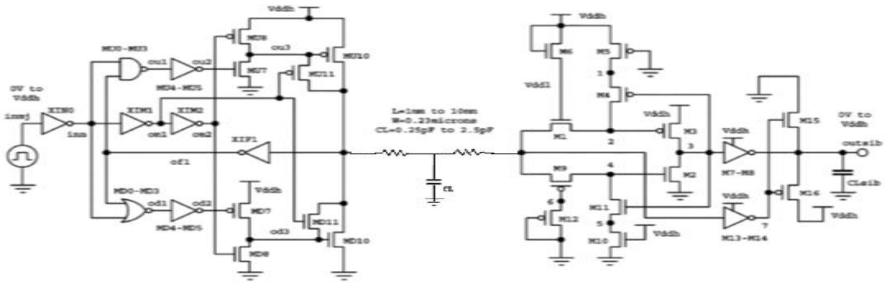

Fig 3.3 Circuit structure for the LHOS CMOS driver-receiver version I (MJ-SIB), with Vddh =1.0 V, Vtn=0.21 V, and |Vtp|=0.25 V.

Driver circuit

When the input is fed to the inverter, it increases the fan-out so as to drive three other gates i.e NOR, NAND and NOT gates. The logic gates connected before the DDC topology helps maintaining the input signal within the stable limits. The condition can be explained as follows: inmj=0, MU11 is ON and hence the drain and gate of MU10 are at equal potential. When UD2=0, it turns MD7 OFF and MD8 ON, which results in turning OFF MD10 and MD11.The output from XIM2 = 1, turning MU8 OFF. MU10 provides a path between the outmj to the ground meaning low voltage or 0 bit is transmitted. The operation of MJ-SIB driver part of circuit in Fig. 3.3 can be explained in as follows.

Low state at the output, outmj : For output outmj in the low state we have inn= outmj= low, ou1= high and ou2=low, MU7, MU10 and MU11 off and MU8 on. In this state, the output is driven low through the diode connected pair MD10 - MD11.

Low-to-high transition at the output, outmj : After a low-to-high transition at inn, due to delay in the feedback loop (XIF1), ou1, and ou3 will go low, and ou2 will go high briefly. This causes MU7, and consequently MU10 to turn on and strongly pull the output node outmj to high, to charge up the output load. The feedback loop eventually turns ou3 and ou2 to their steady state values of high and low, respectively, turning MU7 off, disabling it from driving the gate of MU10. However, transistor MU11 which was turned on when outmj went low will remain on, providing a diode connected configuration (pair MU10- MU11) to maintain the output voltage nearly at (|Vdd-Vtp|)

High state at the output, outmj : For output outmj in the low state we have inn= outmj= high, od1= low and ou2=high, MD7, MD10 and MD11 off and MD8 on. In this state, the output is driven low through the diode connected pair MU10 - MU11.

High-to-low transition at the output, outmj : After a high-to-low transition at inn, due to delay in the feedback loop (XIF1), od1, and od3 will go high, and od2 will go low briefly. This causes MD7, and consequently MD10 to turn on and strongly pull the output node outmj to low, to discharge up the output load. The feedback loop eventually turns od3 and od2 to their steady state values of high and low, respectively, turning MD7 off, disabling it from driving the gate of MD10. However, transistor MD11 which was turned on when outmj went high will remain on, providing a diode connected configuration (pair MD10- MD11) to maintain the output voltage nearly at Vtn.

Transmission Line: The transmission line is designed with π model analogy, consisting on cascaded resistors and capacitors. Hence our work is to find the efficient value of capacitor and resistor so that signals of any frequency can be transmitted without disturbing the key features of the signal.

Receiver Circuit : The operation of MJ-SIB receiver part of circuit in Fig.3.3 can be explained in as follows.

In the MJ-SIB receiver circuit, the pass transistor M1 isolates the internal node 2, from the previous stage. Without it the lower potential from the previous stage causes the current to flow from the Vdd through M3 back to the driver side. With node 2 isolated, the feedback transistor M4 can pull-up the gate of M3 above the high swing voltage level at the input Vin. The proposed sib-receiver uses the inverter (M13-M14), and M15 transistor to reduce the output pull-down transition time. Splitting the pull-up for node 2 to M4, and

M5 will help to reduce the load on node 3 and reduce energy consumption without hurting the performance M1 and M9 act as pass transistors and always at saturation ,hence M2 and M3 together act as an inverter. Introduction of M11 and M12 will ensure that there is no static power dissipation when M2 is not fully turned off when Vin is low. Finally, sib-receiver improves the low-to-high propagation delay through the introduction of the additional pull-up transistor M16.

The intermediate output is feedback by the two level converters. When Out1=0, the signal is sent forward through the buffer and therefore out sib=0. At the same point of time, when the expected voltage signal is not obtained, it is fed back through an inverter to the transistors M11 and M4.Now, Out1=0 implies that the output at node 3 is high, which switches M4 OFF and M11 ON. As M10 is always ON, node 4 is grounded, which turns M2 OFF.

Further, M9 and M1 being always ON will switch M3 ON and thus providing a conduction path between node3 and Vdd. The high voltage from Vdd then encounters an inverter and hence giving a low voltage signal/ bit at outsib. As for Out1 = 1, the upper level converter will be active and hence sending a high voltage signal/ bit at outsib.

MJDB (Multi Junction Double Band)

Driver circuit

When the input is fed to the inverter, it increases the fan-out so as to drive three other gates i.e NOR, NAND and NOT gates. The logic gates connected before the DDC topology helps maintaining the input signal within the stable limits. The condition can be explained as follows: inmj=0, MU11 is ON and hence the drain and gate of MU10 are at equal potential. When UD2=0, it turns MD7 OFF and MD8 ON, which results in turning OFF MD10 and MD11.The output from XIM2 = 1, turning MU8 OFF. There is path between outmj to the ground meaning, a 0 bit is transmitted, because of MU10.

Transmission Line

The transmission line is designed with π model analogy, consisting on cascaded resistors and capacitors. Hence our work is to find the efficient value of capacitor and resistor so that signals of any frequency can be transmitted without disturbing the key features of the signal.

Receiver circuit

The receiver has two inverters cascaded, which forms the buffer and stabilize the intermediate signal that may be affected by noise. Thus, giving the required signal at the output.

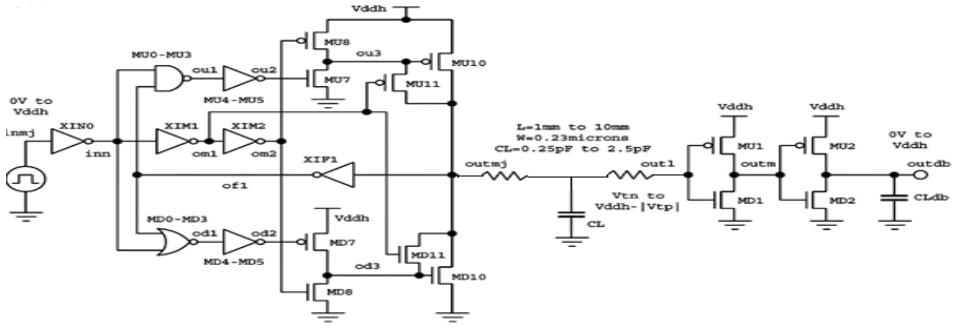

Fig 3.4 Circuit structure for the LHOS CMOS driver-receiver version II (MJDB), with Vdd=1.0 V, Vtn=0.21 V, and |Vtp|=0.25 V.

IV RESULTS

HOA						
PI Model				Split R- π model		
Values of R (K Ω)	Delay (n sec)	Power Results (m W)	Power-Delay Product (p W)	Delay (n sec)	Power Results (m W)	Power-Delay Product (p W)
1	58.1	4.280	248.668	15	2.196	32.940
5	69.9	2.846	198.935	14.2	3.826	54.329
10	89	8.840	786.760	31.3	7.326	229.303
15	109.7	7.707	845.457	Waveform distorted		
20	Waveform distorted			Waveform distorted		

25	Waveform distorted			Waveform distorted		
30	Waveform distorted			Waveform distorted		
DDCD						
1	37.2	1.034	38.464	31.7	0.295	9.351
5	36.6	1.244	45.530	32	1.239	39.648
10	39	1.149	44.811	32.5	0.647	21.027
15	45.1	1.659	74.820	33	0.894	29.502
20	47.3	1.805	85.376	33.5	0.946	31.691
25	48	1.994	95.712	34	1.174	39.916
30	50	2.005	100.12	34.4	1.293	44.447
MJ SIB						
1	7.3	2.275	16.607	3.7	3.507	12.975
5	9.8	1.981	19.413	5.2	1.941	10.093
10	16.6	1.377	22.858	6.2	1.762	10.924
15	23	1.095	25.185	7.6	1.816	13.801
20	25.4	0.965	24.531	9.2	1.616	14.867
25	30.6	3.222	98.593	11.35	1.459	16.559
30	Waveform distorted			15	1.334	20.010
MJ DB						
1	10.8	2.220	23.976	5.8	1.014	5.881
5	15.3	1.965	30.064	7.3	1.888	13.782
10	26.8	1.333	35.724	8.75	1.707	14.936
15	37	1.056	39.072	10.84	1.492	16.173
20	40.7	0.942	38.339	14.1	1.338	18.865
25	44.8	3.264	146.227	17.7	1.203	21.293
30	45.9	3.083	141.509	21.1	1.104	23.294

V COMPARATIVE EVALUATION

The study of result table proves that the MJSIB and MJDB schemes when implemented with nominal π- interconnect model perform better then ASFLC and DDCD. However MJSIB performs better than MJDB for shorter wire lengths as evident from Fig . 5.1.

When, the above schemes are implemented with split R-π model for the interconnect, power delay product is far better than the results obtained from nominal π model as shown in Fig. 5.2.

However, both MJDB and MJSIB when implemented with split R-π model for the interconnect line shows the performance improvement. The delay obtained for MJSIB implemented in split R-π model gives nearly 45 % improvement in delay, and 63 % improvement in power- delay product, compared to other counterparts. (Fig. 5.3)

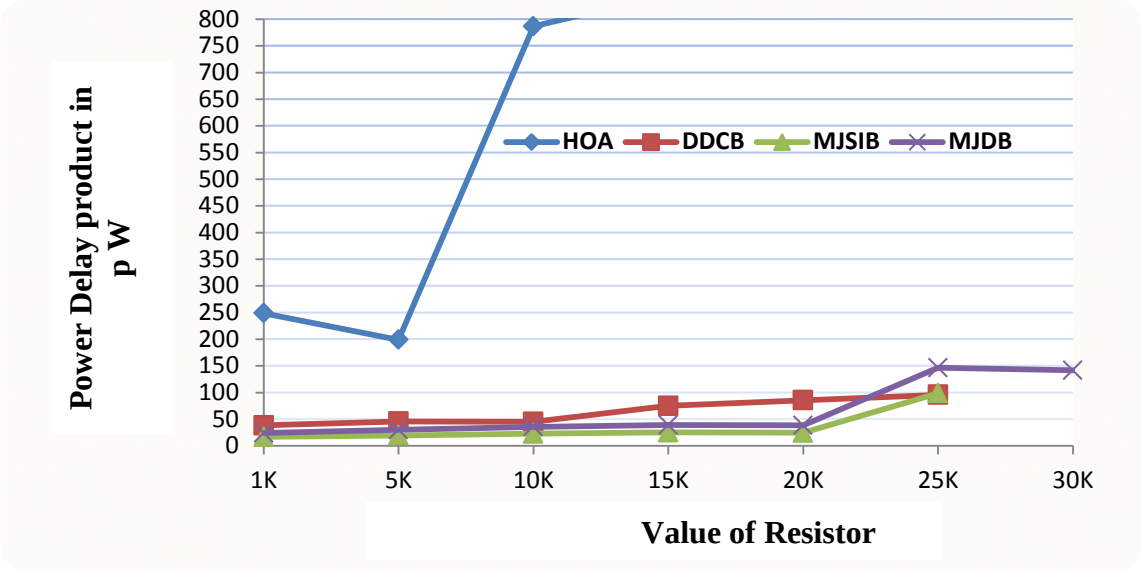

Fig. 5.1 Four schemes implemented wit π model

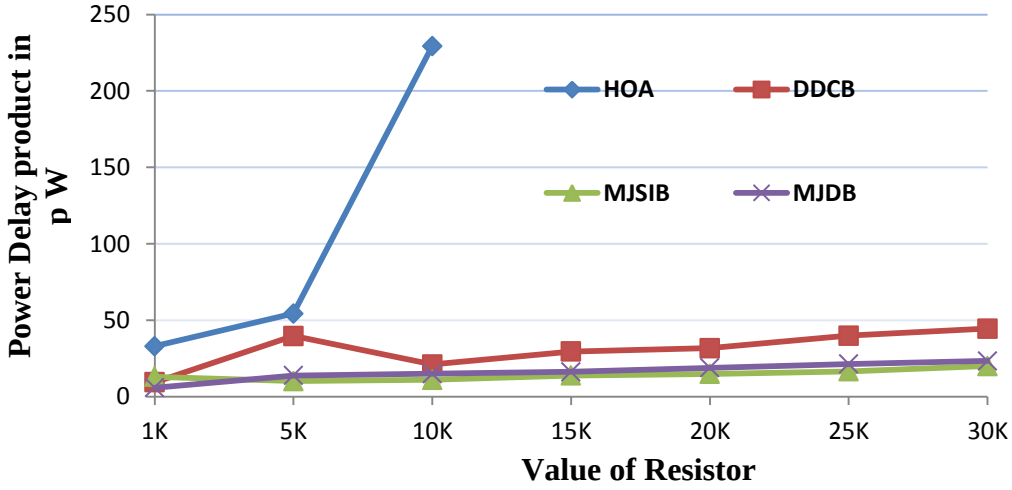

Fig. 5.2 Four schemes implemented with split R-π model

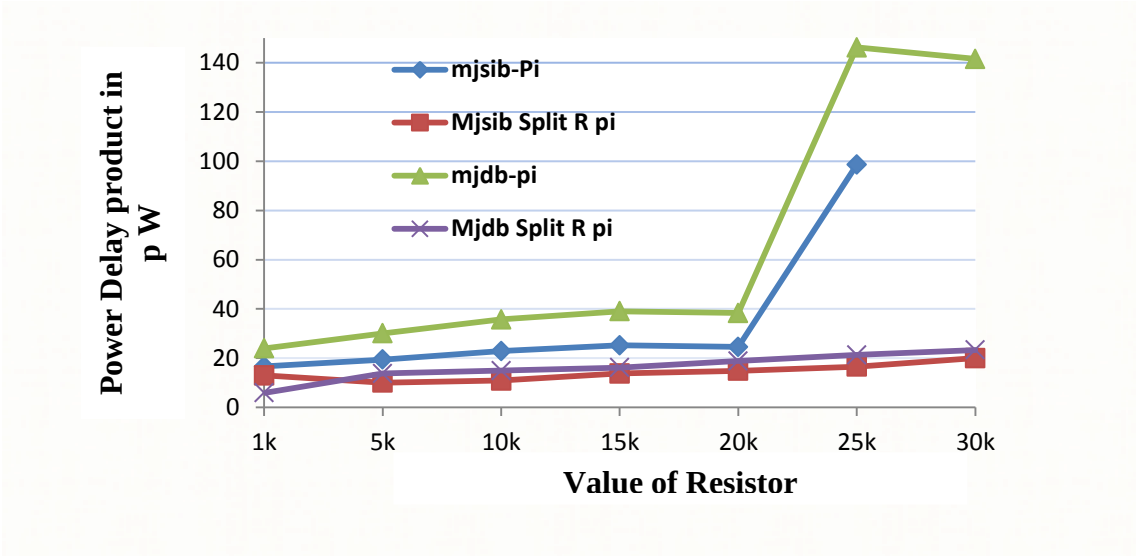

Fig. 5.3 MJDB and MJSIB schemes implemented with split R-π model and nominal π model

VI Conclusion

When all the four schemes are implemented with both the models for the interconnect, MJSIB LHOS scheme proves to be the best when compared with other configurations in terms of power, delay and power-delay product, either implemented with π-model or with split R-π model.

MJ-SIB scheme implemented in split R-π model reduces delay by up to 45% and power–delay product by up to 63% when compared with other counterparts.

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Authors

First Author – Dr. Meghana Kulkarni, M Tech, Ph D, Gogte Institute of Technology, Belgaum. meghnakulkarni@git.edu
Second Author – Shubha B Baravani, B.E , Gogte Institute of Technology, Belgaum. shubha_baravani07@rediffmail.com