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An Improved VCO Design with Negative Feedback to Reduce Jitter at High Frequencies

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Abstract- This paper presents an improved design of voltage controlled oscillator (VCO) utilizing the three differential cell CMOS inverters for forming the ring oscillator. The differential cell reduces the power supply fluctuations impact on the oscillator jitter while the negative feedback from frequency to voltage converter reduces the jitter at high frequencies. Finally the proposed model is designed using CMOS 0.18um foundry technology and simulated using P-Spice software. The result shows that the proposed design improves the jitter attenuation at different offset frequencies up to 40dB.

Index Terms- Phase Locked Loop (PLL), Voltage Controlled Oscillator (VCO), Ring Oscillator, Jitter, Phase Noise.

I. INTRODUCTION

A CMOS ring voltage controlledBasic inverter oscillator was initially used for clock recovery inEthernet controllers. Since then, the ring oscillator hasbecome a widely used component in communication system. In this role, the ring oscillatoris still the most widely produced of all oscillators ascompared to alternatives such as LCresonator-based oscillators. Since the ring oscillator is exceptionallycompact hencea large number of ring oscillators can be designed with the samechip area as a small spiral inductor also it can oscillateat very high frequencies, (very short periods limited onlyby gate delays), which is far greater than maximum oscillation frequencyof RC phase shiftoscillators. Furthermore the ring oscillator provides a large frequency tuning range. One of the major application area of ring oscillators is PLL. The Phase locked loop (PLL) is a critical component in many highspeed communication systems, because it provides the basis for time functions such as clock control, data recovery, and synchronization. Looking inside of a PLLthe Voltage-controlled-oscillator (VCO), is the most important element of the PLL, which can be built by Ring structures, relaxation schemes, or LC resonant circuit. LC design has the best noise and frequency performance with a good quality factor Q of the resonant networks. However, adding high-quality inductors to CMOS design increases the cost and complexity of the chip, it also introduces problems such as eddy currents.Ring oscillators, on the other hand, can be built in anystandard CMOS process may require less space die LCdrawings. The design is simple, and ring architecturescan be used to provide multiple output stages and wide tuningranges. However, the ring oscillatorusually shows poorer phase-noise performance than the LC-tank oscillator because of its low effective quality factor. The time jitter in a normal periodic signal can be considered as fluctuations inphase at the discrete set of zero-crossing instant. The fluctuations are causedby the phase noise of an oscillator, which is defined as continuously evolvingstochastic process. The jitter can arise from many reasons such as unwanted injection of signals from other parts of circuits, inherent thermal noise etc.

In this brief, we present an improved of CMOS ring oscillators design controlled by a frequency to voltage converter through negative feedback and developed aprototype circuits implemented in TSMC CMOS 0.18um foundry technologywhich shows the excellent jitter reduction. In rest of the paper the section II presents the functional overview of ring oscillators followed by section III which explains the phase noise and jitter in CMOS ring oscillators. The Section IV presents the proposed design and it functionality while Vth section simulation results are presented and finally section VI the conclusion on the basis of simulated results are derived.

II. RING OSCILLATOR

A ring oscillator consisting of a number of delay stages in a loop, which constitutes a negative unstable feedback loop. The period of oscillation is twice the sum of the delay of each delay cell in the ring. Figure 1 shows the linear model of a three-stage ring oscillator. The open loop transfer function of this model is:

$$H_{j\omega} = \left(\frac{-g_m R}{1 + Rj\omega C}\right)^3 \dots\dots\dots\dots\dots\dots (1)$$

Where g_m is the gain of each delay stage of the signal, R and C are the load resistance and capacitance at the output of each delay stage. The circuit oscillates only if the frequencydependent phase shift equal to 180 degrees thatmeans, if each phase contributes 60 degrees.The frequency at which this occurs is givenby:

$$\tan^{-1} \omega_{osc} RC = 60^o \dots\dots\dots\dots\dots\dots (2)$$

Hence

$$\omega_{osc} = \frac{\sqrt{3}}{RC} \dots\dots\dots\dots\dots\dots\dots\dots (3)$$

The minimum voltage gain per stage must be such that the magnitude of the loop gain at ωosc is equal to unity:

$$\frac{(g_m R)^3}{(1+(w_{osc}RC)^2)^{\frac{3}{2}}} \geq 1 \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

$$g_m R \geq 2 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

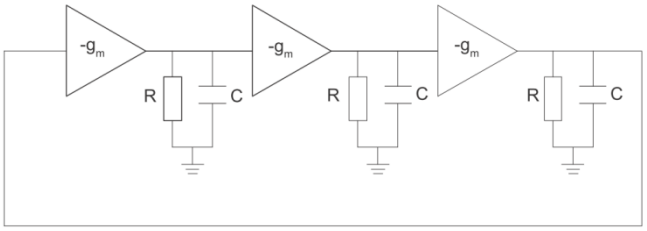


Figure 1: Linear model of a three-stage ring oscillator.

The minimum number of stages of a ring oscillator is 3, because for rings 1 or 2 stages does not provides phase shift sufficient for oscillation. The frequency of oscillation is usually controlled by varying the bias current of the delay cell. However, since ring oscillators do not have high-Q tank for the selection of frequency, have traditionally much more phase noise of oscillators based LC-tank.

2.1 VCOs based on differential ring oscillator

Presenly almost all mixed signal ICs use ring oscillators stages of differential delay because of their higher immunity to interference power and the noise substrate. A phase differential delay with the conventional bias circuit replication is shown in Figure 2. The frequency of oscillation of a N-stage differential ring oscillator can be expressed as:

$$f_o = \frac{1}{2Nt_d} \approx \frac{I_{bias}}{NC_L V_{sw}} \ldots\ldots\ldots (6)$$

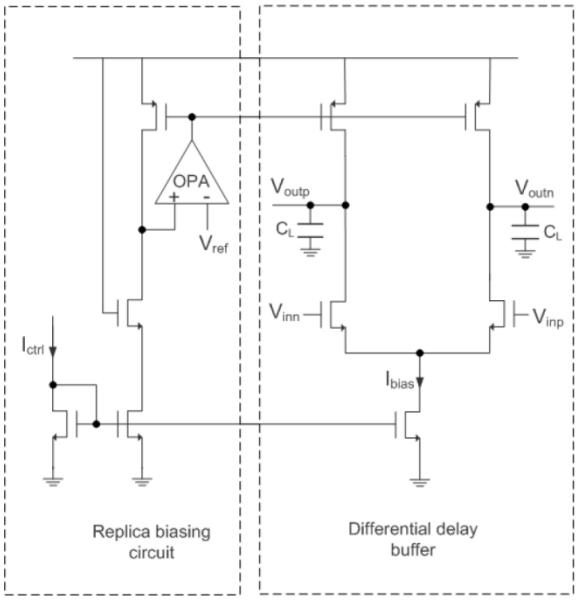


Figure 2: A differential delay buffer with the replica-biasing circuit.

where V_{sw} is the oscillation of the output voltage. The frequency of oscillation is controlled by current I_{ctrl}. The bias circuitreplication is made from an operational amplifier and the copy of the buffer half delay. Through negative feedback, the output swing is maintained at a constant value $V_{DD} - V_{ref}$ independent of the bias current. The value of V_{ref} is chosen so that the PMOS load transistors work in the triode region.

III. Phase Noise and Jitter in CMOS Ring Oscillator.

3.1 Phase Noise General Defination

The output of an ideal sinusoidal oscillator can be expressed as:

$$V_{out} = A\sin(\omega_o t + \varphi) \ldots\ldots\ldots\ldots (7)$$

where A is the amplitude, ω_o is the oscillation frequency, and φ is an arbitrarily fixed phase reference. Therefore, the spectrum of an ideal oscillator is apair of impulses at ± ωo . In a practical oscillator, however, the output is moregenerally given by:

$$V_{out} = A(t)\,f\big(\omega_o t + \varphi(t)\big) \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

where $A(t)$ and $\varphi(t)$ are now functions of time, and f is a periodic functionwith a period of 2π. As a consequence of the fluctuations represented by $A(t)$and $\varphi(t)$, the output spectrum of a practical oscillator has sidebands closeto the oscillation frequency ω_o. A signal's short-term instabilities are usuallycharacterized and measured in terms of the single side-band spectrum density.It has units of decibels below the carrier per hertz (dBc/Hz) and is defined as:

$$L_{total}(\Delta\omega) = 10\log\left(\frac{P_{sideband}(\omega_o + \Delta\omega, 1Hz)}{P_{carrier}}\right) \ldots\ldots (9)$$

where $P_{sideband}(\omega o + \Delta\omega, 1Hz)$ represents the single sideband power at afrequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of$1Hz$. The above definition includes the effect of both amplitude and phasefluctuations, $A(t)$ and $\varphi(t)$. However, in an oscillator, the amplitude noise isnaturally rejected by the limiting action inherent in any real implementation.Therefore, in most applications, $L_{total}(\Delta\omega)$ is dominated by its phase portion,$L_{phase}(\Delta\omega)$, known as phase noise, which is simply denoted as $L(\Delta\omega)$.

3.2 Phase Noise in Differential Ring Oscillators

A differential ring oscillator consists of several differential delay stages connected in series. The advantage of differential ring oscillator is that the noisefrom the supply and the substrate appears as common mode on both outputs,and is rejected by the next stage. A typical differential delay stage is shownin Figure 3. It consists of a differential pair, a tail current transistor, capacitor loads and resistor loads. In actual circuits, the resistor R_L is realized witha single or compound MOSFET working in triode region, embedded in anamplitude control loop.The propagation delay of the differential delay stage is defined as the timet_d between an input step and the zero crossing of the differential output voltage. The differential peak output voltage swing is:

$$V_{op} I_b R_L \ldots\ldots\ldots\ldots\ldots (10)$$

As the loads are RC circuits, the propagation delay and the oscillation frequency are determined by decaying exponentials:

$$t_d = \frac{C_L V_{op} ln2}{I_b} = R_L C_L ln2 \ldots\ldots\ldots\ldots (11)$$

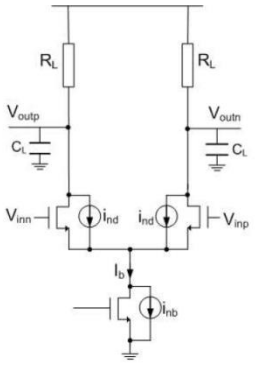


Figure 3: A typical differential delay stage in ring oscillators.

$$f_o = \frac{1}{2M t_d} \ldots\ldots\ldots\ldots\ldots\ldots (12)$$

The differential pair has an input transition range of:

$$V_{id} = \pm\sqrt{2V_{eff}} \ldots\ldots\ldots\ldots\ldots\ldots (13)$$

over which it steers the tail current. V_{id} is the input differential voltage, andV_{eff} is the effective gate voltage on the differential pair at balance.

Since the differential inverter already suppresses the phase noise due to power supply flactuations and flickers the phase noise in such systems is only caused by the jitter at the moment ofthe zero crossing of the output differential voltage or by the fluctuations in voltage of the zero crossing moment (also called Phase Noise Due to White Noise). The SSB phase noise due to white noise in the differential ringoscillator is Defined by:

$$L(f) = \frac{2kT}{I_b ln2}\left[\gamma\left(\frac{3}{4V_{effd}} + \frac{1}{V_{effb}}\right) + \frac{1}{V_{op}}\right]\left(\frac{f_o}{f}\right)^2 \ldots\ldots\ldots (14)$$

where V_{effd} is the effective gate voltage of the differential pair at balance.g_{mb} is the small signal transconductance of the tail transistor.

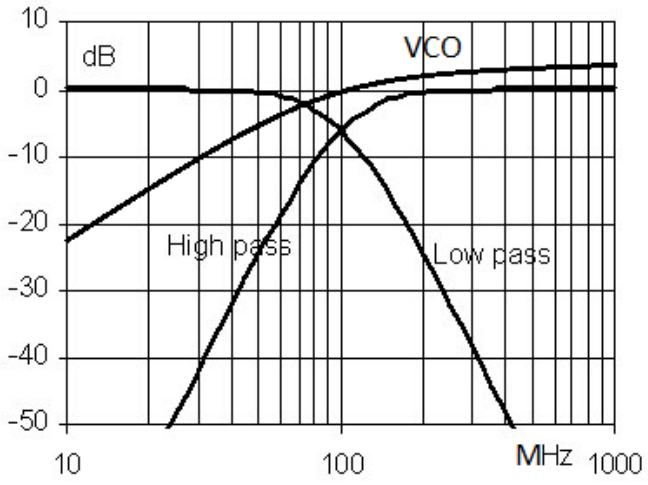
Now according to equation 14 the following conclusions can be drawn for the phase noise.

1. The phase noise is independent of the number of delay stages, and only depends on the frequency of oscillation f_0. Thus, the phase noise is equal in two rings which oscillate at the same frequency, where one ring comprises a few stages loaded heavily while the other ring comprises more lightly loaded stages.
2. The only technology-dependent parameters are V_t and γ.

IV. Proposed Work

The bloack diagram of the proposed design is shown in figure 3, as it shows that design consists of a negative feedback block in between the output and input of the VCO. The importance of the circuit can be explaind by analyzing the behaviour of ring oscillator for phase noise and jitter. Since the phase noise of the ring oscillator increases with the frequency of oscillation.The phase noise in caused by fluctuations in theinstants when the output ramp in a delay element crosses thetoggle point.

Figure 4: Block Diagram of Proposed Model



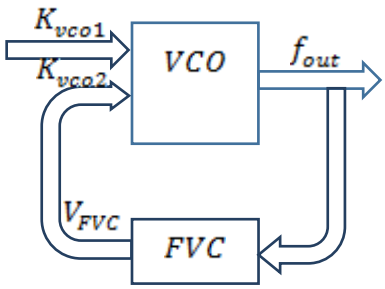


Figure 5: Jitter in a VCO using Differential Ring Oscillators can be modeled as High Pass Filter, and if another High Pass Filter is used with Negative feed back it can convert the VCO jitter transfer function to Low Pass Filter and can reduce the Jitter at higher frequencies.

In the proposed work the High Pass Filter for the feed back loop is designed by voltage to frequency converter (VFO), which generates the output voltage in proportion to the output frequeny of VCO.

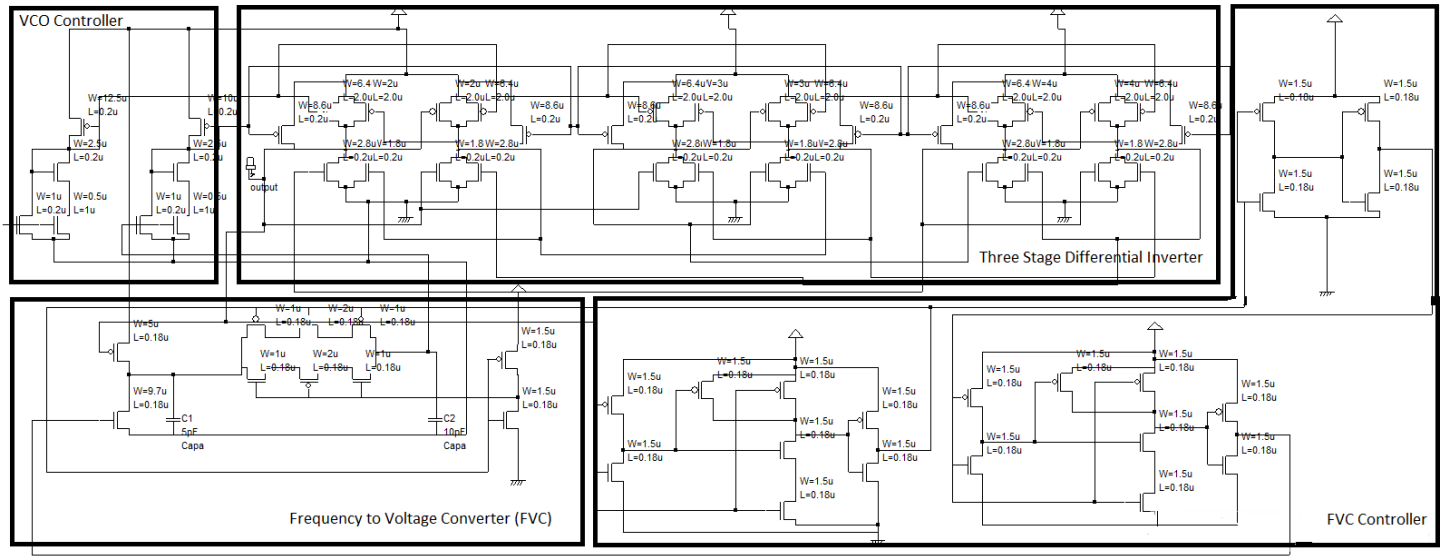


Figure 6: Circuit Diagram of the Proposed Model

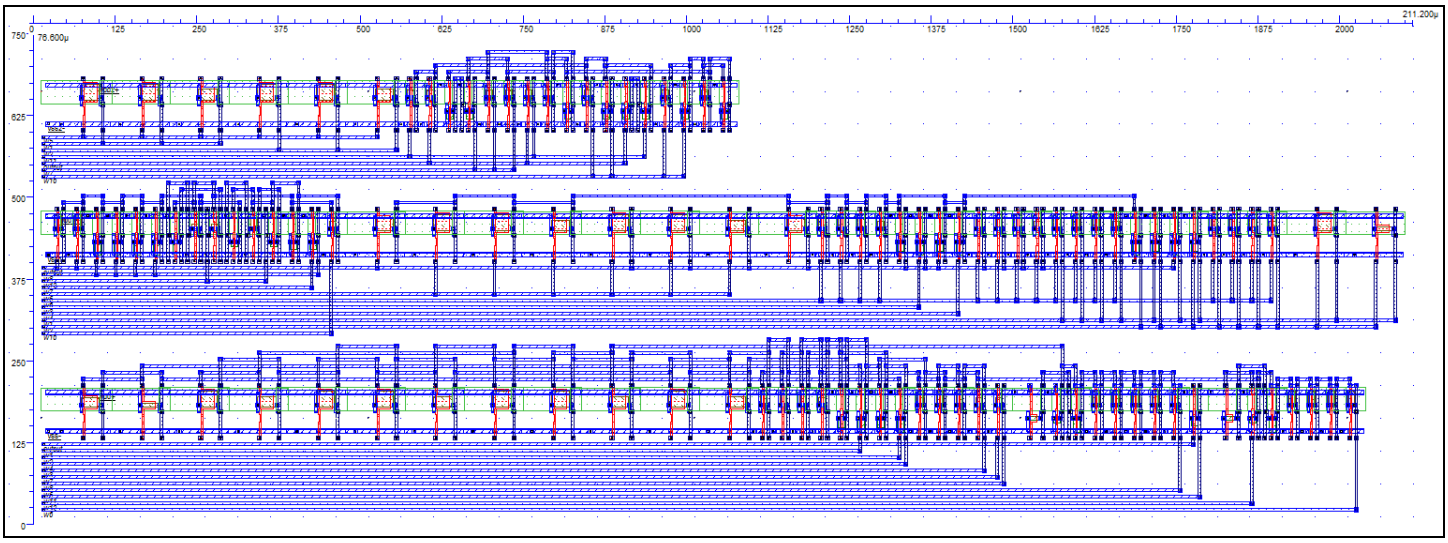


Figure 7: Layout Diagram of the proposed VCO

V. Simulation Results

The Proposed ring-oscillator-based VCOhas fabricated in 0.18um CMOS technology. Since the design does not contains any capacitors hence implementationdoes not reuires MOS capacitance. A layout of the fabricated VCO is shown in Fig. 7. Which requires the core area of 100umX50um. The activearea is approximately equal to 0.19 mm 2. The prototype has been tested for oscillation frequency of 1 GHz. The measured output spectrum of the VCO is shown inFig. 8, which presents maximum ampletude at the 1 GHz.Figure 8 also shows the phase noise of the prototype. Using the Phase Noise Calculation as mentionedin (9) and converting it for volatage

$$L_{total}(\Delta\omega) = 20\log\left(\frac{V_{sideband}(\omega_o + \Delta\omega, 1Hz)}{V_{carrier}}\right) \dots\dots (15)$$

$$L(f) = \left(\frac{V_{sideband}(f_o + \Delta f, 1Hz)}{V_{carrier}}\right)^2 \dots\dots\dots (16)$$

$$RMS\ Phase\ Noise = s(f) = \frac{180}{\pi}\sqrt{2\int L(f)\,df} \dots . (17)$$

$$RMS\ Jitter = J_{RMS} = \frac{s(f)}{2\pi f} \dots\dots\dots\dots\dots\dots . . (18)$$

$$L_{total}(1\ MHz) = 20\log\left(\frac{10^{-9}}{1}\right) = -180dBc/Hz$$

$$s(1\ MHz) = \frac{180}{\pi}\left(10^{-6}\sqrt{2}\right) = 8.103 * 10^{-5}$$

$$J_{RMS} = \frac{8.103 * 10^{-5}}{2\pi * 10^{9}} = 0.0139ps$$

the phase noise is –180 dBc/Hz at 1MHz offset fromthe 1.0 GHz carrier and the jitter performance of the VCOfor same offset is 0.0139 ps RMS.

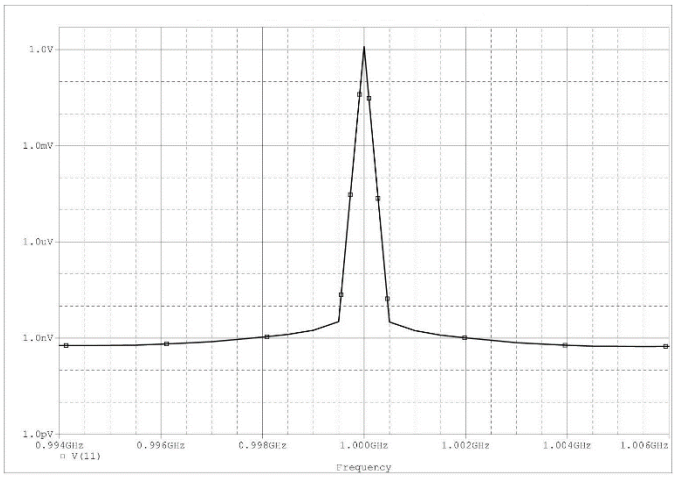


Figure 8: the FFT of the output waveform from Propsoed VCO.

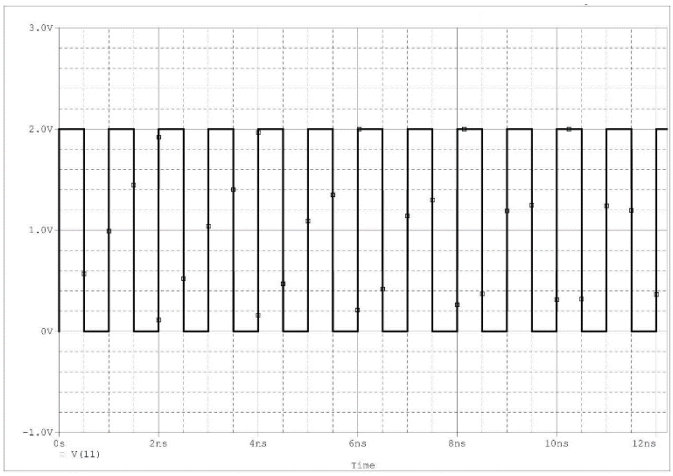


Figure 9: the Generated output waveform (1 GHz)

The power consumption of the proposed design is 1.3mW which is also considerably low.

VI. Conclusion

This paper presents a negative feedbackcontroller VCO architectureaimed to reduce jitter noise, especially for a VCO working at higherr frequencies. Firstly Phase noise due to power suppy flactuations is inherently improved by differential ring oscillator secondly the use of VFCat feedback loop enhance noise rejection. A wide operating frequency range over allPVT is obtained by using a dual-delay path scheme and digital calibration techniques in the VCO. Experimental resultsdemonstrate that the proposed PLL is a good solution to improve noise rejection.

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