

VOLTAGE LEVEL SHIFTER USING MODIFIED WILSON CURRENT MIRROR AND ITS APPLICATION

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Abstract: This describes the architecture of voltage level shifter and an application of voltage level shifter. Voltage level shifter plays an important role in circuits with multi-supply. Level shifter are used in between blocks for voltage level shifting. The proposed level shifter converts sub-threshold voltage level to supply voltage with increased speed and low power consumption. The multi-threshold voltage CMOS technique is used in the design of voltage level shifter in order to reduce delay and power consumption. This design has been implemented in 180nm, 90nm and 45nm technologies in Cadence virtuoso. The propagation delay, power consumption is verified.

Keywords- CMOS,nMOS, pMOS, voltage level shifter.

I. INTRODUCTION

As , the size of electronics devices goes on decreasing and , the demand of battery-operated devices like phones, laptops etc is increasing, power consumption is the

amount of power consumed by the device. Power consumption is of two types- static and dynamic power consumption. Static power consumption is due to leakage current in the circuit. And , dynamic power consumption is due to charging and discharging of load capacitors. Dynamic power consumption can be reduced by reducing supply voltage. Delay and power consumption is main concern. Delay can be reduced by increasing the supply voltage but increase in supply voltage increases power consumption.

Now-a-days, in a small area ,larger circuits are implemented. To avoid the problem of delay, multiple power supply is used. The circuit with multiple supply is divided into parts and each part is applied with individual supply to reduce delay in larger circuits.

As ,implementing individual power supply in multi-supply circuits increases the size of the circuits and makes it clumsy. So, voltage level shifter is used between blocks with more speed and less power consumption is implemented.

II. VOLTAGE LEVEL SHIFTER

A. Proposed design

This level shifter uses a Modified Wilson Current Mirror and an inverter between two NMOS. The operation is as follows, when input is high, MN1 and MN2 are on and off respectively. MP1 goes off and MP2 is on and output is taken as high. When input is low, MN1 is off and MN2 goes on making MP1 and MP2 on and off respectively.

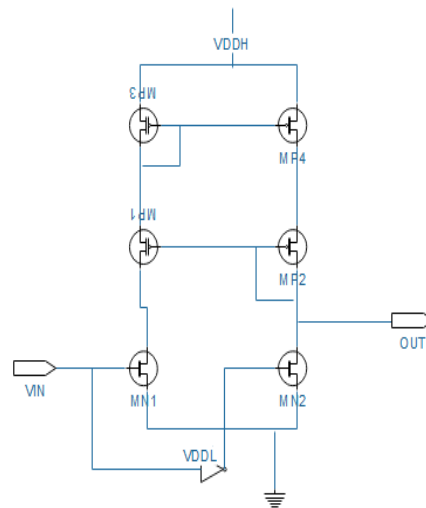


Fig 1: Proposed voltage level shifter

B. Multi-supply design

In order to verify the working of the proposed level shifter, it is implemented in multi-supply design. This application is composed of three blocks- Half-adder voltage level shifter and D- Flip flops.

The inputs are applied to half-adder . The half-adder provides two outputs- SUM and CARRY. The SUM is allowed to one voltage level shifter and CARRY to another. The level shifter converts the voltage range from 1v to 3v. Then ,the outputs are applied to D-Flip flop for storing the data. As Flip-flops can store only one bit of data. So, here two flip flops are used. The operation is explained as follows-

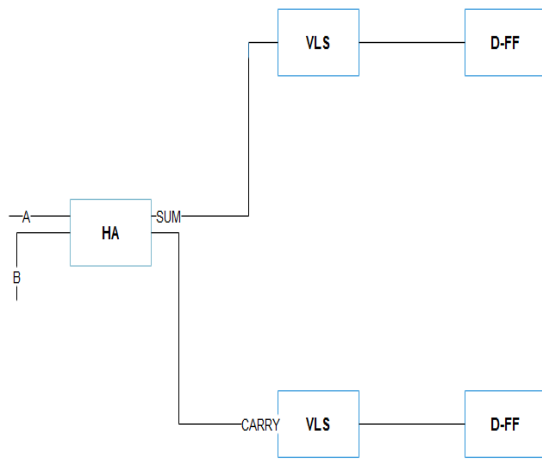


Fig 2: Block Diagram of Multi-Supply design

1) Half-adder

Half-adder is a combinational circuit that performs addition operation. It has two inputs and two outputs. Here, half-adder operates at 1v supply voltage. It consists of one XOR gate and one AND gate.

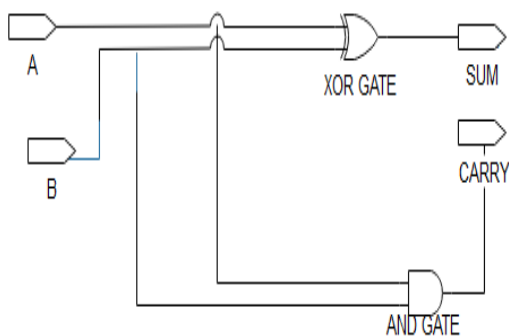


Fig 3: Half-adder circuit

The CARRY bit is high, only if both the inputs are high. And , the SUM is high , when the inputs are not same in other words, when one input is high and the other is low, the SUM is high.. this output is given to the Voltage level shifter.

2) Voltage level shifter

The output of half-adder is given to the voltage level shifters. The SUM is applied to one level shifter and CARRY to the other. The voltage level shifter shifts the voltage level from 1v to 3v. The D-Flip flop operates at 3v supply.

3) D- FLIP FLOP

The D-Flip flop comprises of four NAND gates and one inverter. It is used for storing data. It is also termed as Delay flip flop because it applies some delay at the output. It operates at 3v supply.

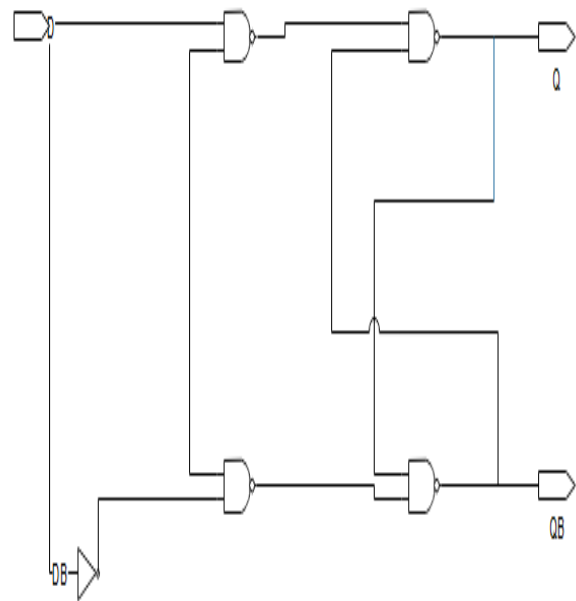


Fig 4. D-Flip flop circuit

When input to half-adder is applied (a=1, b=1) then, SUM=0, CARRY=1 for half-adder as, the half adder operates at 1v supply the output voltage range is also at 1v. this output is applied to two different level shifters. SUM is applied to one level shifter and CARRY to other for level shifting. The output of level shifter is at 3v supply. The output of first level shifter is applied to one D-Flip flop and CARRY to other.

III. SIMULATION RESULTS

A. Proposed design

The proposed level shifter is implemented at 180nm, 90nm and 45nm technologies in Cadence virtuoso simulator. The delay , power consumption are verified. Area is calculated using layout.

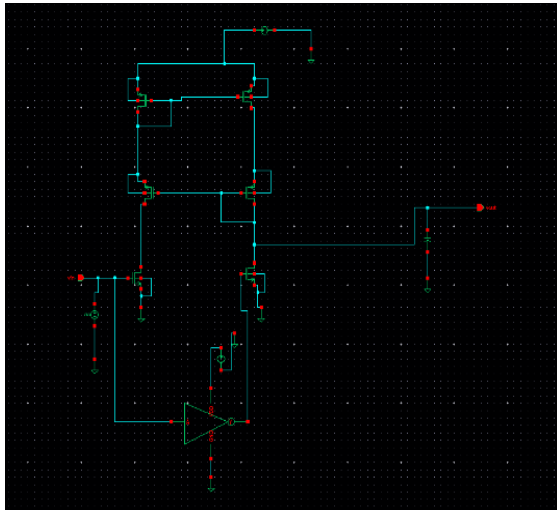


Fig 5. Schematic of proposed level shifter

It operates at VDDL=1V and VDDH=3v. the schematic is implemented at 180nm technology in Cadence virtuoso simulator.

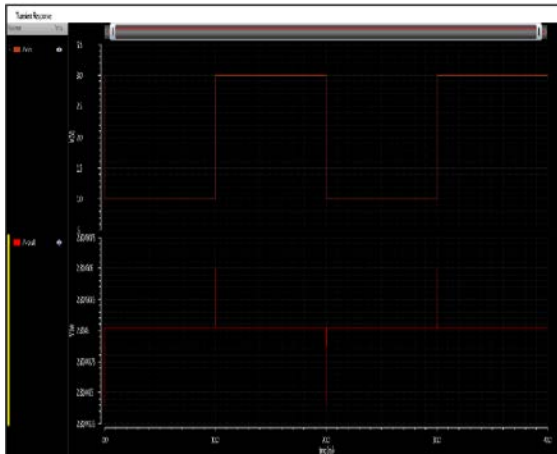


Fig 6. Waveform of proposed design

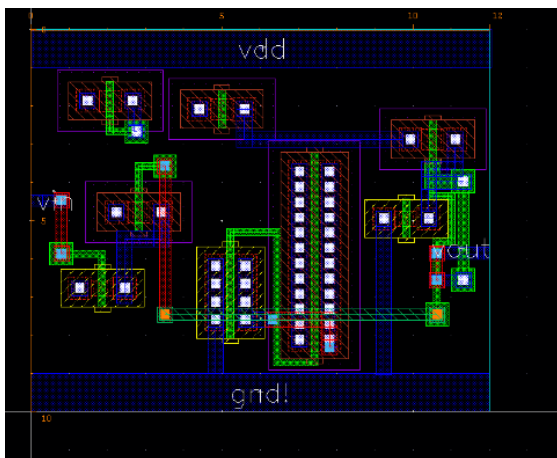


Fig 7. Layout of proposed design

TABLE I

COMPARATIVE SIMULATION RESULTS SHOWING PROPAGATION DELAY AT DIFFERENT TECHNOLOGIES

AT VDDH=3V, VDDL=1V

Level shifter	180nm	90nm	45nm
Proposed level shifter	1.56 *10 ⁻⁹	5.68* 10 ⁻¹²	4.49* 10 ⁻¹²

TABLE II

COMPARATIVE RESULTS SHOWING POWER CONSUMPTION OF PROPOSED DESIGN AT DIFFERENT TECHNOLOGIES

AT VDDH=3V, VDDL=1V

Level shifter	180nm	90nm	45nm
Proposed level shifter	145.9* 10 ⁻⁹	126.7* 10 ⁻⁹	102.2* 10 ⁻⁹

TABLE-III

COMPARATIVE SIMULATION RESULTS SHOWING PROPAGATION DELAY AT DIFFERENT TECHNOLOGIES

VDDH= 1V, VDDL=0.2V

Level shifter	180nm	90nm	45nm
Proposed level shifter	3.23 *10 ⁻⁹	1.20*10 ⁻¹¹	5.79* 10 ⁻¹¹

TABLE IV

COMPARATIVE RESULTS SHOWING POWER CONSUMPTION OF PROPOSED DESIGN AT DIFFERENT TECHNOLOGIES

AT VDDH=1V, VDDL=0.2V

Level shifter	180nm	90nm	45nm
Proposed	98.0*	55.7*	45.65* 10 ⁷

level shifter	10^{-9}	10^{-11}	10^{-12}
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TABLE V

COMPARATIVE RESULTS SHOWING AREA OF PROPOSED DESIGN AT DIFFERENT TECHNOLOGIES

Level shifter	180nm	90nm	45nm
Proposed level shifter	120um ²	20um ²	9um ²

B. Multi-Supply design

Fig 8 and 9 shows the simulated waveform for half-adder and D-Flip flop. In Fig 8, the two inputs to half-adder are A and B. The operating voltage of half-adder is 1v so we get output SUM and CARRY in 1v supply. When both the inputs are high, we get CARRY as high. For unequal input bits the SUM is high. In Fig 9, input is applied at D and clock pulse is applied at CLK and output is seen. The output is obtained at Q which is similar to the input signal with some delay.

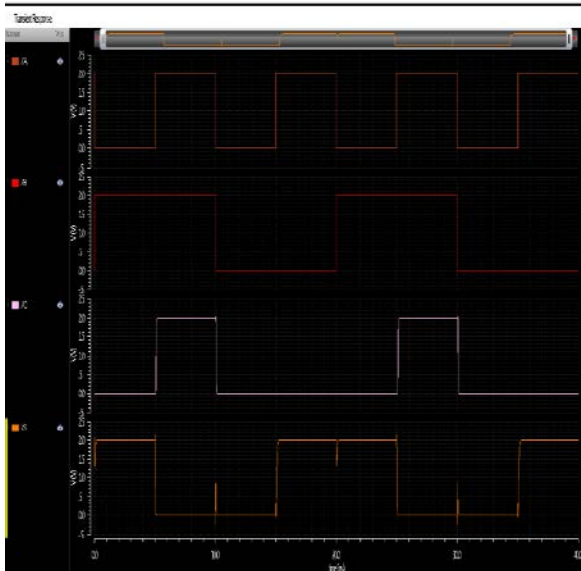


Fig 8. Simulated waveform of Half-adder

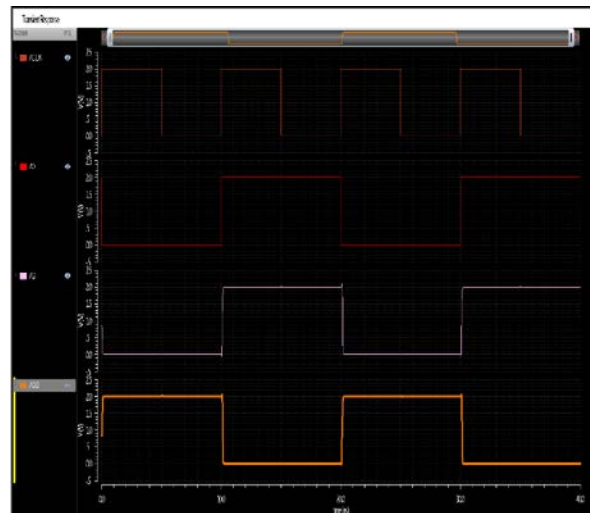


Fig 9. Simulated waveform of D-Flip flop

Fig.10 represents the simulated waveform for multi-supply design. The input signal is applied to half-adder, its output is applied to voltage level shifter for voltage level shifting. The output from the level shifter is again applied to D-Flip flop.

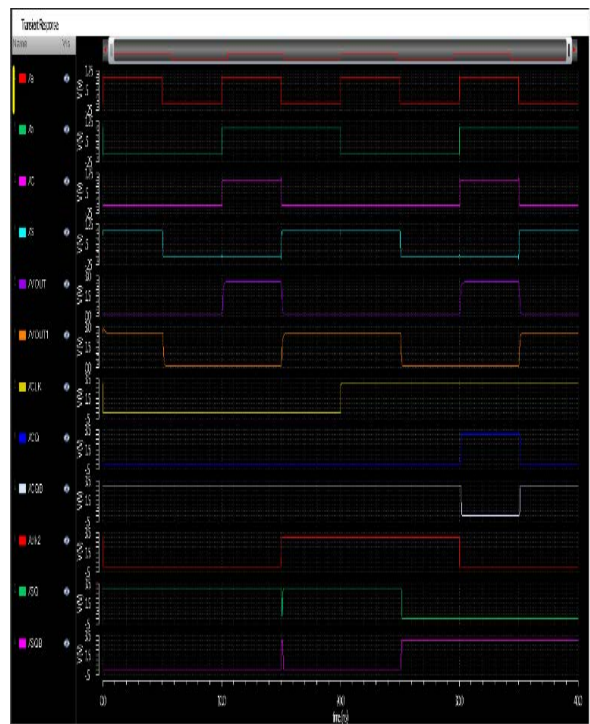


Fig 10. Simulated waveform for multi-supply design

IV . CONCLUSION

The proposed voltage level shifter is able to convert one voltage range to the other. As, voltage level shifter is a circuit which is used as a intermediate between blocks with different supply voltages. The efficiency of proposed level shifter is

verified at 180nm, 90nm and 45nm technologies in Cadence virtuoso simulator. Application of voltage level shifter is also presented in this paper, which explores the efficiency of level shifter.

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