Design and Development of Verification Environment to Verify GPIO Core using UVM

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Abstract- The GPIO core design provides a general purpose input/output interface to a 32-bit On-Chip Peripheral Bus (OPB). This GPIO core requires simple output and/or input software controlled signals and implements the functions that are not implemented using dedicated controllers in the system. Almost all FPGA boards contain GPIO peripheral. In this project we are atomizing the functions of the GPIO core by writing the code in VERILOG and simulating it in QUESTASIM. In this project we verify the all functions of GPIO core by writing verification code in UVM with different test cases. The functional and code coverage and functional verification of the GPIO RTL design is carried out for the better optimum design.

Index Terms- GPIO, OPB, QUESTASIM, XILINX ISE, Verilog, UVM, Coverage, FPGA

I. INTRODUCTION

The General purpose input/output IP core is user-selectable or user-programmable general-purpose Input/output controller. It is mainly used for implementation of functions that are not implemented with help of dedicated controllers in a system and require simple output and input software controlled or programmable signals.

The General Purpose IO module is part of Inicore's IP module family. This general purpose input/output controller gives some unique features that ease system integration and use. Each General Purpose IO port can be configured for output input or bypass mode. In one set all output data can be access. Single or multiples bits can be cleared or set independently. Every General Purpose IO port can serve as an interrupt source and has its own configuration options: • Level sensitive, single edge triggered or level change • Active low or high respectively positive edge or negative edge. • Individual interrupt enable register and status flags. The GPIO core provides several synthesis options to ease the system integration and minimize the gate count: •CPU bus width is selectable: default options are 8/16/32-bit • Selectable number of General Purpose I/O ports • CPU read back enable

II. GPIO (GENERAL PURPOSE I/O)

General architecture of GP I/O IP core is consists of four main building blocks:
• APB interface
• GP I/O registers
• Auxiliary inputs
• Interface to external I/O cells and pads

A. Architecture of GPIO

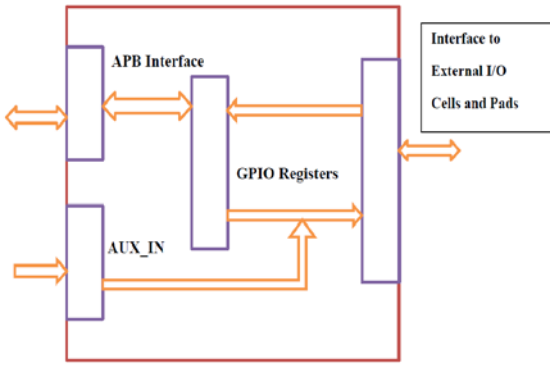


Fig.1 Architecture of GPIO

i. **Clocks:** The GP I/O core has two clock domains. All registers are in system clock domain except RGPIO_IN. The register RGPIO_IN can be clocked by external clock or by system clock.

ii. **APB Interface:** APB(Advanced Peripheral Bus) interface connects GP I/O core to the host system. The implementation implements a 32-bit bus width and does not support other bus widths.

iii. **GPIO Registers:** The GP I/O IP Core has several software accessible or programmable registers. Most registers have the same width as number of general-purpose I/O signals and they can be from 1 – 32 bits. The host through these registers programs type and operation of each general-purpose I/O signal or three-state outputs, appropriate open drain or three-state I/O cells must be used. Part of external interface is also ECLK register. It can be used to register inputs based on external clock reference. General-purpose inputs can generate interrupts so that software does not have to be in poll mode all the time when sampling inputs. Switching output drivers into open-drain or three-state mode will disable general-purpose outputs. To lower number of pins of the chip, other on-chip peripherals can be multiplexed together with the GPIO pins. For this purpose, auxiliary inputs can be multiplexed on general-purpose outputs.

iv. **Auxiliary Inputs:** The auxiliary inputs can bypass RGPIO_OUT outputs based on programming of RPGIO_AUX register. Auxiliary inputs are used to multiplex other on-chip peripherals on GPIO pins.

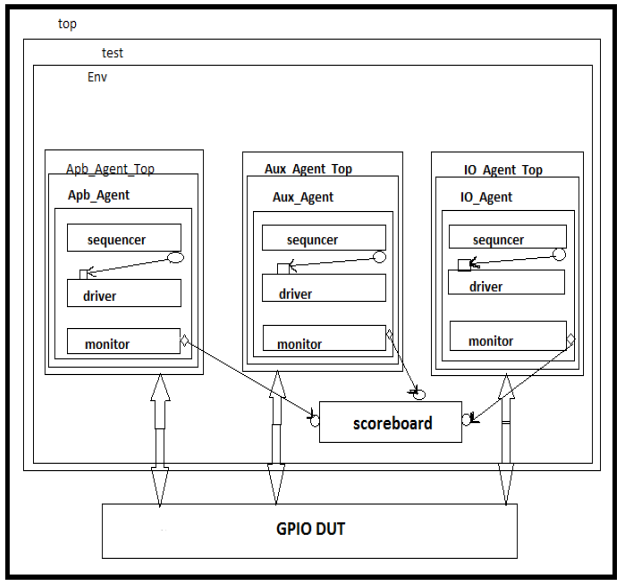
v. Interface to External I/O Cells and Pads: External interface connects GPIO core to external I/O ring cells and pads. To support open-drain or three-state outputs, appropriate open-drain or three-state I/O cells must be used. Part of external interface is also ECLK signal. It can be used to register inputs based on external clock reference.

III. UNIVERSAL VERIFICATION METHODOLOGY

The UVM (Universal Verification Methodology) was introduced in December 2009, by a technical Sub committee of Accellera. UVM uses Open Verification Methodology as its foundation. Accellera released version UVM 1.0 EA on May 17, 2010.UVM Class Library provides the building blocks needed to quickly develop well-constructed and reusable verification components and test environments. It uses system Verilog as its language. All three of the simulation vendors (Synopsys, Cadence and Mentor) support UVM today which was not the case with other verification methodology. Today, more and more logic is being integrated on the single chip so verification of it is a very challenging task. More than 70 percent of the time is spent on the verification of the chip. So it is a need of an hour to have a common verification methodology that provides the base classes and framework to construct robust and reusable verification environment. UVM provides that.

In this paper, all the terminology related to UVM is introduced along with the sample example. In first phase uvm components are introduced. In second phase some of the features related to UVM are introduced and in final phase small environment is built using UVM from the scratch.

IV. UVM TESTBENCH ARCHITECTURE



The following subsections describe the components of a verification component.

- Data Item (Transaction)
- Driver (BFM)
- Sequencer
- Monitor
- Agent
- Environment

- **Data Item (Transaction)**

Data item are basically the input to the device under test. All the transfer done between different verification components in UVM is done through transaction object. Networking packets, instructions for processor are some examples of transactions. From the top level test many data items are generated and applied to the dut so by intelligently randomizing the data items object we can check corner cases and Maximize the coverage on the device under test.

- **Driver (BFM)**

Driver as the name suggest, drive the dut signals. It basically receives the transaction object from the sequencer and converts it in to the pin level activity. So for example it can generate read or write signal, write address and data to be transferred. It is the active part of the verification logic.

- **Sequencer**

Sequencer is the component on which the sequences will run. The dut needs to be applied a sequence of transaction to test its behaviour. So sequence of transaction is generated and it is applied to driver whenever it demands by the sequencer.

- **Monitor**

A monitor is the passive element of the verification environment. It just sample the dut signal from the interface but does not drive them. It collect the pin information, package it in form of a packet and then transfer it to scoreboard or other components for coverage information.

- **Agent**

Agent is basically a container. It contains driver, monitor and sequencer. Driver and sequencer are connected in agent. Agent has two modes of operation: passive and active. In active mode it drives the signal to the dut. So driver and sequencer are instantiated in active mode. In passive mode it just sample the dut signals does not drive them. So only monitor is instantiated in passive mode. Normally there is one agent per interface like AHB or APB.

- **Scoreboard:**

Scoreboard is a verification component that checks the response from the dut against the expected response. So it keeps track of how many times the response matched with the expected response and how many time it failed.

- **Environment**

Environment is at the top of the test bench architecture, it will contain one or more agents depend on design. If more than one agents are there then it will be connected in this component. Agents are also connected to other components like scoreboard in this component.

V. RESULTS AND DISCUSSION

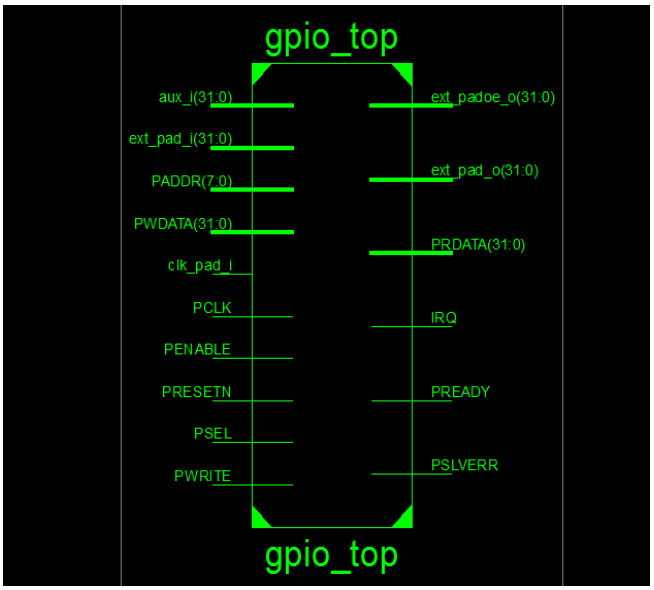


Fig 2. GPIO Schematic Diagram from Synthesis

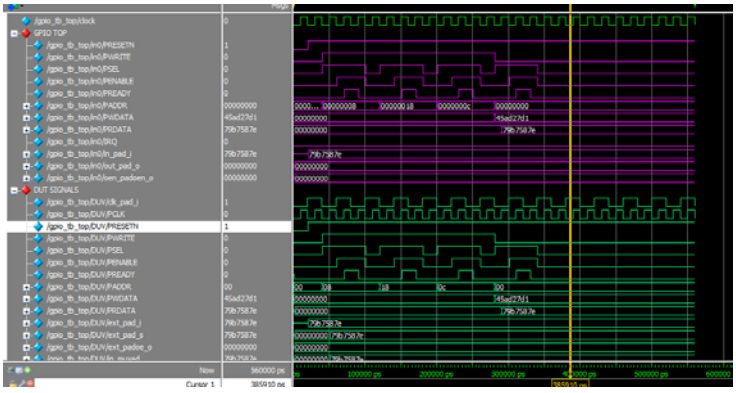


Fig 3. simulation showing GPIO Functional Verification for write operation

The GP I/O is carried out for the functional verification using the UVM technique for both the read and write operation. The functional verification is of the RTL design is of the GPIO is yields the complete code and functional coverage.

Functional Verification of GPIO Core Using UVM

As verification methodology plays a important phase in the circuit design. The read operation of the GPIO is carried out in XILINX for RTL design and the verification methodology is carried out using Questasim 10.0b. The design is carried out using in HDL and the verification is carried out in UVM. The GPIO is set up as DUT for the functional verification and the code coverage is obtained for 100%.

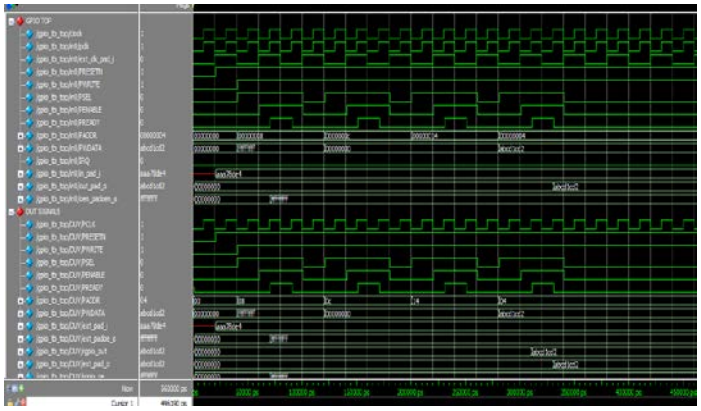
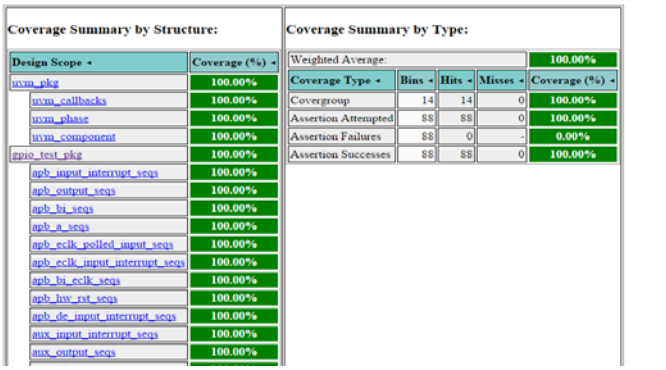


Fig 4. simulation showing GPIO Functional Verification for read operation.

VI. COVERAGE REPORT



Coverage Summary by Structure:

Design Scope	Coverage (%)
uvm_pkg	100.00%
uvm_callbacks	100.00%
uvm_phase	100.00%
uvm_component	100.00%
gpio_test_pkg	100.00%
apb_input_interrupt_seqs	100.00%
apb_output_seqs	100.00%
apb_bi_seqs	100.00%
apb_a_seqs	100.00%
apb_eclk_polled_input_seqs	100.00%
apb_eclk_input_interrupt_seqs	100.00%
apb_bi_eclk_seqs	100.00%
apb_hw_rst_seqs	100.00%
apb_de_input_interrupt_seqs	100.00%
aux_input_interrupt_seqs	100.00%
aux_output_seqs	100.00%

Coverage Summary by Type:

Weighted Average:				100.00%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Covergroup	14	14	0	100.00%
Assertion Attempted	$$	$$	0	100.00%
Assertion Failures	$$	0	-	0.00%
Assertion Successes	$$	$$	0	100.00%

Fig 5 Functional code coverage of GPIO

VII. CONCLUSION

In this we have designed and verified the GPIO core using Verilog and UVM technique using Questasim. The code coverage is obtained for the RTL design and 100% code coverage and functional coverage is extracted. This methodology provides the complete coverage of the RTL design so as to acquire the fault free Protocol design of GPIO. So that can be implemented in real time systems. This can be further implemented for the ASIC implementation and SOC Applications.

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