SDRAM Controller Based Vedic Multiplier in DWT Processor for Video Processing

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Abstract- Real time video processing has been the subject of interest for research work in last decade. Image and video processing technique are computationally demanding for various applications in various domains. Due to overwhelming demand we have focused on designing and implementing this new architecture which is effective. This paper we have focused on designing a DWT VEDIC processor which has a special SDRAM controller which takes care of this real time video processing. The design here is focused on real time DWT video compression and implementing the design on a Spartan 6 Altys FPGA board. Real time video applications have been implemented in the architecture with various results are projected to demonstrate its applicability and flexibility.

Index Terms- DWT, DCT, SDRAM.

I. INTRODUCTION

Discrete wavelet transform (DWT) decomposes images into multiple sub bands of low and high frequency component. This encoding of sub band components leads to compression of image and video .Image compression finds application in every discipline such as entertainment, medical, defence, industrial and commercial sectors. Thus the core of compression unit is DWT.DWT has lot of computational mathematical operations which are very intensive operations which consumes lot of time and power .Our focus is on design of SDRAM controller which controls data movement in DWT computation and to increase the performance of DWT Processor we are designing and implementing a 16*16 vedic multiplier in the DWT processing unit. This architecture has greatly reduce the power consumption of the circuit and at the same time increase the speed of operation of processing unit. The rapid increase in packing density, clocking frequency and computational power of an embedded system in general has inevitably resulted in rise in power consumption .For many years to come, miniaturization of size of devices together with the search of various architectures for low power and voltage requirement will continue. The work explores the new DWT architecture with Vedic multipliers incorporated in designing the hardware and determining its power consumption.

II. SYNCHRONOUS CONTROLLER

The usual memory hierarchy of a FPGA includes the data path, Main Memory Controller (MMC) and Local Memory Controller (LMC) as shown in the below figure1.The MMC will control the SDRAM (Synchronous Dynamic Random Access Memory) and generates the burst signals for the remaining units of the device. The LMC controls the data path and waits for the burst signals from the MMC. The main aim of our paper is to design Synchronous Ram Controller which will help to improve the performance matrix of the Vedic multiplier which will act as one of the component inside the DWT processor.
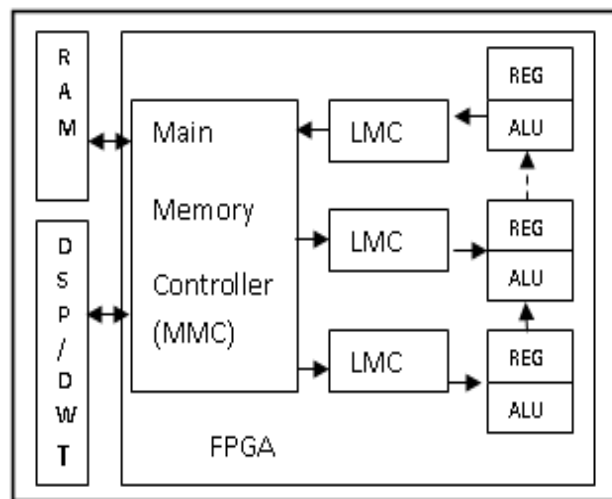

Fig 3.1 Architecture of MAC Unit in a processor.

III. MULTIPLY AND ACCUMULATE UNIT

In most of the digital signal processing units the critical operations involved are comprised of many multiplications and accumulations. There for the key focus is to increase the speed of any digital signal processing unit. In this regard our focus is to use Vedic mathematics and design a high speed Multiplier-Accumulator Unit. These days computers contains dedicated video graphics unit similarly computers may contain dedicated MAC unit. The generalised structure of MAC unit is shown in the figure 3.1 below. The MAC unit consists of a multiplier implemented in combinational logic followed by an adder and an accumulator registers which stores when clocked. The output of the register is fed back to one input of the adder, so that on each clock, the output of the multiplier is added to the register. Combinational multipliers require a large amount of logic, but can compute a product much more quickly than the shift and add based multiplier.
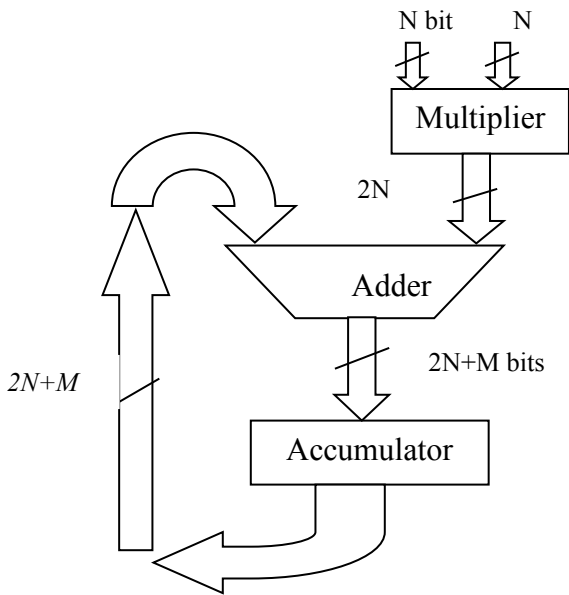
Fig 3.1 Architecture of MAC Unit in a processor

IV. 16*16 VEDIC MULTIPLIER Architecture for DWT processor

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. like power This Vedic algorithm through which DWT video compression architecture is build using DSP Slices available in MATLAB system generator helps us to make various analysis. Some analysis performed that can be constantly checked for various parameters consumed, processing time and overall performance can be evaluated. This algorithm is implemented on a Spartan 6 FPGA.

Fig4.1 Architecture of 16*16 Vedic Multiplier

Architecture of a 16*16 Vedic Multiplier is structured based on building basic blocks. The individual 4*4 Vedic

multiplier blocks is implemented using Verilog hardware description language. Once we have verified the functionality of 4* 4 Vedic multiplier, we have designed 8*8 Vedic multiplier. In the above architecture we have four 8*8 Vedic multipliers and three full adders. Instead of three full adders we can go to latest adders like carry save or carry select adders. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. Delay in Vedic multiplier for 16 x 16 bit number is 32 ns while the delay in Booth and Array multiplier are 37 ns and 43 ns respectively [1]. The functionality of each block is verified using Xilinx ISE 14.2

V.   DIGITAL VIDEO PROCESSING

Digital video processing is the technology that is almost evergreen domain of research which is also the fastest growing technology this century and, therefore, it poses tremendous challenges to the engineering community. Faster additions and multiplications are of extreme importance in DSP for convolution, discrete Fourier transforms digital filters and Discrete Wavelet Transforms etc. The core computing process is always a multiplication routine therefore DSP engineers are constantly looking for new algorithm and architecture to improve performance of the system. Using this algorithm we can constantly design and implement it on suitable hardware.
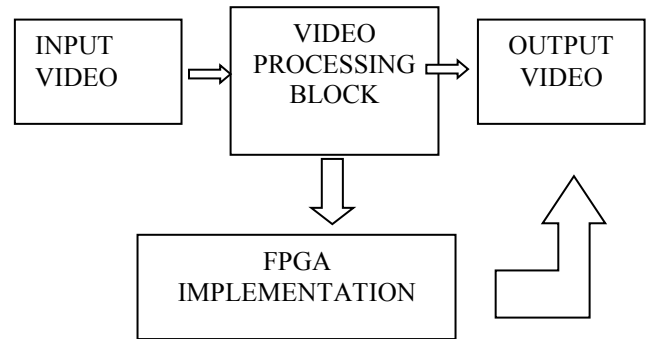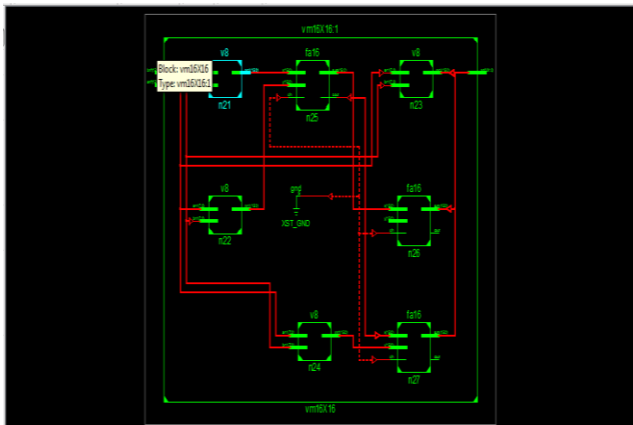

Fig 5.1 Block Diagram Approach

The block diagram shown in figure 5.1 gives the complete flow of digital video compression flow. The block diagram basically consists of an input block, processing block, output block and the entire video processing algorithm is implemented on desired FPGA implementation. Initially we have a video file which is to be processed is received from real time camera which feeds in the input video. This video is processed in the processing block. The main objective is to save the real time video for surveillance or any security measures in restricted areas. To save the video continuously it will tedious task as it consumes lot of memory space. Thus to reduce the memory space utility, we compress the real time video using DWT video compression technique. The major processing is done according to our algorithm then the video compressed will be displayed in output video file. This algorithm is designed in MATLAB Simulink which is finally implemented on a FPGA with certain modifications in the MAC unit and controlling the processing using SDRAM controller.

VI. VIDEO COMPRESSION USING DISCRETE WAVELET TRANSFORM

There are several technique can be used to compress image which are Discrete Cosine Transform (DCT) and Discrete Wavelet Transform. DCT works by separating images into parts of differing frequencies. During the step quantization, where part of compression usually occurs, the less important of frequencies are discarded, hence the use of the term of "lossy". Then, only the most important frequencies are used to retrieve the image compression process. As a result, the reconstruct image contains some distortion but this level of distortion can be adjusted during the compression stage. There is some loss of quality in the reconstructed image below; it is clearly recognizable, even though almost 85% of the DCT coefficients were discarded. Images contain large amounts of information that requires large transmission bandwidths, much storage space and long transmission times. Therefore it is crucial to compress the image by storing only the essential information needed to reconstruct the image. An image can be thought of as a matrix of pixel values.

In order to compress the image, redundancies must be exploited, for example, areas where there is little or no change between pixel values. Therefore large redundancies occur in the images which having large area of uniform color and conversely images that have frequent and large changes in color will be less redundant and harder to compress.

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VII. SUB BAND CODING

A signal is passed through a series of filters to calculate DWT. Procedure starts by passing this signal sequence through a half band digital low pass filter with impulse response h(n).Filtering of a signal is numerically equal to convolution of the tile signal with impulse response of the filter.

$$x[n] * h[n] = \sum_k^\infty = -\infty \, x[k].h[n-k] \qquad (7.1)$$

A half band low pass filter removes all frequencies that are above half of the highest frequency in the tile signal. Then the signal is passed through high pass filter. The two filters are related to each other as

$$h[L-1-n] = (-1)^n \, g(n) \qquad (7.2)$$

Filters satisfying this condition are known as Quadrature mirror filters. After filtering half of the samples can be eliminated since the signal now has the highest frequency as half of the original frequency. The signal can therefore be sub sampled by 2, simply by discarding every other sample. This constitutes 1 level of decomposition and can mathematically be expressed as

$$Y1[n] = \sum_k^\infty = -\infty \, x[k].h[2n-k] \qquad (7.3)$$

$$Y2[n] = \sum_k^\infty = -\infty \, x[k].g[2n+1-k] \qquad (7.4)$$

Where Y1 [n] and Y2 [n] are the outputs of low pass and high pass filters, respectively after sub sampling by 2. This decomposition halves the time resolution since only half the number of sample now characterizes the whole signal. Frequency resolution has doubled because each output has half the frequency band of the input. This process is called as sub band coding. It can be repeated further to increase the frequency resolution as shown by the filter bank.
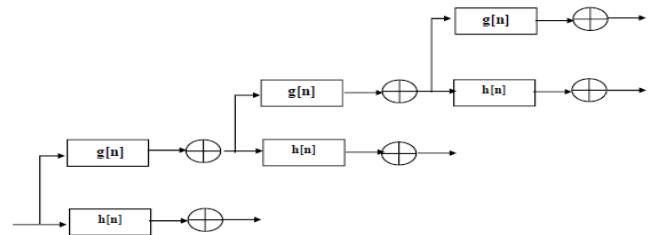

Fig 7.1 Filter Bank

VIII. SYNCHRONOUS RAM CONTROLLER INTERFACES

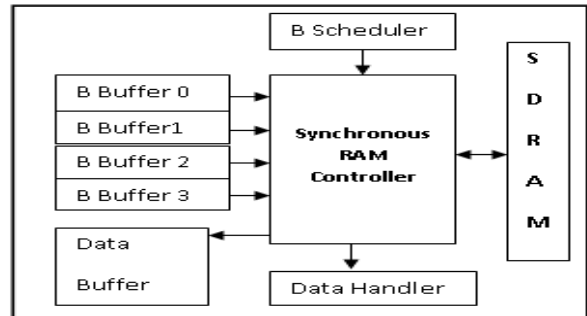As shown in the figure 8.1 is the basic interfaces of a Synchronous ram controller.

Fig 8.1 Interfaces of Synchronous Ram Controller

a. Bank Buffers: Each bank buffer will intern refer to one of the banks of SDRAM. It receives signals from SDRAMC.

b. Bank Scheduler: The bank scheduler will select a particular bank depending on the priorities being assigned.

c. Data Handler: The read and write signals are being controlled by SDRAMC by sending appropriate signals to the data handler.

d. Data Buffer: It receives two signals from SDRAMC and operates accordingly.

e. SDRAM: Here the term SDRAM refers to CMOS high speed Synchronous Dynamic Random Access memory with R rows columns of B bits each. Internally it has

been organized as quad bank DRAM with synchronous interface.
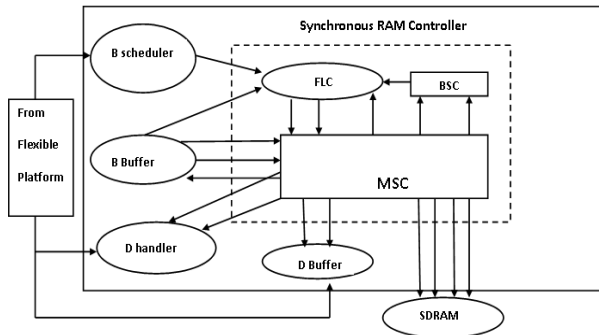
IX.   SYNCRONOUS RAMCONTROLLER ARCHITECTURE

Fig 8.2. The Synchronous RAM Controller Architecture

The above Synchronous RAM Controller Architecture has following modules

Flexible Logic Controller Module: The bank scheduler sets the priority and the bank buffers send the request then depending upon the priority of the bank buffer a particular bank will be selected and its number will be sent to the MSC module.

The Bank State Controller (BSC) Module: The requested bank number and its actual request either read or write will be received by this module by the MSC module to start its own state machine.

The Main State Controller (MSC) module: This module will receive the request either read or write the bank number and then start its own state machine and finally creates proper SDRAM signals such as CAS, RAS, WE, address lines etc
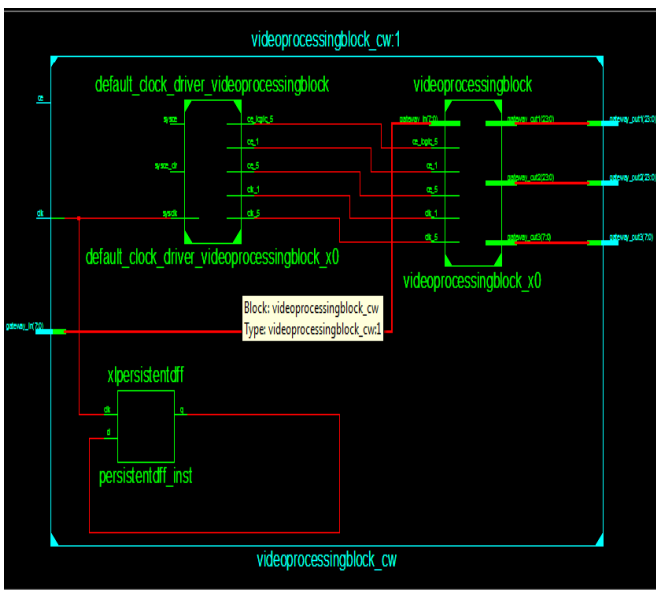
X.   RESULTS

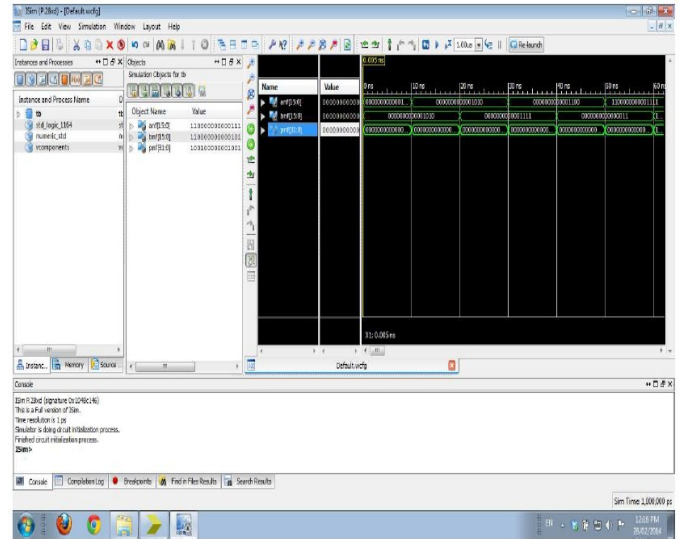**Fig 9.1 RTL schematic Results of 16*16 Vedic Multiplier**

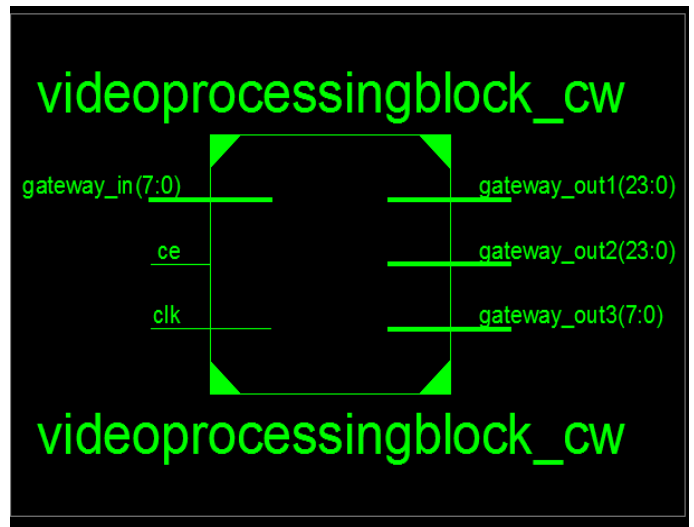**Fig 9.2Simulation Results of 16*16 Vedic Multiplier**

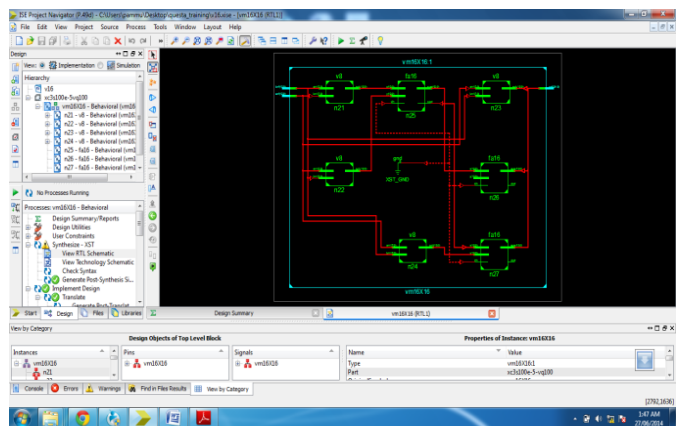**Fig 9.3Simulation Result of DWT Video Processing Block**

Fig 9.4 RTL results of DWT Video Processing Block

Fig 9.5 RTL MSC schematic

Fig 9.6 Simulation results of MSC simulation

Fig 9.7 Implementation of Algorithm on FPGA
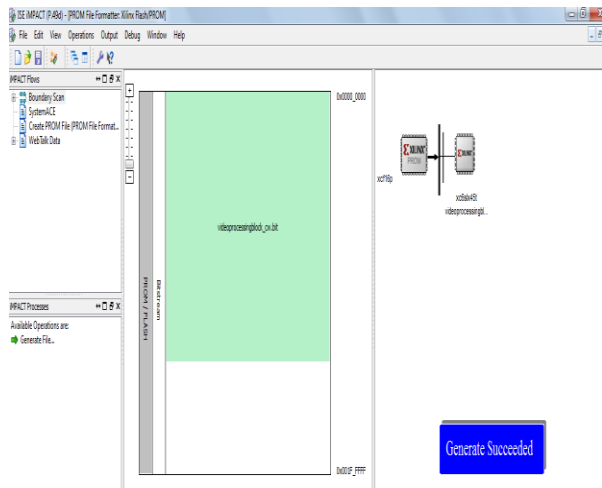
XI.   CONCLUSION

A real-time video processing algorithms with new architecture was implemented on FPGA. Implementation of these types algorithms on a FPGAs have lot of practical application at the same time there will be issues large memory requirement and embedded multipliers which process faster. Here in order to resolve the above complexity a new architecture with SDRAM controller helps us to maintain the large memory used for processing. We can finally conclude that implementing DWT video compressing algorithm with MAC unit compromising of 16* 16 Vedic Multiplier is implemented successfully. The algorithm created in Xilinx system generator and by using JTAG it is successfully implemented on Spartan6-LX45 FPGA board.

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