Reduction of THD in Diode Clamped Multilevel Inverter employing SPWM technique

M.Kedareswari

B-tech (EEE), M-tech (PEED), Email:kedar_eee@yahoo.co.in
EEE Department, GNITS for women, Hyderabad, India

***Abstract*—** Conventional two-level pulse width modulation (PWM) inverters generate high dv/dt, high frequency common mode voltages and introduces harmonics which is very harmful in electric drives applications. It may damage motor bearings, conducted electromagnetic interferences, and malfunctioning of electronic equipments. Multilevel inverter (MLI) technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Neutral-point-clamped (NPC) inverters are the most widely used topology of multilevel inverters in high-power applications (several megawatts). This paper presents the most relevant control and modulation method developed for inverters to reduce total harmonic distortion (THD): multilevel sinusoidal pulse width modulation (SPWM). More relevant applications of these converters are laminators, conveyor belts, and unified power-flow controllers. Simulation results obtained in Matlab/Simulink confirms the effectiveness with negligible THD.

Index Terms- PWM, Multilevel Inverter, Neutral Point Clamped Inverter, Total Harmonic Distortion, SPWM.

I. INTRODUCTION

Multilevel Inverters have gained much attention in the field of the medium voltage and high power applications because of their many advantages, such as their low voltage stress on power switches, low harmonic and EMI output. At present, there are three basic multilevel inverter topologies: diode-clamped multilevel inverter (DCMI), flying capacitor multilevel inverter (FCMI) and multi-module cascaded inverter (MMCI). These are shown below in Fig. 1[1].

For research on multi level inverter topologies, a preferred multilevel inverter topology shall have the following characteristics:

1) The level is easy to extend.

2) When the number of levels is high enough, the harmonic content is low.

3) There is no need for filters.

4) Inverter efficiency is high because all devices are switched at the fundamental frequency.

5) The control method is simple.

Performance of multilevel inverters depends on the PWM converter topology. In two-level or multilevel

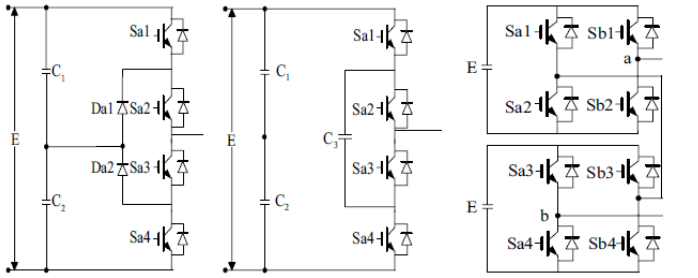


Fig. 1. Multilevel inverter topologies

inverters, there is only one turn-on, turn-off per device per cycle. With these converters, the ac output voltage can be controlled, by varying the width of the voltage pulses, and/or the amplitude of the dc bus voltage. Another approach is to have multiple pulses per half-cycle, and then vary the width of the pulses to vary the amplitude of the ac voltage. The principle reason for doing so is to be able to vary the ac output voltage and to reduce the low-order harmonics.

PWM switching strategies not only addresses the primary issues viz, less THD, effective dc bus utilization etc but also take care of secondary issues like EMI reduction, switching loss, better spreading of harmonics over the spectrum.

Among various modulation techniques [1] for a multilevel inverter, sin-triangle pulse width modulation (SPWM) is an attractive candidate due to the following merits. It proportionally varies the width of each pulse to the amplitude of a sine wave evaluated at the center of the same pulse [2]. It is suitable for MATLAB/SIMULINK implementation.

In sin-triangle PWM, three phase reference modulating signals are compared against a common triangular carrier to generate PWM pulses for the three phases. Reduction of total harmonics distortion (THD) of inverter output voltage and the distortion seamless when level of diode-clamped inverter has got increased is the main advantage of the proposed control method.

II. VOLTAGE SOURCE INVERTERS

A voltage source inverter consists of a turn-off device connected in anti-parallel with a diode which has lowest reverse leakage current with the anode of turn-off device connected to the positive side of DC side. In inverter action, turn-off device will conduct and current / power flows from DC side to AC side. In rectifier action, the diode will conduct and current / power flows from AC to DC side. Under inverter operation, current and voltage will be of opposite polarity and under rectifier operation

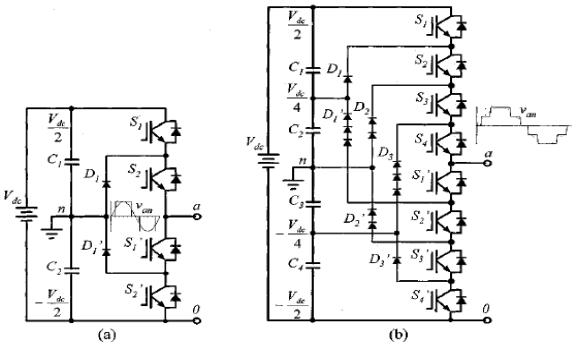
they will be of same polarity. The compensation is applied at mid-point to improve the voltage regulation. For radial lines, shunt compensation is applied at the end of line to prevent voltage instability, for dynamic voltage control, to increase transient stability and for damping of power oscillations. Mid-point of transmission line is the best location for compensator because the voltage sag for uncompensated line is maximum at the mid-point. Also, the compensation at mid-point breaks the line into equal segments, for each of which, the maximum transmittable power is the same.

III. INVERTER TOPOLOGY

Neutral Point-Clamped Inverter:

A three-level diode-clamped inverter is shown in Fig. 2(a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors *n* can be defined as the neutral point. The output voltage v_{an} has three states: $V_{dc}/2$, *0*, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the *0* level, S_2 and S_1' need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across *a* and *0* is V_{dc} i.e., $v_{a0} = V_{dc}$. In this case, D_1' balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is the voltage across C_2, which is V_{dc} /2. If the output is removed out between *a* and *0*, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc} , $V_{dc}/2$, and *0*.



(a) (b)

Fig. 2. Diode-clamped multilevel inverter circuit topologies.
(a) Three-level. (b) Five-level.

Considering that *m* is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load *k* is

$$k = 2m+1 \qquad (1)$$

and the number of steps *p* in the phase voltage of a three-phase load in wye connection is

$$p = 2k - 1. \qquad (2)$$

The term multilevel starts with the three-level inverter introduced by Nabae *et al.* [3]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

Fig. 2(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point *n* is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across *a* and *n*.

1) For voltage level $V_{an} = V_{dc}/2$, turn on all upper switches $S_1 – S_4$.

2) For voltage level $V_{an} = V_{dc}/4$, turn on three upper switches $S_2 – S_4$ and one lower switch S_1'.

3) For voltage level $V_{an} = 0$, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'.

4) For voltage level $V_{an} = –V_{dc}/4$, turn on one upper switch and three lower switches $S_1' – S_3'$.

5) For voltage level $V_{an} = –V_{dc}/2$, turn on all lower switches $S_1' – S_4'$.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4').

TABLE I. SWITHCING STATES OF THE FIVE LEVEL INVERTER

Output	*Switch States*							
v_{a0}	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1= 0$	0	0	0	0	1	1	1	1

Although each active switching device is only required to block a voltage level of $V_{dc}/(m-1)$, the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1'of Fig. 2(b) as an example, when lower devices S_2' ~ S_4' are turned on, D_1' needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, D_2 and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be $(m-1) \times (m-2)$. This number represents a quadratic increase in *m*. When *m* is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

IV. CONTROL STRATEGY

In many industrial applications, to control of the output voltage of inverters is often necessary to cope with the variations of dc input voltage, to regulate of inverters and to satisfy the constant volts and frequency control requirement. There are various techniques to vary the inverter gain. The most efficient

method of controlling the gain and output voltage is to incorporate PWM control within the inverters.

The modulation methods used in multilevel inverters can be classified according to switching frequency [4], [5]. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform.

Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage [6].

V. PROPOSED TECHNIQUE

SPWM:

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals [7], [8], [9].

The sinusoidal PWM compares a high frequency triangular carrier with three sinusoidal reference signals, known as the modulating signals to generate the gating signals for the inverter switches. This is basically an analog domain technique and is commonly used in power conversion with both analog and digital implementation.

The smallest distortion is obtained when the carriers are shifted by an angle of $\theta = 360°/Nc = 120°$. A very common practice in industrial applications for the multilevel inverter is the injection of a third harmonic in each cell to increase the output voltage [6], [10]. Another advantageous feature of multilevel SPWM is that the effective switching frequency of the load voltage is three (N_C=3) times the switching frequency of each cell, as determined by its carrier signal. This property allows a reduction in the switching frequency of each cell, thus reducing the switching losses.

Proposed SPWM for NPC Multilevel Inverter:

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other. The SPWM technique, for multilevel inverters, involves comparing the reference phase voltage signals with a number of symmetrical level-shifted carrier waves for PWM generation [11]. It has been shown that for an n-level inverter, n-1 level-shifted carrier waves are required for comparison with the sinusoidal references [11].

When used for an NPCMLI with *n* number of voltage levels, *n-1* number of triangular carrier waves is used. These carrier waves have the same frequency and are arranged on top of each other, so that they together span from maximum output voltage to minimum output voltage [12]. When one carrier wave is crossed by the reference the output wave steps one level up or down with a switch transaction.

VI. SIMULATION RESULTS

To verify the proposed scheme, MATLAB/SIMULINK software is implemented. The experimental results are presented for different levels of NPCI using sinusoidal PWM technique. In SPWM control the pulse widths are generated by comparing a triangular reference signal with carrier sinusoidal signal. And these generated pulses are given for all switching devices of proposed inverter. DC voltage of the inverter for three level is *E=100V* and for five level *E=440V*. Fig 5.1 shows the reference signal is compared with two *(3-1)* carrier signals to generate three level output. Similarly Fig 5.4 shows the comparison with four *(5-1)* carrier signals to generate five level output. Fig. 5.2 illustrates the line voltage of NPC three level inverter with SPWM and Fig. 5.3 illustrates the THD spectrum of NPC three level inverter with SPWM. In this modulation technique the THD is *34.51%*. Fig. 5.5 illustrates the line voltage of NPC five level inverter with SPWM and Fig. 5.6 illustrates the THD spectrum of NPC five level inverter with SPWM. In this modulation technique the THD is *16.82%*.

The output voltage is closer to sinusoid and the THD values of line voltages also seamless as the level increases.

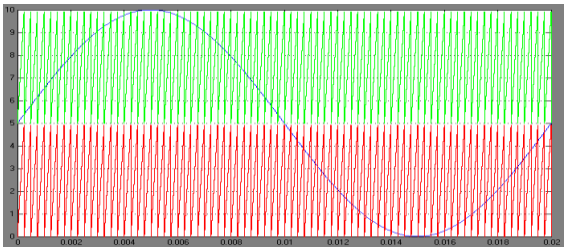


Fig. 5.1 The reference (cosine) and carrier waves (triangular) for a three-level NPCMLI with SPWM.

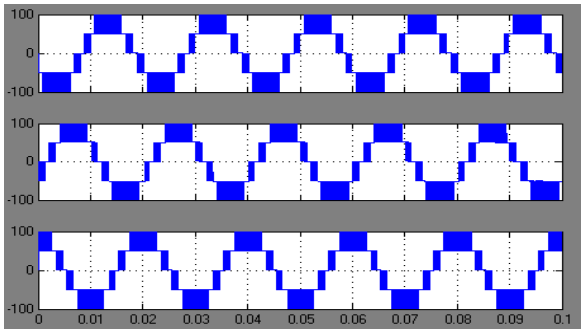


Fig. 5.2 The output voltage for a Three-level NPCMLI with SPWM.

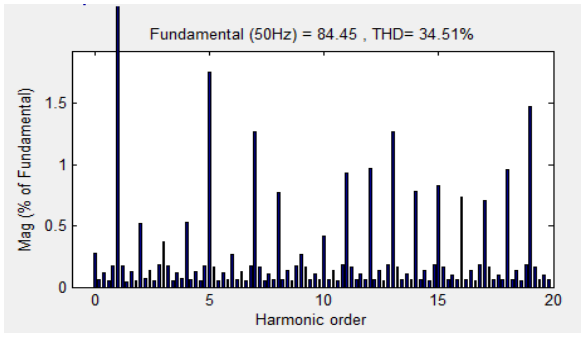


Fig. 5.3 THD spectrum for a three-level NPCMLI with SPWM

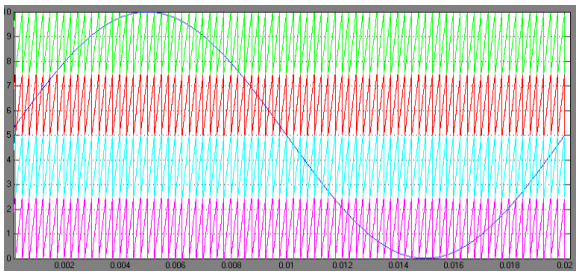


Fig. 5.4 The reference (cosine) and carrier waves (triangular) for a five-level NPCMLI with SPWM.

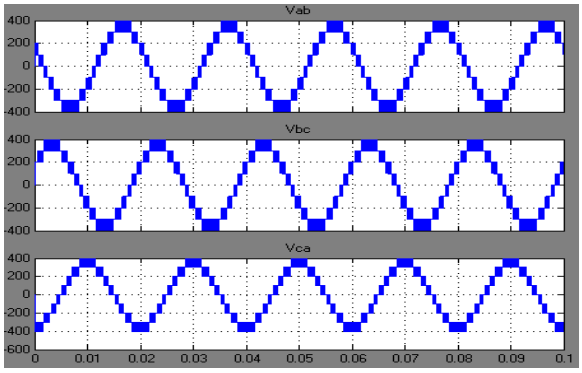


Fig. 5.5 The reference (cosine) and carrier waves (triangular) for a five-level NPCMLI with SPWM.

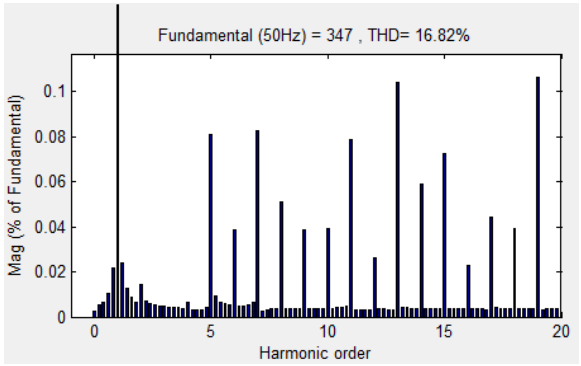


Fig. 5.6 THD spectrum for a three-level NPCMLI with SPWM

TABLE II. REDUCTION OF THD BY VARYING INVERTER LEVEL

Output Voltage level of NPCI	*THD*	*Fundamental Component*
Three Level	34.51%	84.45
Five Level	16.82%	347

VII. CONCLUSION

A classical SPWM technique is proposed for three-level and five-level NPC inverter. The main feature of the modulation scheme lies in its ability to eliminate the harmonics in the inverter output voltages. To assist the analysis and design of the classical scheme, the mechanism of the THD reduction with increase in level of inverter employing SPWM technique is discussed.

The harmonic content and THD of the inverter output voltage produced by the three and five levels are compared and it seamless for five level neutral point clamped inverter compared to three level NPCI. The proposed technique can be applied to any multilevel inverter configurations and we can generalize this method to any higher order inverters.

REFERENCES

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] T.Ohnishi and H.Okitsu, "A novel PWM technique for three-phase inverter/converter," *International Power Electronics Conference*, 1983, pp.384-395.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. Ind. Applicat.*, vol. IA-17, pp. 518–523, Sept./Oct. 1981.

[4] N. Celanovic and D. Boroyevic, "A fast space vector modulation algorithm for multilevel three-phase converters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Phoenix, AZ, Oct. 1999, pp. 1173–1177.

[5] J. Rodríguez, P. Correa, and L. Morán, "A vector control technique for medium voltage multilevel inverters," in *Proc. IEEE APEC*, Anaheim, CA, Mar. 2001, pp. 173–178.

[6] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 202–208, Jan./Feb. 1997.

[7] L. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 1098–1107, Sept./Oct. 1999.

[8] B. N. Mwinyiwiwa, Z.Wolanski, and B. T. Ooi, "Microprocessor implemented SPWM for multiconverters with phase-shifted triangle carriers," in *Conf. Rec. IEEE-IAS Annu. Meeting*, NewOrleans, LA, Oct. 1997, pp. 1542–1549.

[9] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE PESC'98*, Fukuoka, Japan, May 1998, pp. 172–178.

[10] W. A. Hill and C. D. Harbourt, "Performance of medium voltage multilevel inverters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Pheonix, AZ, Oct. 1999, pp. 1186–1192.

[11] Carrara, G.,Gardella, S.G., Archesoni,M., Salutari, R., and Sciutto, G.: 'A new multi-level PWM method: A theoretical analysis', IEEE Trans. Power Electron., 1992, 7, (3), pp. 497–505

[12] McGrath, B.P.; Holmes, D.G.; "Multicarrier PWM strategies for multilevel inverters," *Industrial Electronics, IEEE Transactions on*, vol.49, no.4, pp. 858-867, Aug 2002 doi: 10.1109/TIE.2002.801073