Comparative Analysis of Existing Clock Gating ALU

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***Abstract*- Digital world multimedia and DSP based applications work on certain clock pulse and as we know, clock signal. The clock signal consumes maximum applied power and this is a major drawback in digital synchronous circuit. Clock gating is an important technique for reducing the dynamic power losses in digital circuits. In a typical synchronous circuit such as the general purpose ALU multimedia, only a portion of the operating circuit is active at any given point of time and the other circuits remain inactive. Hence, by making the other circuits inactive selectively, the unnecessary power dissipation can be avoided. By using this approach dynamic power losses can therefore be minimized. The new proposed work implements another gated clock technique by using T& D flip flop and making comparative analysis between various gating clock techniques. This approach of minimizing dynamic power is implemented by using Artix-7 and Spartan-6 with 45nm and 40nm FPGA technology respectively.**

***Index Terms*-** DSP based application, dynamic, clock gating, ALU multimedia

I. INTRODUCTION

Now-a-days, the power-sensitive or low power dissipation devices are required and the demand of these types of devices has grown significantly. This tremendous demand mainly initiated due to the need for low power consumption and small size digital devices have aggressively dominated successive technology generations. The power has been continuously reduced by improving the implementation of technology and design. The power dissipation can reduced by use of integrating circuit (IC) .The circuit level as well as system level technology are also required to be improved for lower power dissipation. Further, the power dissipation can be reduced by applying the scaled voltage. But the scaled voltage supply limits the possibility of high performance. Hence, the scaling of supply voltage alone may not be sufficient to reduce the power dissipation, which is more important only for power-sensitive applications. Clock signal is main life line for digital circuit operation. Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems. Synchronization of signal is a major drawback in digital circuits which causes the dynamic power dissipation.

Traditionally, the demand for high performance was addressed by increasing clock frequencies with the help of technology scaling. Generally the dynamic power occurs due to clock synchronization and on-off operation of the clock signal. A very clear example of this trend is the recent move towards multi-core architectures for processors [1]. Thus innovative clocking techniques for decreasing the power consumption of the clock networks are required for future high performance and low power designs.

Electronic design is the software to design the electronics system the EDA, mostly used to print the CRT integrated circuit. The most important parameters are area, power, and performance. Area can be found in terms of gate count and transistor count and final chip area optimization is done with the help of positioning placement routing. The power optimization analysis which depends mainly on logic level area of the chip, routing cost and many more factors. Also the performance of the electronics system design depends upon gain logic levels, working frequencies and temperature. These parameter lies between 8 different abstraction levels of the design to make it optimal over the all reliable features on EDA tool which may or may not always be a practical solution. To reduce power consumption, to start the proper planning & register transistor (RTL) design in this paper, we use some stream techniques that can be used at the article coding stage that will consume less power than the other technique and keep the basic design unchanged.

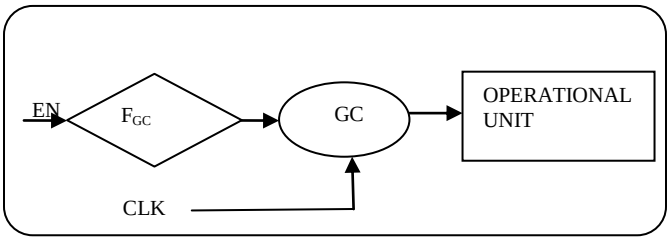

Fig.1 gated clock generation

This approach first presents review on various clock gating technique and also make a comparative analysis of those clock gating techniques on some synchronous digital device like ALU (Arithmetic logical unit). Also it will introduce a new clock gating approach that will have low dynamic power losses.

II. APPLICATIONS OF GATED CLOCK

1- All sequential circuit.
2- Memory processing
3- Registers & counters.
4- Data processing.
5- Arithmetic and logic units.

III. REVIEW CLOCK GATING

There are different types of clock gating techniques for implementation of gated clock.

1. AND GATES

Implementation of the Clock gating signal is done through the AND gate [6][9][13].The AND gated clock is latch free clock gated signal. As shown form the fig .1 the gated clock is applied to ALU with enable signal and operation select and the ALU perform selected operation.

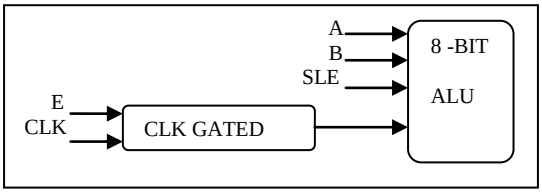

Fig.2 logic gate generate clock gating.

But gates based design suffer from the major problem in this technique as gated clock remain active till the enable signal remains active. When the enable goes to negative logic or 0, clock terminates and also glitches are introduced in gate or latch base gated clock signal.

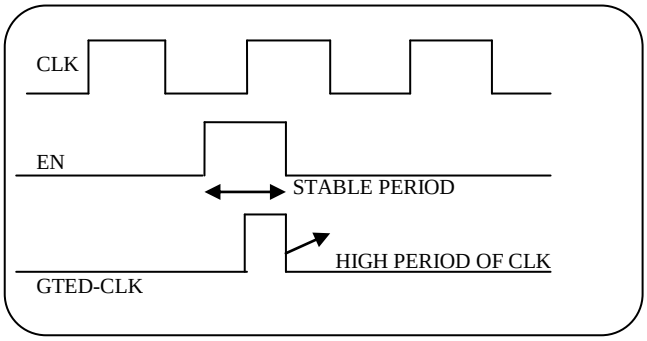

Fig.3 Wave form of latch free -GC

2. LATCH BASED CLOCK GATING

Latch based implementation overcome the glitch problem [11]. In the latch based gated clock the enable signal is not applied directly and not applied to gated clock generation device. The enable signal is applied through the latch. This approach reduces the glitch problem and reduces the unwanted transition of enable signal.

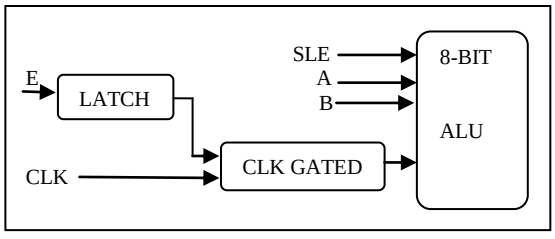

Fig.4 Latch based clock gating.

Fig . Show the wave form of latch based gated design in which the gated clock remain active till the EN remains in active high and have no transition in the gated clock. When the EN goes low the gated clock terminates after completing selected operation.

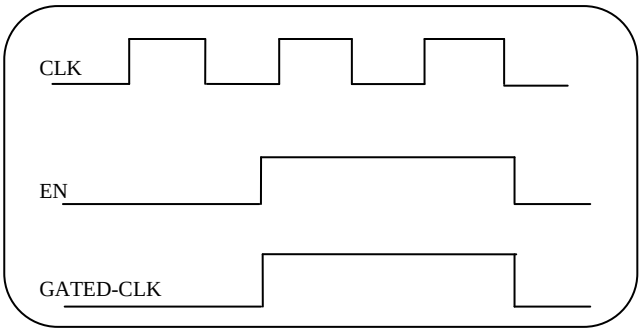

Fig.5 wave form of latch based design

3. MUX BASED CLOCK GATING

During implementation of multiplexer based clock gating [13][11] we take mux to close and open a feedback path around a basic D-type flip-flop. In this technique, the enable signal is used as control signal as shown in the figure. This is the reasonable choice because it is simple, robust, and compliant with the rules of synchronous design. It is a safe to use Multiplexer based process because it has number of good features but consumes more power due to multiplex per bit. This is because any toggling of the clock input of a disabled flip-flop amounts to wasting of energy in discharging and recharging the associated node capacitances for nothing. The capacitance of the CLK input is not the only contribution as any clock edge causes further nodes to toggle within the flip-flop itself [11].

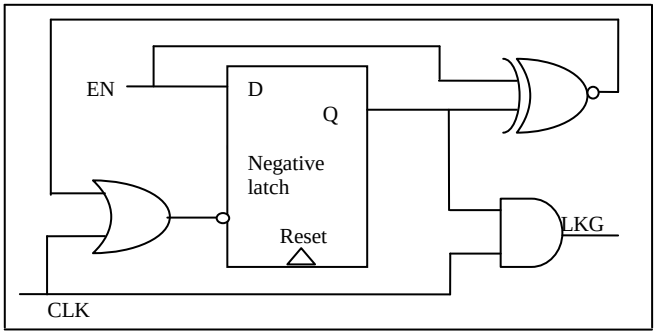

Fig.6 Multiplexer generated clock.

All the previous clock gating approaches face the problem of size meaning those approach which require less size and low power, there will be the issue of glitches and those approaches which have large size , face no glitches problem ,but these structures have increased static power dissipation problem. In all previous approaches only few approaches will reduce the clock power but still some are facing the problem of clock power consumption. In some previous architecture there was need of extra input and output pins. As we know for VLSI chip increase in input and output pins will increase the cost of the whole process.

4. *FLIP*–FLOP BASED GATED CLOCK

Flip flop based gated clock is developed on the phenomena of the latch [11][15][18].The positive and negative latch are used to generate flip flop based gated clock pulse. Here D flip flop used to generate gated clock flip flop has a good feature which is most effective to implement the gated clock. The D flip flop produce continuous logic1 in output by providing 1as an input and 0 logic at 0 input .The implemented gated clock is shown in figure.

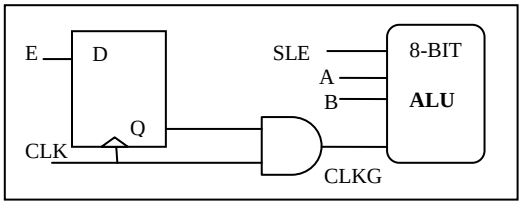

Fig.7 Flip flop based gated clock

IV. CONCLUSION

There are number of gated clock generation techniques that are implemented. But every process has some week point such as, in AND gate based clock gating design, there are glitches and clock dies before the life time .This glitch can be overcome by designing latch based gated clock.

Flip flop based gated clock has improved results but at the cost of size. In the new proposed work the gated clock is generated through the T and D flip flop and also makes comparison between various implementation techniques. T flip flop is used to generate gated clock because it has inverting property. The inverting property of the signal consumes less power than in the other techniques. T flip flop produce gated clock at 0 input . This is the most important parameter to reduce power consumption.

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