Future Generation Ultra Supercomputing 256 × 256 Bits Multiplier for Signed-Unsigned Number

Ravindra P Rajput *, M. N Shanmukha Swamy **

* Electronics and Communications Engineering, JSS Research Foundation, Mysore University, Mysore, Karnataka, India.
** Electronics and Communications Engineering, SJCE, Mysore, Karnataka, India.

   Abstract- With the future 1 nm Hybrid CMOS technology, we proposed the Future Generation Ultra Supercomputing 256 × 256 Bits Multiplier for Signed-Unsigned Number. The Hybrid CMOS consists of the CMOS and Complimentary Pass Transistor Logic (CPTL). With the 1 nm future technology the various parameters predicted are the critical path delay of 0.1 ns (10 GHz), chip area of 136.23 μm^2 and the power dissipation of 1171.4 μW.

   Index Terms- MMBE, CPTL, PPG, VCA, PPRT, CLCSA, CMOS Technology.

I. INTRODUCTION

Future generation ultra supercomputers and requires ultra high speed multipliers. The matrix data multiplication by the supercomputers has wide range of applications such as weather forecasting, oil and gas exploration under the sea, molecular modeling, DNA testing etc. Supercomputer uses the concept superscalar; in this technique up to 8 instructions can be fetched and executed in parallel. There can be more than two dedicated multiplier units in the functional unit of a supercomputer. To meet the requirements of future applications the design of ultra supercomputer is essential. The ultra supercomputing speed may be required to forecast about natural calamities such as the earthquake, tsunami etc. Such applications needs to process huge matrix data from the sensors located at the remote place. Since, multiplication is the most time critical, most area and power consuming operation, the specialized design of multipliers for least delay, smallest in area and lowest in power consumptions are essential.

   All the high speed parallel multiplication operation in hardware consists of three phases as follows.

1.   Partial Product Generator (PPG).

2.   Partial Product Reduction Tree (PPRT).

3.   3. Carry Propagate Adder (CPA).

Since, the performance of the multipliers can be enhanced by designing high speed PPG circuits, many recent advanced paper [1]-[3] has been published. Since, the performance of the multipliers can also be enhanced to the most extent by designing high speed PPRT, many high performance papers [4]-[6] has been published. And finally since, the maximum speed of the multipliers depends on the performance of the Carry Propagate Adder (CPA), various high speed CLA techniques have published in papers [7]-[10].

   References [1]-[3] have presented the design of MBE architecture to generate a partial products in parallel. Reference [1] presented the design of PPG with 68 transistors in CMOS logic, and delay, area and power consumption measured has 0.033 ns/bit, 7.83 μm^2/bit and 1.81 μW /bit respectively. Reference [2] presented the design of PPG with 56 transistors in CMOS logic, and its delay, area and power consumption measured has 0.029 ns/bit, 0.13 μm^2/bit and 1.62 μW /bit respectively. Reference [3] presented the design of PPG with 56 transistors in CMOS logic, and its delay, area and power consumption measured has been 0.045 ns/bit, 0.12 μm^2/bit and 1.65 μW /bit respectively.

   The second phase of the multiplier PPRT. Whose function is to reduce the *n* number of partial products to two only. Reference [4] presented the design of a PPRT using Three Dimensional Minimization (TDM) Method. The TDM has implemented with 98 transistors in CMOS logic, and its delay, area and power consumption measured has 0.06 ns, 30.87 μm^2 and 26.43 μW respectively. Reference [1] has used the concept of reference [4] as PPRT.

   Reference [5] presented the design of 4:2 and 5 :2 compressors. The 4:2 compressor has implemented with 60 transistors in CMOS logic, and its delay, area and power consumption measured has 0.047 ns, 18.9 μm^2 and 20.67 μW respectively. The 5:2 compressor takes 7-inputs and produces 4 outputs namely three carry and a sum. The 5:2 compressor has implemented with 90 transistors in CMOS logic, and its delay, area and power consumption measured has 0.06 ns, 28.35 μm^2 and 24.3 μW respectively.

   Reference [6] presented the design of Wallace tree for the addition of 7-bits of the PPRT, and the number of transistors, delay, area and power consumption has been same as the reference [6].

   The final stage is the CPA, the fastest of all the CPA is the CLA. Reference [1] presented the design of multiple-level conditional-sum adder (MLCSMA) as the final stage adder for high speed operation. References [2]-[3] has been used the concept of references [7] - [10] presented the design of CPA for high speed, small area, and low power consumption.

II. PROPOSED 256×256 BITS MULTIPLIER

This multiplier is designed predicting the future 1 nm CMOS technology to the requirements of next generation ultra supercomputers. Fig. 1 shows the block diagram of super fast multiplier based on MMBE logic. Its operation is based on the concept of 4 to 1 multiplexer, and this is called as partial product generator (PPG). The MMBE produces all the partial products in parallel. Table I shows the truth table of proposed MMBE scheme. From table I equations (1) – (5) are obtained.
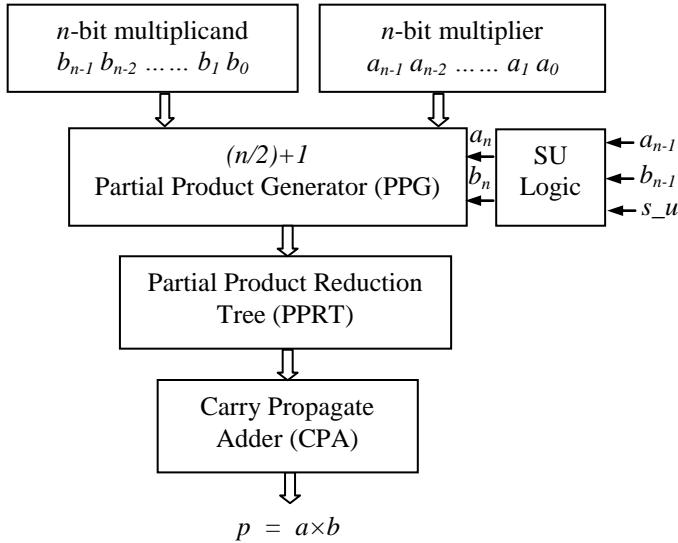
Where the symbol '$\oplus$' represents exclusive OR operation. For the Equations (1) to (4) MMBE logic diagram is as shown in Fig. 2. And using hybrid CMOS logic with 16 transistors is implemented as shown in Fig. 3. According to the input multiplier operand b, the MMBE logic selects 0, a, $2a$, $-a$, $-2a$ to generate the partial product rows in parallel. In equation (1) when $s_i = 1$, MMBE selects $-2a$ or $+2a$. And when $z_i = 1$, the MMBE selects $-a$, $+a$. The negate operation is achieved by one's complimenting each bit of a and then adding $n_i = 1$ to the least significant bit. The negate operation is implemented using equation (5).
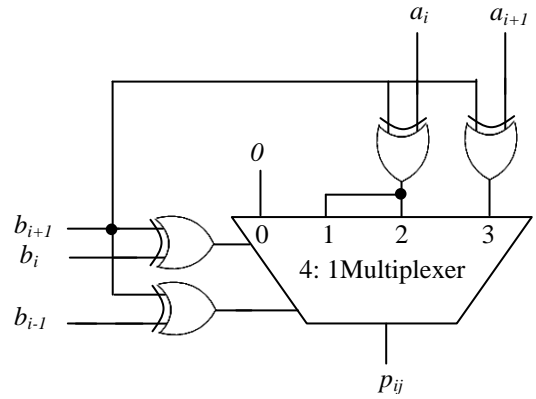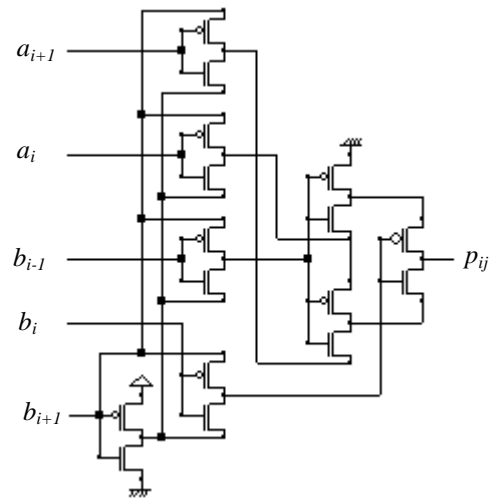

Fig. 1. Block diagram of proposed multiplier.

TABLE I

TRUTH TABLE OF NMBE SCHEME

b_{i+1}	b_i	b_{i-1}	Operation	z_i	s_i	n_i
0	0	0	+0	0	0	0
0	0	1	+a	1	0	0
0	1	0	+a	1	0	0
0	1	1	+2a	0	1	0
1	0	0	-2a	0	1	1
1	0	1	-a	1	0	1
1	1	0	-a	1	0	1
1	1	1	-0	0	0	0

Fig. 2. Logic diagram of MMBE

Fig. 3. Circuit diagram of MMBE

$$p_{ij} = x_{i+1} s_i + x_i z_i \qquad (1)$$

$$s_i = b_i \oplus b_{i+1} \qquad (2)$$

$$z_i = b_{i+1} \oplus b_{i-1} \qquad (3)$$

$$x_{i+1} = b_{i+1} \oplus a_{i+1}, \qquad x_i = b_{i+1} \oplus a_i \qquad (4)$$

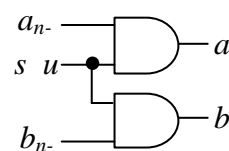$$n_i = b_{i+1} (\overline{b_{i-1} b_i}) \qquad (5)$$
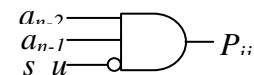

Fig. 4. Sign converter logic.

Fig. 5. Logic diagram for final bit of final row of PPG.

Fig. 4 shows the logic diagram of sign converter. A mode signal called signed-unsigned (*s_u*) is used to indicate whether the multiplication operation is for signed or unsigned number.

When
  s_u = 0, indicates unsigned number multiplication.
  s_u = 1, indicates signed number multiplication

For unsigned number multiplication, the requirement of 0 sign extended bit is as given in equation (6), and for the signed multiplication the sign extended bits required are given by the equations (7) and (8). Equation (9) generates a bit for signed-unsigned multiplication operation.

$$a_n = a_{n+1} = b_n = b_{n+1} = 0 \qquad (6)$$

$$s\_u = 1, \ a_{n-1} = 1, \ b_{n-1} = 0, \ a_n = a_{n+1} = 1, \ b_n = b_{n+1} = 0 \qquad (7)$$

$$s\_u = 1, \ a_{n-1} = 0, \ , \ b_{n-1} = 1, \ a_n = a_{n+1} = 0, \ b_n = b_{n+1} = 1 \qquad (8)$$

$$P_{ij} = \overline{s\_u} \ a_{n-1} \ a_{n-2} \qquad (9)$$

Where *i = n-1, j = n-1.*

Our proposed design of 256 bits multiplier is based on the prediction of the future 1 nm process technology. The various parameters required for the future process technology is explained as follows. For 1 nm process technology the delay of NMOS transistor is computed as follows.

$$T_{dn} = \frac{L^2}{\mu_n V_{ds}}$$

Where L is the length of the channel and for 1 nm technology L is 1 nm, μ_n is the electron mobility carrier and its typical value at room temperature is 550 cm^2 / V sec, and for $V_{ds} =$ 1.8 V supply voltage, $T_d = 0.01 \times 10^{-15}$ second = 0.01 fs (femto second).

For 1 nm process technology the delay of PMOS transistor is computed as follows.

$$T_{dp} = \frac{L^2}{\mu_n V_{ds}}$$

Where L is the length of the channel and for 1 nm technology L is 1 nm, μ_p is the hole mobility carrier and its typical value at room temperature is 240 cm^2 / V sec, and for $V_{ds} = 1.8$ V supply voltage, $T_d = 0.023 \times 10^{-15}$ second = 0.023 fs (femto second). But for the CMOS inverter shown in Fig. 6 when PMOS is turned ON, its resistance R$_{ON}$ is about 4.5 KΩ, then the switching speed of inverter reduces to 0.1 ps (pico second). The CMOS inverter delay measured by 45 nm technology has 0.006 ns, when CMOS technology decreases to 1 nm, then delay decreased to 0.006/25 = 0.24 ps. And thus the delay for the MMBE shown in Fig. 3 consists of 4 inverter delay is computed as follows.

  Delay of MMBE *(T$_{MMBE}$)* = 4 × 0.24 ps = 0.96 ps
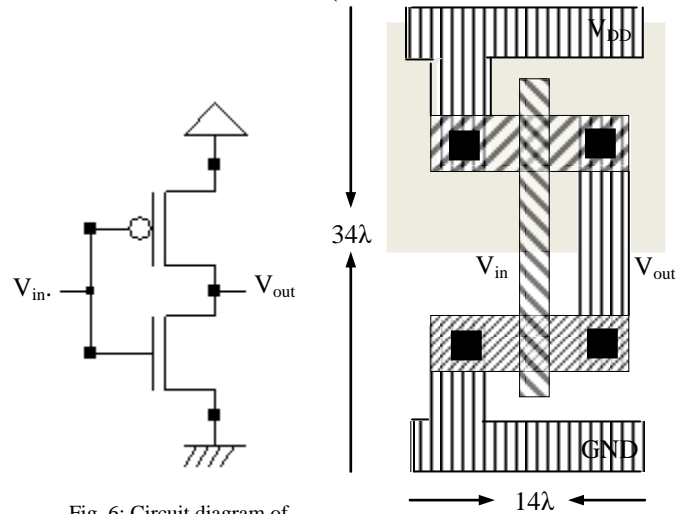

Fig. 6: Circuit diagram of CMOS inverter.

Fig. 7: Layout of CMOS inverter.

For the layout of CMOS inverter shown in Fig, 7, area is computed as follows.

  Area $= 34\lambda \times 14\lambda$

With $\lambda = 1$ nm

  Area $= 34 \times 14\lambda = 476$ nm^2

The MMBE circuit of Fig. 3 uses 8 inverters, and the area is computed as follows..
.

  MMBE area *(A$_{MMBE}$)* $= 8 \times 476$ nm$^2 = 3808$ nm^2

For 256 bits multiplier, there are 33280 MMBE's, thus the total area occupied by the MMBE is computed as follows.

Total MMBE area (A$_{TMMBE}$) $= 3808 \times 33280$ nm^2

  $= 126.73 \ \mu$m^2

The power dissipated (P_d) by MMBE is computed as follows.

$$P_d = N F C V^2_{dd}$$

N = Number of transistor
F = Frequency = 10 GHz
Capacitance (C) = 0.0001 × 10^{-15}F
Power supply (V$_{dd}$) = 1.8 V

The power dissipated by the MMBE (*P$_{MMBE}$*) is computed as follows.

$$P_{MMBE} = 258 \times 129 \times 10 \times 10 \times 10^9 \times 0.0001 \times 10^{-15} \times 1.8^2$$

  $= 1078.3 \ \mu$W

III. DESIGN OF VCA

Our proposed Vertical Column Adder (VCA) is based on the concept of references [4], [6] which presented the design of a PPRT with minimum delay. In this method, each column partial product bits of that column and carry bits generated by the previous column has been added to produce a sum bit and the number of carry bits. The carry bits from the previous column have been fed as input to the full adder so that the delay of the VCA has been the minimum. Fig. 8 (a) shows the circuit diagram of full adder, and is implemented in CMOS logic using only 10 transistors. Fig. 8(b) shows the circuit diagram of SCGP logic, this is the final cell of each VCA. Where cp_i is called carry propagate term, and cg_i is called carry generate term This is designed to perform operations such as sum, carry generate and carry propagate terms so as to save the extra hardware for carry generate and carry propagate terms and is implemented in CMOS logic using only 10 transistors.
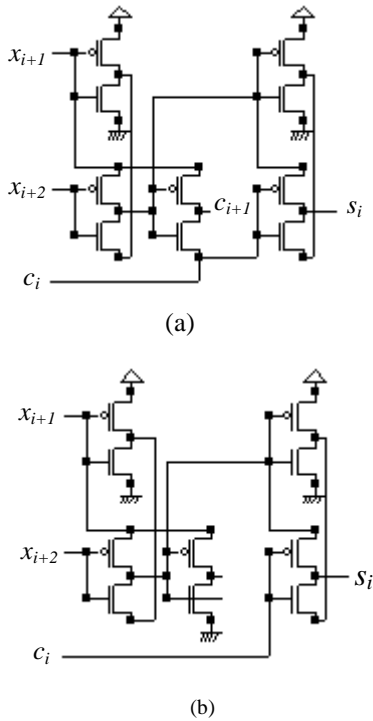

(a)

(b)

Fig. 8. Architecture of full adder. (a). Logic diagram.
(b) Circuit diagram. (c) Circuit diagram of SCGP.

For 256 bits multiplier there are 256 VCA's, and VCS's are implemented using full adders. Each full adder is implemented using 5 inverters. Therefore, the delay and area are computed as follows/

PPRT delay (T_{PPRT}) $= 41.48 \times 10^{-12}$

PPRT area $= 2496 \times 5 \times 476 \ nm^2$

$= 5.92 \ \mu m^2$

The power dissipated by the PPRT is computed as follows.

$P_{PPRT} = 2496 \times 10 \ \times 10 \times 10^9 \times 0.0001 \times 10^{-15} \times 1.8^2$

$= 80.87 \ \mu W$

Thus, the delay, area and power dissipated by the 256 bits multiplier is computed as follows.

IV. DESIGN OF CPA

The final adder which combines the effect of Carry Lookahead Adder and Carry Select Adder (CLCSA) is as shown in Fig. 11. The 8-bit CLA adder is designed and is used in cascade through carry select adder technique for high performance. All the 8-bit CLA adders produce carry in parallel and there are two such 8-bit CLA's in each stage with 0 and 1 as the initial carry input. If the final carry output from the previous stage of 8 bit CLA is 1 then the output selected by the 2:1 multiplexer is the output of the CLA adder with 1-input as the initial carry. Carry expressions for 8-bit CLA adder's are as follows.

$c_1 = g_0 + p_0 c_{in}$

$c_2 = g_1 + p_1 g_0 + p_1 p_0 c_{in}$

$c_3 = g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_{in}$

$c_4 = g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0 + p_3 p_2 p_1 p_0 c_{in}$

$c_5 = g_4 + p_4 g_3 + p_4 p_3 g_2 + p_4 p_3 p_2 g_1 + p_4 p_3 \ p_2 p_1 g_0$

$\quad\quad + p_4 p_3 \ p_2 p_1 p_0 c_{in}$

$c_6 = g_5 + p_5 g_4 + p_5 p_4 g_3 + p_5 p_4 p_3 g_2 + p_5 p_4 p_3 \ p_2 g_1 + p_5 p_4 p_3 \ p_2 p_1 g_0$

$\quad\quad + p_5 p_4 p_3 \ p_2 p_1 p_0 c_{in}$

$c_7 = g_6 + p_6 g_5 + p_6 p_5 g_4 + p_6 \ p_5 p_4 g_3 + p_6 p_5 p_4 p_3 \ g_2$

$\quad\quad + p_6 p_5 p_4 p_3 \ p_2 g_1 + p_6 p_5 p_4 p_3 \ p_2 p_1 + p_6 p_5 p_4 p_3 \ p_2 p_1 p_0 c_{in}$

$c_8 = g_7 + p_7 g_6 + p_7 p_6 \ g_5 + p_7 p_6 p_5 \ g_4 + p_7 p_6 p_5 p_4 \ g_3$

$\quad\quad + p_7 p_6 \ p_5 p_4 p_3 g_2 + p_7 p_6 p_5 \ p_4 p_3 p_2 \ g_1$

$\quad\quad + p_7 p_6 \ p_5 p_4 p_3 \ p_2 p_1 g_0 + p_7 p_6 \ p_5 p_4 p_3 \ p_2 p_1 p_0 c_{in}$

Equations c_1 through c_8 are implemented as shown in Fig. 9. Inputs g_0 through g_7 has provided from the SCGP circuit of Fig. 9 (b). The inputs n_1 through n_8 are the outputs of nand gates, where n_1 is the output of 2-inputs nand gate, n_2 is the output of three inputs nand gate, and $n_3, n_4, n_5, n_6, n_7, n_8$ are outputs of 4, 5, 6, 7 and 8 inputs nand gates respectively. This has been implemented using only 94 transistors. The critical delay measured is 0.05ns.
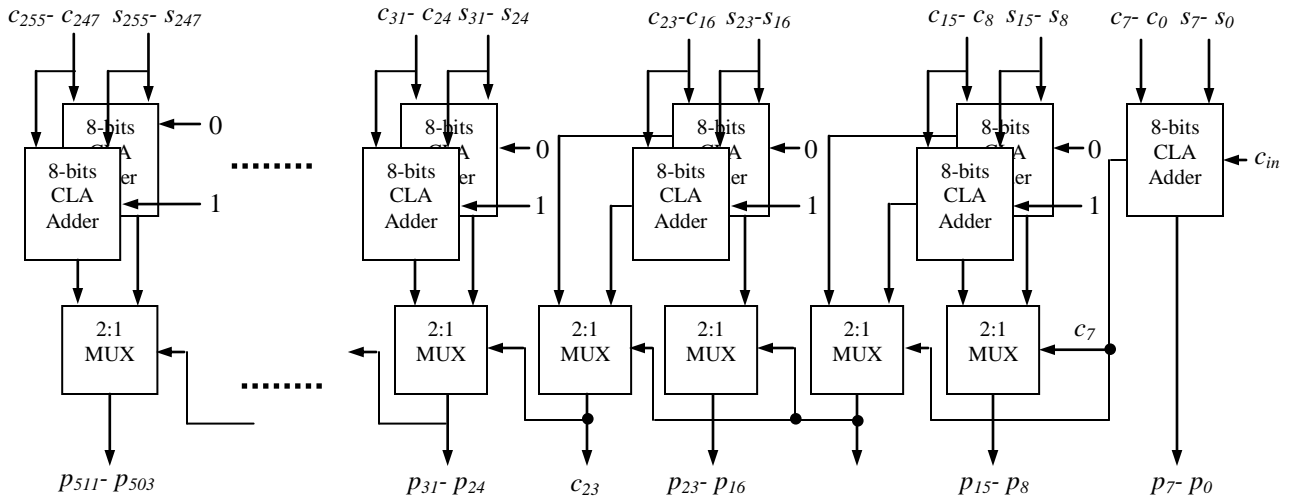
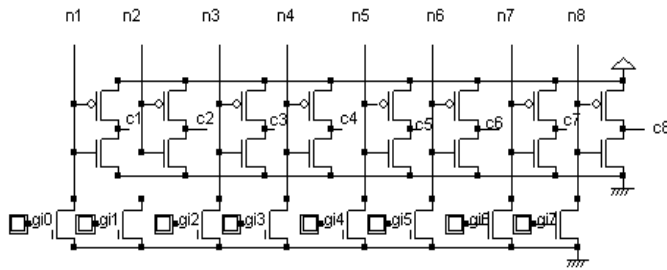Fig. 9. Architecture of CLCSA for 256 bits multiplier.
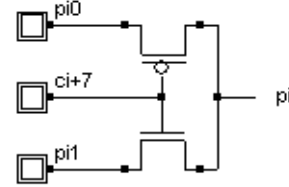

Fig. 10. Circuit diagram of 8-bit CLA carry

Fig. 11. Circuit diagram of 2:1

The delay of CLCSA is computed as follows.

$T_{CLCSA} = 0.045$ ns/25 = 1.8 ps

For 256 bits multiplier 32 CLCSA's are required, and its delay is computed as follows.

$T_{CLCSA} = 0.045$ ns/25 = 32 × 1.8 ps = 57.6 ps

The area for CLCSA is computed as follows.

8-bits CLCSA area = 59 × 476 nm² = 0.028 μm²

For 256 bits multiplier 64 CLCSA's are required

256 bits CLCSA area = 128 × 0.028 μm²

$$= 3.58 \ μm²$$

The power dissipated by the CLCSA is computed as follows.

$P_{dCLCSA} = 64 × 59 × 10 × 10^9 × 0.0001 × 10^{-15} × 1.8^2$

$$= 12.23 μW$$

V. THEORETICAL RESULTS

The critical path delay of 256 × 256 Bits multipliers can be computed by using equation as follows.

Delay $T_{256} = T_{MMBE} + T_{PPRT} + T_{CLCSA}$

$$= 0.92 × 10^{-12} + 41.48 × 10^{-12} + 57.60 × 10^{-12}$$

$$= 0.1 × 10^{-9} s = 0.1 \ ns$$

Area $A_{256} = A_{MMBE} + A_{PPRT} + A_{CLCSA}$

$$= 126.73 \ μm² + 5.92 \ μm² + 3.58 \ μm²$$

$$= 136.23 \ μm²$$

Power $P_{256} = P_{MMBE} + P_{PPRT} + P_{CLCSA}$

$$= 1078.3 \ μW + 80.87 \ μW + 12.23 μW$$

$$= 1171.4 \ μW$$

These theoretical results listed in table I.

Table – 2 Comparison of multipliers

Multiplier Size	References	Delay (ns)	Area (μm^2)	Power (μW)
256×256	Reference [1]	0.21	11452.4	3806.0
	Reference [2]	0.23	10464.8	3206.0
	Reference [3]	0.24	9041.6	3007.7
	Proposed	0.10	136,23	1171.4

VI. CONCLUSION

Our proposed "Future Generation High Performance, Area Efficient And Low Power Multiplier Operating at 10 GHz". With the future 1 nm Hybrid CMOS technology, the various parameters of the 256×256-Bit multiplier are the critical path delay of 0.1 ns, and with this delay it can operate with 10 GHz frequency, with chip area of 136.23 μm^2 and the power dissipation of 1171.4 μW. These results shows the better performance of our proposed multiplier.

REFERENCES

[1] W. –C. Yeh and C. –W. Jen, "High Speed Booth encoded Parallel Multiplier Design," IEEE transactions on computers, vol. 49, no. 7, pp. 692-701, July 2000.

[2] Shiann-Rong Kuang, Jiun-Ping Wang, and Cang-Yuan Guo, "Modified Booth multipliers with a Regular Partial Product Array," IEEE Transactions on circuits and systems-II, vol 56, No 5, May 2009.

[3] Gensuke Goto, Atsuki Inoue, Ryoichi Ohe, Shoichiro Kashiwakura, Shin Mitarai, Takayuki Tsuru, and Tetsuo Izawa, "A 4.1 ns Compact 54×54-b Multiplier Utilising Sign-Select Booth Encoders", IEEE journal of solid-state circuit, VOL. 32, NO. 11, November 1997.

[4] Vogin G. Oklobdzija, David Vileger, Simon S. Liu, "A Method for Speed Optimized Partial Product Reduction and Generation of Fast Parallel Multipliers Using an Algorithmic Approach",IEEE transaction on computers, Vol. 45, No. 3, pp. 294-306, March 1996.

[5] C.-H. Chang, J. Gu, and M. Zhang, "Ultra low-voltage low-power CMOS 4–2 and 5–2 compressors for fast arithmetic circuits," *IEEE Trans.Circuits Syst. I, Reg. Papers*, vol. 51, no. 10, pp. 1985–1997, Oct. 2004.

[6] C. S. Wallace, "A Suggestion for a Fast Multiplier", IEEE Transaction on Electronic Computers, pp. 14-17, February 1964.

[7] Radu Zlatanovici, Sean Kao, and Borivoje Nikolic´ "A 240 ps 64 b carry-lookaheadadder in 90 nm CMOS," IEEE journal of solid-state circuit,, VOL. 44, NO. 2, pp.569-583, February 2009.

[8] *II*: Analog and Digital Signal Processing,, VOL. **43,** NO. 10, OCTOBER 1996, pp.689-702.

[9] **T.** P. Kelliher, R. M. Owens, M. J. Irwin, and T.-T. Hwang, "ELM-A Fast Addition Algorithm Discovered by a Program", *IEEE Trans. Comput,* VOL. 41, NO. 9, September 1992, pp.1181-1184.

[10] Amaury Nève, Helmut Schettler, Thomas Ludwig, Denis Flandre,,*"Power-Delay Product Minimization in High-Performance 64-bit Carry Select Adders", IEEE Trans. Very Large Scale Integr. Systems,* VOL. 12, NO. 3, pp.235-244, MARCH 2004.

AUTHORS

First Author – Ravindra P Rajput received the BE degree in Electronics and Communication Engineering from Karnataka University Dharwad in 1996, M.Tech degree in Digital Electronics from Visvesvaraya Technological University, Belgaum in 2000. He is currently pursuing the PhD degree from Mysore University, Mysore. He is presently working as Associate Professor in the Department of Electronics and Communication, University BDT College of Engineering, Davanagere, Karnataka, India. He has published many books and papers in international conferences and Journals. His research interests include VLSI design, computer architecture, embedded systems, digital signal processing, Advanced microprocessors, design of high speed multipliers, Design of high speed adders.

Second Author – Dr. M. N. Shanmukha Swamy received the BE degree in Electronics and Communication Engineering from Mysore University in 1978, M.Tech degree in Industrial Electronics from the same University in 1987, and obtained his Ph.D. in the field of Composite materials from Indian Institute of Science, Bangalore in 1997. He is presently working as Professor in the Department of Electronics and Communication, Sri Jayachamarajendra College of Engineering, Mysore, Karnataka, India. He is guiding several research scholars and has published many books and papers both in national and international conferences and Journals. His research area includes Wireless Sensor Networks, Biometrics, VLSI and composite materials for application in electronics.

Correspondence Author – Ravindra P Rajput, rprajput2006@gmail.com , 9886083949.