Power and Delay Optimized Edge Triggered Flip-Flop for low power microcontrollers.

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Abstract- The demand for low power circuit design has increased tremendously due to explosive growth of battery operated portable devices like Microcontroller.Microcontroller uses register blocks that are inturn consists of flip flops. The mandate to reduce system power consumption and design energy-efficient ICs has led to the increasing use of low-power IC design techniques that prolong the battery life. In this paper, a novel highly efficient power and delay optimized True Single Phase clocked (TPSC) edge triggered flip-flop has been proposed. The proposed circuit uses lesser number of transistors than the conventional transmission gate D flip-flop that reduce the overall power and delay.The proposed design is also free from both glitch and charge sharing problems making it suitable for high speed and low power applications. The circuits are simulated in TANNER EDA simulation tool using PTM 180nm technology files to compare the performance of proposed circuit with the existing ones. The circuit performs well at different supply voltages.

Index Terms- Register,Flip-flop,Edge triggered,low power,TANNER EDA.

I. INTRODUCTION

The present day technologies require low power considerations for portable devices. And demand for low power circuit design has increased significantly due to the explosive growth of battery- operated portable applications like laptop computers and cellular Phones. The mandate to reduce system power consumption and design energy-efficient ICs has led to the increasing use of low-power IC design techniques that prolong the battery life. Power consumption is an important part of the equation determining the end product's size, weight, and efficiency. The microcontroller is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. The program memory in the form of NOR flash or OTP ROM is often included on chip, as well as typically small amount of RAM. Some microcontrollers may use four -bit words and operate at clock rate frequencies as low as 4 KHz, for low power consumption. There will generally have the ability to retain the functionality while waiting for an event such as a button press or other interrupt, making many of them well suited for long lasting battery applications. The traditional register blocks are often bottlenecks for retrieving data for the processor which is fast when compared with the memory blocks. So this register's blocks are chosen for the low power consideration

Register organization of Microcontroller

In 1981 Intel Corporation introduced an 8-bit microcontroller. Generally this MC has 128 bytes of RAM, 4K bytes of on-chip ROM, two timers, one serial port, and four ports (each 8-bits wide) all on a single chip. At that time it was also referred as a system on a chip. Generally it has a 8 bit processor, Data larger than 8 bits are broken into 8 bits to be processed by the CPU. This MC has a total of four I/O ports, each of 8 bits wide. It also contains serial communication ports and local osscillator. The total 32 bytes of RAM are set aside for the register banks and stack. These 32 bytes are divided into 4 banks of registers in which each bank has 8 registers, RO-R7. RAM locations from 0 to 7 are set aside for bank 0 of RO -R7 where RO is RAM location 0, RI is RAM location I, and so on, until the memory locations 7, which belongs to R7 of bank O. The second bank of registers RO-R7 starts at RAM location 08 and goes to location OFH. The third bank of RO- R 7 starts at memory location 10Hand goes on to location 17H. Finally, RAM locations 18H to I FH are set aside for the fourth bank of RO- R 7. In excess of this banks there are other registers called as special function registers such as DPTR, SP, PC, A, B,C, TMOD, TCON, SCAN, SMOD, PO,PI, P2,P3 PSW etc. except DPTR remaining all the register are 8 bit register, whereas DPTR is a 16 bit register.

In this paper a low power 8 bit serial shift registers are implemented and are given in fig.2 .A common property of computer is locality of refrence;the same values are often accessed repeatedly; and holding these frequently used values in registers improves program execution performance. Data processing is usually done on fixed size binary 'words". Data are stored in registers which can be thought of simply as collections of D-type flip-flops.

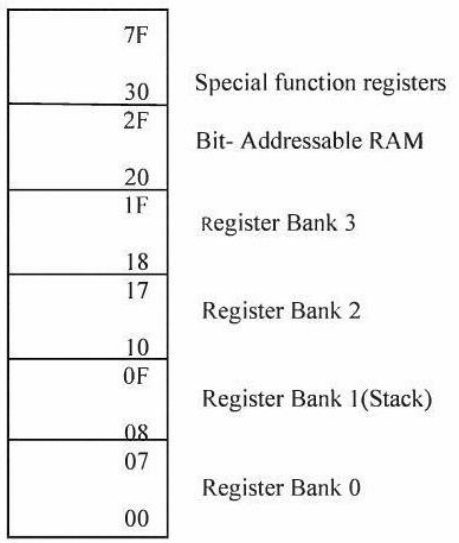


Figure 1:RAM Allocation in microcontroller

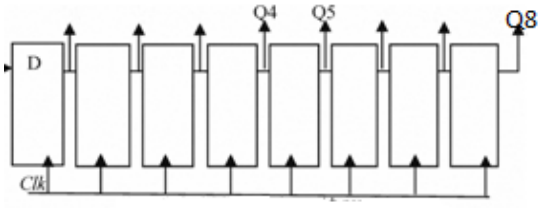


Figure 2: Serial 8-bit register with parallel output.

The D flip flop is the most common flip flop used as the register functional blocks. The Q output takes on the state of the D input at the moment of a positive edge at the clock pin or negative edge if the clock input is active low). It is called the D flip-flop for this reason, since the output takes the value of the D input or data input, and delays it by one clock cycle. The D flip-flop can be interpreted as primitive memory cell, zero order hold, or delay line. Whenever the clock pulses, the value of Qnext is D and Qprev otherwise. Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs). These flip-flops are very useful, as they fonn the basis for shift registers, which are an essential part of many electronic devices. The advantage of the D flip-flop over the D-type "transparent latch" is that the signal on the D input pin is captured the moment the flip-flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. An exception is that some flip-flops have a "reset" signal input, which will reset Q (to zero), and may be either asynchronous or synchronous with the clock. The fig 2 circuit shifts the contents of the register to the right, one bit position on each active transition of the clock. The input X is shifted into the leftmost bit position.

Types of D Flip-Flops
a. Classical edge-triggered D flip-flop
b. Master–slave pulse-triggered D flip-flop
c. Edge-triggered dynamic D storage element

This paper is organised as follows. In section II, conventional D flip –flop have been discussed, section III presents proposed Flip Flop. In section. IV simulation results are presented .In section V,the paper ends with conclusion.

II. EXISTING D FLIP FLOP

a . Conventional D Flip Flop using transmission gate

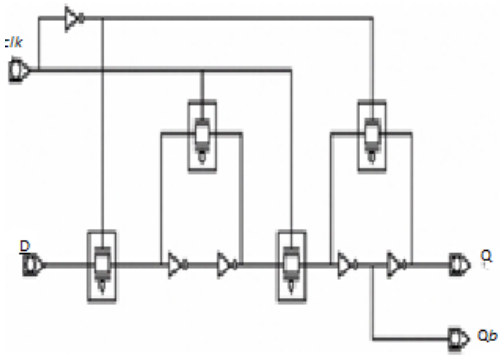


Figure 3: Master –Slave TG FF

A master-slave D flip-flop is created by connecting two gated D latches in series, and inverting the enable input to one of them. It is called master- slave because the second latch in the series only changes in response to a change in the first (master) latch. A Flip-Flop can be designed as a latch pair, where one is transparent-high, and the transparent- low. Master-Slave Flip-Flops based on transmission gates are the best when energy is the main concern. The edge-triggered flip-flop is built from two D-type level-triggered latches. Both latches are enabled with opposite polarity of the clock signal: The second (or slave) latch is controlled by the clock signal, while the first (or master) latch is enabled by the negated clock.

An additional inverter at the output of the TGFF provides non-inverting operation. In this TGFF we use the transmission gates for both master and slave latches shown in above figure It is the one of the fastest classical structure. Its main advantage is the short direct path and the low power feedback. But the disadvantage is that the large load on the clock will greatly affect the total power consumption of the flip-flop. It does have a poor data to output latency because of the positive setup time. Moreover, it is sensitive to clock signal slopes and
data feed through. This adds another concern when using it.

b . Conventional dynamic D Flip Flop

Dynamic or clocked logic gates are used to decrease circuit complexity,,increased operating speed and lower power dissipation[12] of various circuit techniques.A true single phase clock (TSPC) dynamic CMOS circuitis operated with one clock signal that is never inverted.Therefore, no clock skew exits except for clock delay problems, even higher frequency can be achieved[2],[11].

Figure 4 shows a TSPC D flip flop for high –speed operation introduced in[1],[4] [6] .In this flip flop the clocked switching transistors are placed closer to power /ground for higher speed[6].The state transition of the flip flop occurs at the rising edge of the *clk* .Figure 5(a) shows the operation :Q*b* becomes high along *clk* changing low to high with D=0,.In figure 5(a) the dotted lines are the conducting paths when *clk*=0

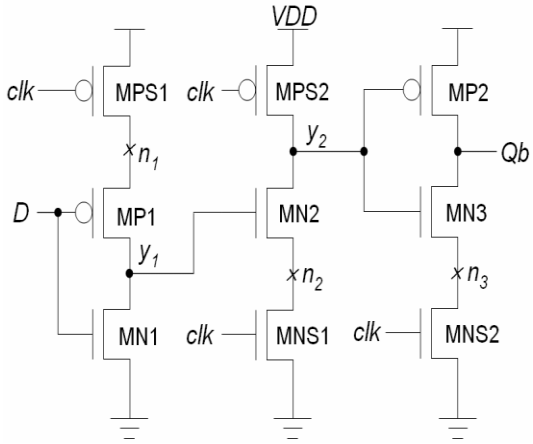
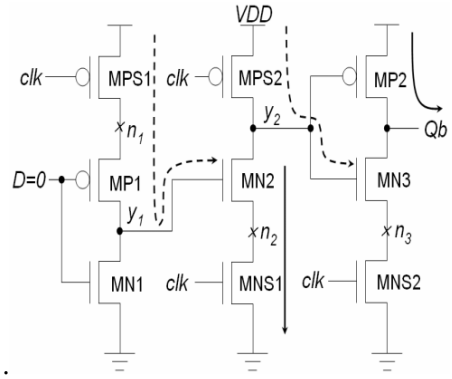
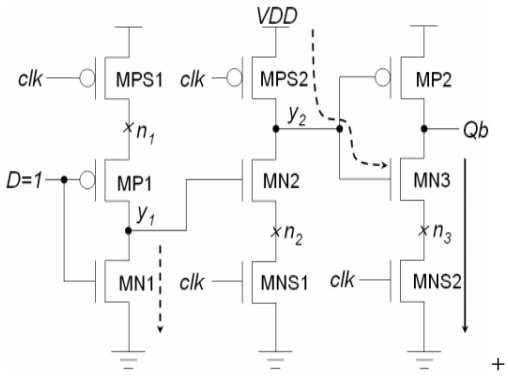


Figure 4 : Conventional Dynamic D Flip Flop

and the solid lines when *clk* =1. If D=0 and *clk* =0,MPS1,MP1 and MPS2 are turned on and n_1,y_1 and y_2 become high .If the single *clk* changes low to high ,the node y_2 is discharged to low through MN2 and MNS1,making MP2 be on and Q*b* high.Figure 5(b),shows the case with clk change low to high and D=0 making MP2 be on and Q*b* high and .Figure 5(b) shows the case with *clk* changes low to high and D=1 making Q*b* be low. The analysis is extended to other input combinations in the same manner.



(a) D=0,*Clk*=0-→1:Q*b*→1



(b) D=1, *Clk=0→1: Qb→0*

Figure 5: Operation of the conventional dynamic D Flip-Flop

GLITCH AND CHARGE SHARING PROBLEM

The main problem with the circuit is the charge sharing .charge sharing raises serious problems when D Flip flop is operating at lower frequency range and second problem is the glitch .It makes the flip-flops fall into the wrong state.Consider the circuit in fig.5(a)with *clk*=0 and D=0 ,where y_1 and y_2 are precharged to high voltage .If *clk* change from low to high,the node y_2 is discharged to low after some delay.In other words,y_2 remain high for a short time,in which MN3 and MNS2 are turned on and Q*b* may change to low.By discharging of y_2,then ,Q*b* returns to the correct state of high.A glitch may appear at Q*b* as indicted in(a) fig .6,

Consider the circuit in fig. 5 to disscuss charge sharing effects when *clk* is low,the node y_2 is always precharged high making MN3 on.The nodes,then,Q*b* and n_3 may share their charges .The high level of Q*b* is somewhat lowered by sharing charges with low level on n_3 as indicated(b) in fig6.

Glitches induced by charge sharing among internal nodes as fig.6 with c*lk* low and D high ,both n_1 and y_2 are precharged to the V_{DD} level and y_1 is discharged to ground ,then clk changes to high making MNS2 turn on and Q*b* low. Here,*clk* is assumed high for a while and D changes high to low instantly .Then MN1 becomes off and MP1 turned on.Nodes n_1 and y_1 share their charges through MP1 making y_1 rise above the threshold voltage of MN2.With *clk* high and MNS1on,the node y_2 discharges slowly,which leads MP2 to be turned on and Q*b* to rise to high.This is shown as (c) and (d) in fig.6.At the point (c),if *clk* changes low to high after D changes to low,there is no critical operation due to small amount of discharg at y_2 and MP2 cannot be turned on. However the edge-triggered operation of the flip flop is prevented in the case that discharing time of y_2 is long as shown at (d) in fig6.

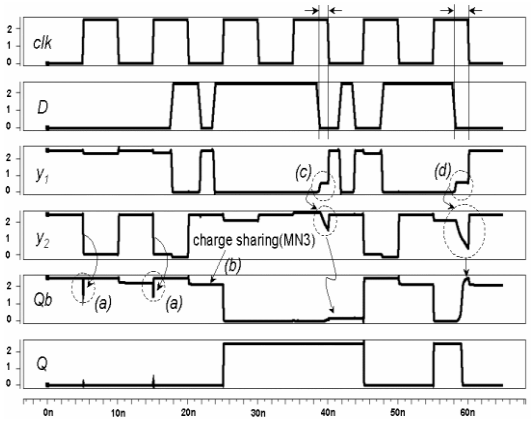


Figure 6: wave form of the d flip flop

III. PROPOSED DYNAMIC D FLIP FLOP

Although above circuit uses only nine transistor but due to above drawbacks of the flip flop loses its edge triggered characteristics and fails to perform proper operation,so a new dynamic d flip flop is introduced which eliminates glitches and charing sharing problem and reducing number of transistor .

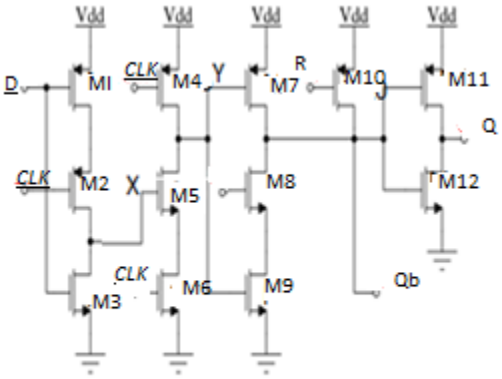


Figure 7: circuit diagram of edge triggered D FF

Fig. 7, shows the design of a specialized single –phase edge triggered register.when *clk=0,* the input inverter is sampling the inverted D input on node X. The second (dynamic) inverter is in precharge mode,with M4 charging up node Y to V_{DD}.The third inverter is in the hold mode,since M7 and M8 are off. Therefore during the low phase of the clock ,the input of the final inverter holding its previous value and the output Q is stable.On the rising edge of the *clk* ,the dynamic inverter M4-M6 evaluates.If X is high on the rising edge,node Y discharges.The third inverter M8-M9 is on during the high phase ,and the node value of Y is passed to the output Q.On the positive phase of clock,note that node X transitions to a low if the D input transition to a high level .Therefore,the input must kept stable till the value on node X before the rising edge of the clock propagates to Y.This represents the hold time of register .transistor sizing is critical for achieving correct functionalities in TPSC .The glitch problem can be corrected by resizing the pull down paths through M5-M6 and M8-M9.This design of dynamic flip flop also enable simple resetting M10 since the reset operation can performed by simple discharging one or two internal nodes.

An efficient functional alternative to a D flip-flop can be made with dynamic circuits (where information is stored in a capacitance) as long as it is clocked often enough; while not a true flip-flop, it is still called a flip-flop for its functional role. Edge-triggered D flip-flops are often implemented in integrated high-speed operations using dynamic logic. This means that the digital output is stored on parasitic device capacitance while the device is not transitioning.

IV. SIMULATION RESULTS

The implementation of the 8 bit register is shown in figure.9.The register blocks are implemented in 180nm technology using the TENNER EDA design tools.

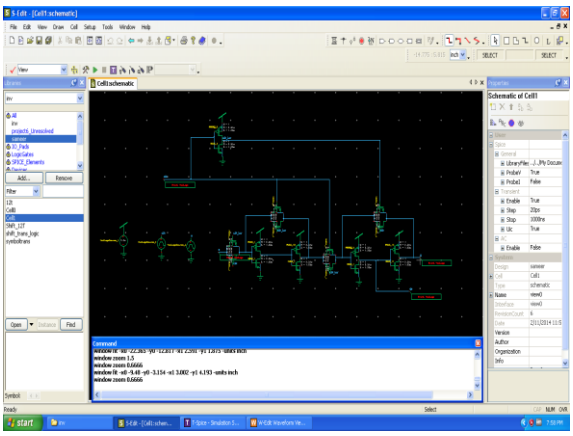


Figure 8: Transmission gate D Flip Flop schematic

The figure 8 is the transmission gate D Flip Flop that is used as building block for the 8 bit serial register.Though it produces the good logic's but has a delay a major constraint that degrade the performance. But comparatively with the CMOS design has the less power consumption. The main drawback of this design is that the lack of capability that drive the large loads. So it was observed that in case of the 8bit register due to worst case of delay and weak driving capabilities the output is degraded. This effect is less in case of Edge triggered TSPC Dynamic D flip - flop.

Figure 9 and figure 10 shows the design and simulation of 1 bit TSPC Flip-Flop respectively. Figure 11 and 12 shows the design of 8 bit serial shift register using the TSPC D Flip-Flop and its simulation

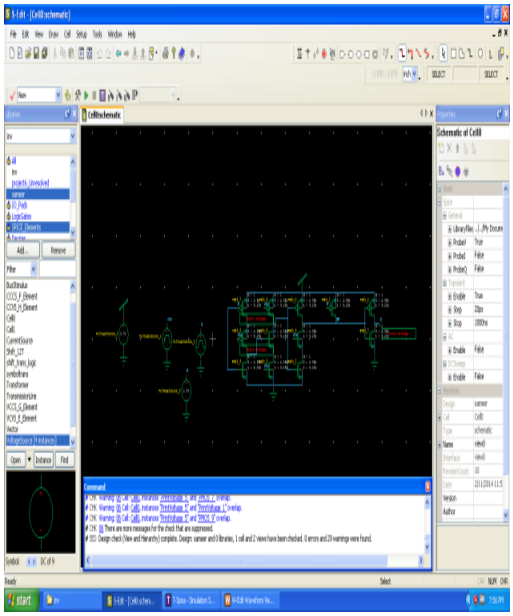


Figure 9 : design of Edge triggered TSPC D flip- flop

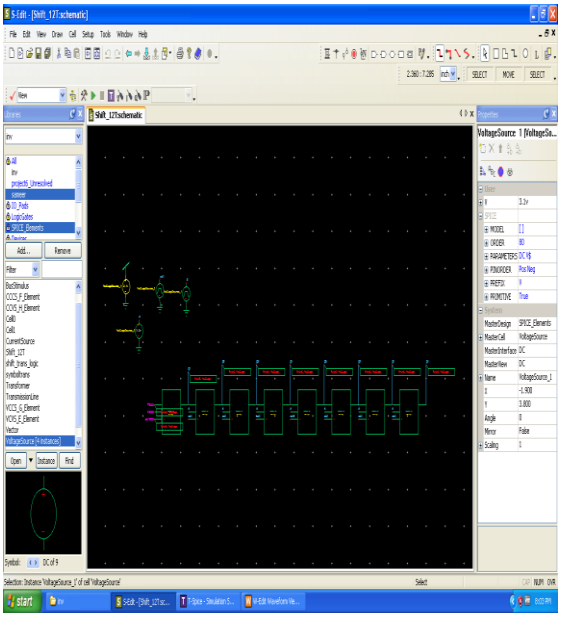


Figure11: design of 8 bit TSPC shift register

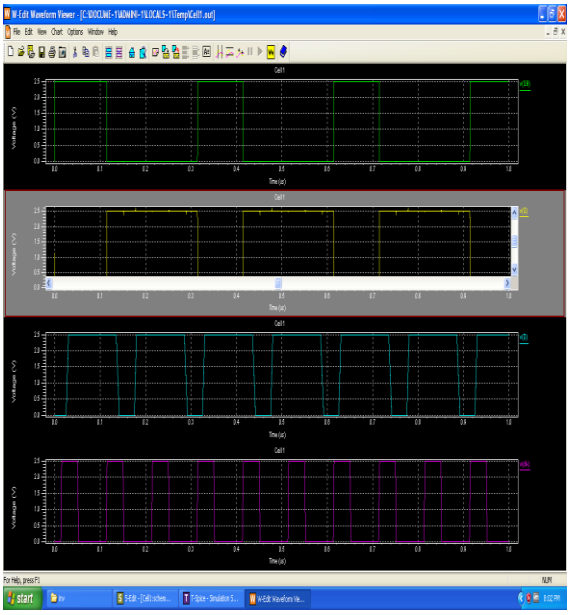


Figure 10: simulation of I bit TSPC D FF

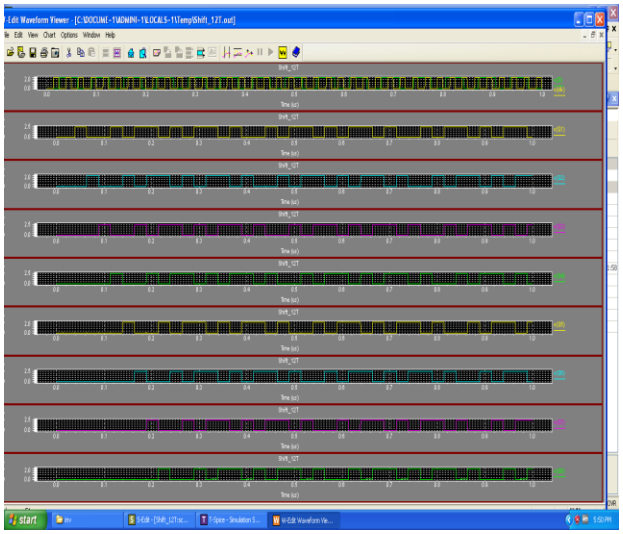


Figure 12: Simulation wave form of 8 bit Edge trigged TSPC register

Comparision of Flip-Flop design results

The comparison of delay and power of 8 bit serial register using TG (transmission Gate), 12T transistor circuits for different operating voltages are as follow

a. Comparision between power consumption in 8 bit serial register.

Voltage(v)	Power(mw) consumed by TGFF	Power(mw)Consumed by TSPC FF
2.5	1.045	0.248
2.8	1.583	0.895
3.1	2.147	0.998

3.5	3.408	1.599
4.0	4.815	1.746

b. Comparision between delay in 8 bit serial register

Voltage(v)	Delay (ps) by TGFF	Delay (ps) by TSPC FF
2.5	250.69	201.5
2.8	270.01	205.1
3.1	275.25	231.8
3.5	290.21	287.3
4.0	292.25	291.2

The Proposed system shows 50%-55% Power improvement than the Existing transmission gate D register and the delay reduces 10%-15% . Thus our proposed system is having very less power and a delay constraints.

V. CONCLUSION

In this Paper, the Flip-Flop designs like TGFF, and proposed flip- flop design are discussed and wok mainly concentrates the design of low register blocks which shows high performance of the Microcontroller .The flip-flops were been designed in TANNER EDA tool in 180nm technology.our proposed system is having very less power and a delay constraints which will lead to improvement in the case of implementation in future mobile devices. This can be much suitable for application of battery oriented operation for less power and delay. In future we can add some other leakage reduction techniques and the power can be further reduced. The future scope of the work might be going for BICMOS register using address transition detection and finFETS that quite match up within nanometer technologies and also replacement of interconnects will further reduce the power and delay that enhances the usability of registers.

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