Design of Topologies of Current Controlled Current Conveyor in 16 nm Bulk CMOS Technology

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Abstract- Advancement in VLSI technology has led to larger number of components on a single chip making it a reality to realise portable systems. Analog circuits are important in every VLSI systems such as filters, current and voltage amplifiers, comparators, A/D and D/A converters, etc. Miniaturization in circuit design requires low-power low-voltage (LPLV) analog integrated circuits to be designed. Analog signal processing's inherent advantage of low power and high speed has led to extensive research in analog domain. Current domain processing having advantages of higher bandwidth, large dynamic range, greater linearity, simple circuitry seems to be the solution. Among the number of current mode topologies current conveyor is the most versatile building block. The second generation Current controlled current conveyor (CCCII) has attained greater popularity in recent years due to electronic adjustability of its X-terminal intrinsic resistance through bias current. Here we have designed three topologies of CCCII found in literature namely dual output current controlled current conveyor (DOCCCII), current controlled current conveyor transconductance amplifier (CCCCTA) and digitally programmable current controlled current conveyor (DPCCCII) in 16nm bulk CMOS technology using PTM (High Performance 16nm Metal Gate / High-K / Strained-Si parameter).

Index Terms- Current Conveyor, DOCCCII, CCCCTA, DPCCCII

I. INTRODUCTION

With scaling down of CMOS to comply with large scale integration and system on chip requirements together with increased demand for portable and battery operated devices, low power low voltage (LP LV) devices are need of the hour. The current mode devices are more suited for (LP LV) operation than their voltage counterpart [1, 2]. Current mode circuits are more immune to noise, less sensitive to supply voltage and have low electrostatic discharge, low propagation delay, high slew rate etc. [2,4]. Among various current mode devices current conveyor (CC) is the most functional device by virtue of its versatile features such as simplicity in design, higher gain bandwidth product, linearity, high frequency operation, less chip area, low power dissipation [4-7] etc. In 1968 [1] the current conveyor (CC) was introduced and has since found recognition in both conceptual and practical implementation. Researches published in last few years reveals that analog circuit designers are now considering the CC as a building block for designing multitude of applications like signal processing, amplification, instrumentation etc. [1,8,9]. A CC is a three terminal device having a low impedance input, a high impedance input simultaneously with a characteristic of virtual short and a high impedance output terminal [1,3]. Since its introduction many topologies of CC have been developed, but second generation current controlled current conveyor (CCCII) gathers larger attention from designers due to its high tunability [1,2,10]. CCCII has in built parasitic resistance which is self-adjustable by bias current, due to this parasitic resistance the requirement of external resistance is reduced. Practical CC has various non-idealities and some of them prove their importance in different applications [11, 12]. Parasitic resistance of CCCII is one of its useful non idealities. Literature shows there are many tunable circuits i.e. current differencing transconductance amplifier (CDTA) [13], current follower transconductance amplifier (CFTA) [14,15], current controlled current conveyor transconductance amplifier (CCCCTA) [16-18], digitally programmable current conveyor (DPCCII) [19,20] etc. In this work we will be designing CCCCTA, DPCCCII and DOCCCII among various topologies of CCCII in 16 nm bulk CMOS and discuss their features.

II. CCCII AND ITS TOPOLOGIES

After its introduction in 1995 [10] CCCII has been the first choice of analog designers mainly because it includes a X- node parasitic resistance which can be electronically controlled through the input bias current and so needs no additional resistance for activation. Current negation and current duplication is very easy to obtain in case of a CCCII, leading to DOCCCII. The equivalent circuit symbol and the principal equation of DOCCCII are given in FIG.1 and Eq.1. DOCCCII has two high impedance current output nodes which provide quadrature signals.

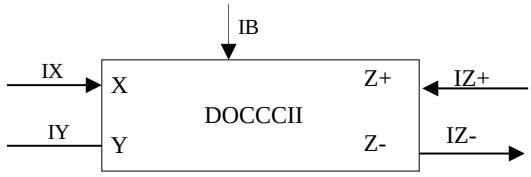

FIG. 1. BLOCK DIAGRAM OF DOCCCII

$$\begin{bmatrix} \mathrm{Vx} \\ Iy \\ Iz \pm \end{bmatrix} = \begin{bmatrix} Rx & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} Ix \\ Vy \\ Vz \end{bmatrix} \quad (1)$$

$$R_x = \frac{1}{g_{m2} + g_{m4}}$$

Where R_x is the parasitic internal resistance at port X and is controlled by bias current I_B.

The CMOS implementation of a class AB DOCCCII is presented in FIG. 2. The circuit consists of a translinear loop consisting of transistors M1 – M4. Two MOS current mirrors (M5 – M6 and M7 – M8) are used to bias the translinear loop with bias current I_B, The input cell presents a high input impedance at input port *Y* and a low input impedance at input port *X*. This cell acts as voltage follower. The current at node *X* is copied to the output nodes *Z*+ and *Z*–. Currents Id_{18} and Id_{14} are cross-coupled through transistors M14, M15, M18 and M19 to generate negative current at *Z*- node. Details are shown in the circuit given in FIG. 2.

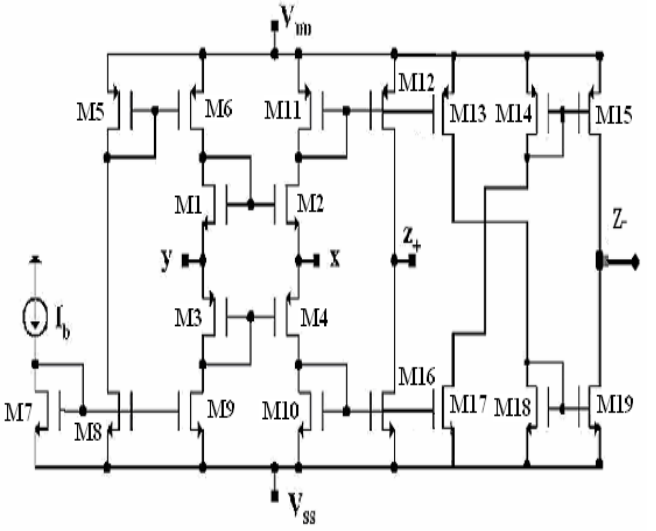

FIG. 2.DUAL OUTPUT CURRENT CONTROLLED CONVEYOR

A. CCCCTA AND ITS DESCRIPTION

It is a four terminal device whose input stage is a CCCII and output stage is made of an operational Transconductance amplifier. The core of the circuit is the differential pair with active load which is used to achieve tunable Transconductance and hence a tunable current gain. The output current of the CCCII is converted in to voltage due to the lumped parasitic capacitances of CCCII and the differential pair. The transistors M_{14} and M_{15} function as a differential amplifier to convert the input voltage to an output current. The transistors M_{16} and M_{17} acts as a current mirror with I_{B2} as input bias current as shown in FIG. 3 When V_{in} is applied it establishes I_{14} and I_{15} in M_{14} and M_{15} respectively. The relation between V_{in} and output current I_o is given in Eq.2.

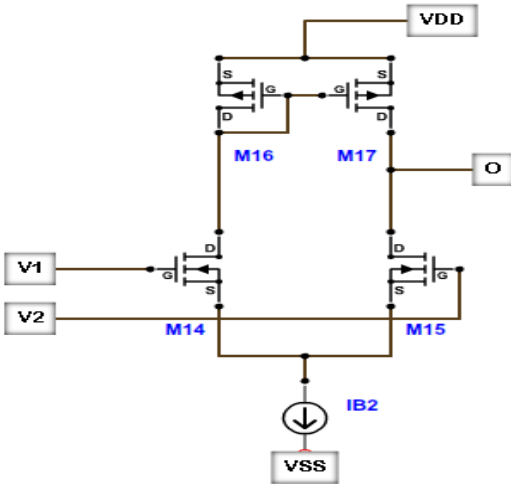

FIG. 3. TRANSCONDUCTANCE AMPLIFIER

$$I_o=\beta_1 g_{m14} V_1 - \beta_2 g_{m15} V_2 \quad (2)$$

Where β_1 *and* β_2 transconductance ratios

If $g_{m14}= g_{m15} =g_m$

$$I_o= g_m(V_1.V_2) \quad (3)$$

Where $g_m=\sqrt{\beta_N I_{B2}}$ (4)

From Eq. 3 & 4 [17] it can be deduced that the input current can be tuned by varying the bias current of transconductance amplifier $I_{B2.}$

The equivalent circuit symbol, port relationship and CMOS implementation of CCCCTA are given in FIG.4, Eq. 5 and FIG.5 respectively.

$$\begin{bmatrix} Iy \\ Vx \\ Iz \\ Io \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ Rx & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} Ix \\ Vy \\ Vz \\ V_o \end{bmatrix} \quad (5)$$

It can be used in both current mode and voltage mode circuits including hybrid (voltage-current) circuits. Authors of [16-18] have demonstrated its versatility by realizing current mode filters, oscillators, inductor etc.

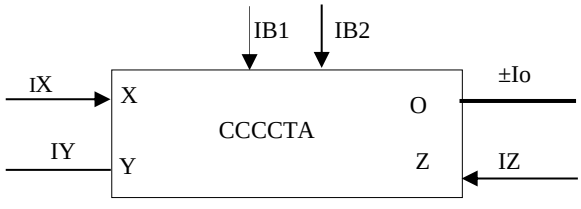

FIG. 4.BLOCK DIAGRAM OF CCCCTA

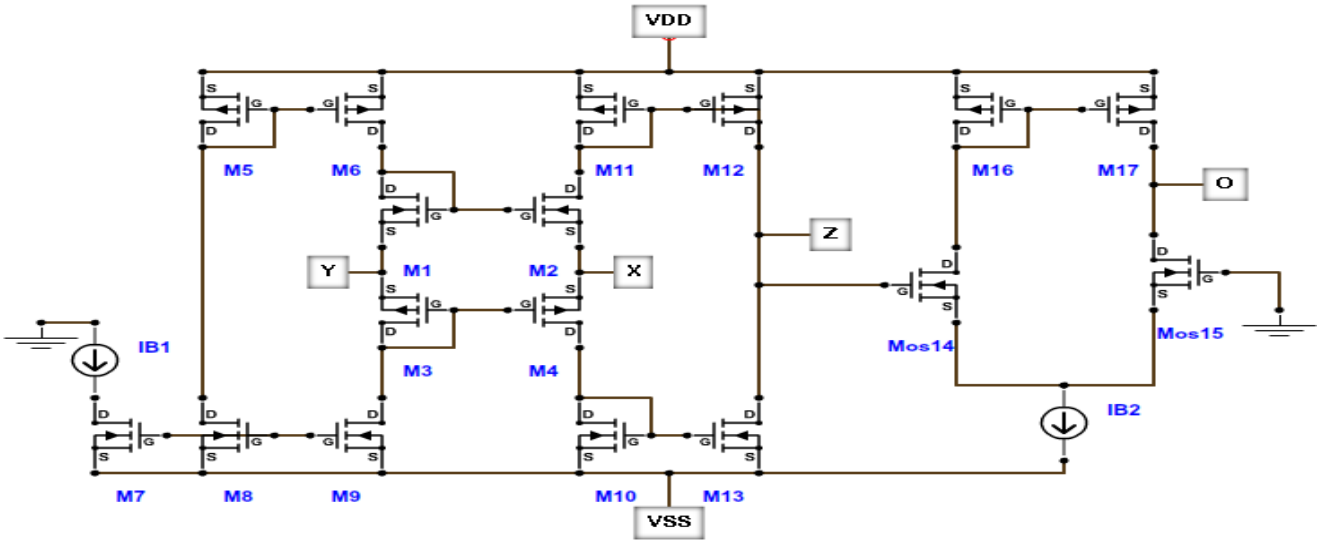

FIG. 5.CURRENT CONTROLLED CURRENT CONVEYOR TRANSCONDUCTANCE AMPLIFIER

B. DPCCCII AND ITS DESCRIPTION

Recently many researches have reported digitally controlled CC [19, 20], the introduction of digital control to CC has increased its functional capability and versatility and eased the on chip control of devices with high resolution capability and reconfigurability [19].

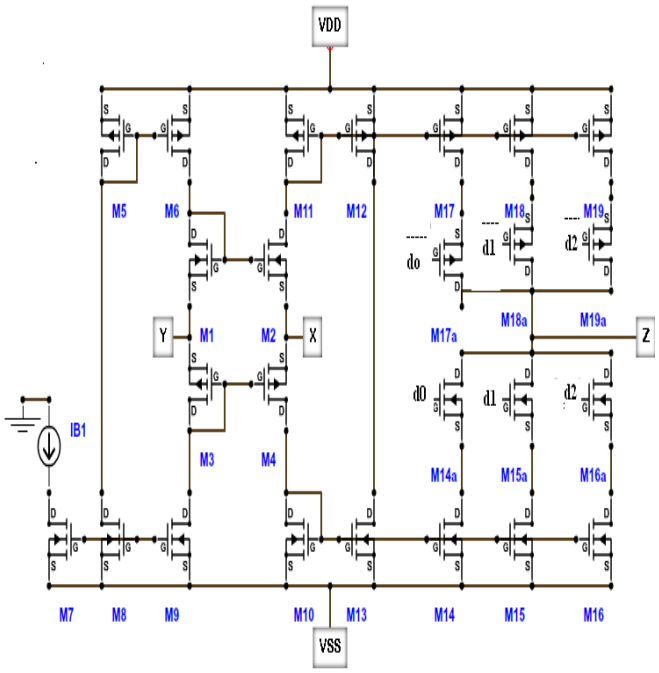

FIG .6 DIGITALLY PROGRAMMABLE CURRENT CONTROLLED CURRENT CONVEYOR

Researchers have used numerous techniques to incorporate digital control in to CC. In this work we have used a current summing network (CSN) as the output stage to get digital control over the current gain, the input stage being the CCCII .CSN mainly consists of array of NMOS & PMOS transistors and their associated switches as shown in FIG.6.The switches (M14a-M19a) in the CSN are controlled by digital code word. A particular branch of the CSN can be activated or deactivated by applying the appropriate code word. The current flowing out of the CSN is the sum of the currents from the activated branches, giving a current gain of 'K', and is given by Eq.7. The block representation of DPCCCII is given in FIG.7.

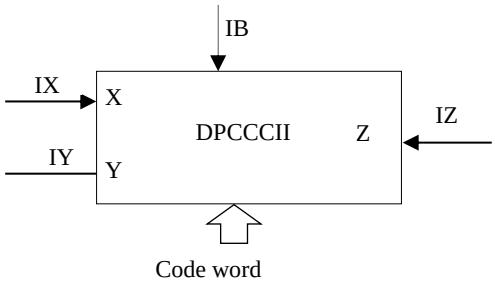

FIG .7 BLOCK DIAGRAM OF DPCCCII

The aspect ratios of CSN transistors are given by:

$$\left(\frac{W}{L}\right)_{Ni} = 2^i \left(\frac{W}{L}\right)_{13} \left(\frac{W}{L}\right)_{Pi} = 2^i \left(\frac{W}{L}\right)_{12} \quad i = \{0,1 \ldots a-1\} \tag{6}$$

The current if flowing out of Z terminal can be expressed by:

$$I_Z = \sum_{i=0}^{a-1} d_i 2^i (I_{12} - I_{13}) \tag{7}$$

Current gain provided by DPCCCII equal to:

$$\frac{I_Z}{I_X}=\sum_{i=0}^{a-1} d_i 2^i \quad (8)$$

Term d_i represents the digital control word applied to the i^{th} branch in CSN. It enables or disables a particular branch of CSN.

III. SIMULATION RESULTS

The topologies of CCCII namely DOCCCII, CCCCTA and DPCCCII are simulated in H-spice using 16nm bulk CMOS PTM [21] to point out the advantage of each. A detailed comparison of the simulation results of the various topologies are given below.

FIG. 8 & 9 shows the AC and transient analysis of DOCCCII. AC analysis gives the range of frequencies of operation. Transient analysis has been carried out with 1 GHz frequency for sinusoidal input undistorted output. At frequencies higher than 2 GHz there is a phase shift in the output so its actual range of frequency is 1Ghz.The simulation results are summarized in the TABLE I given below.

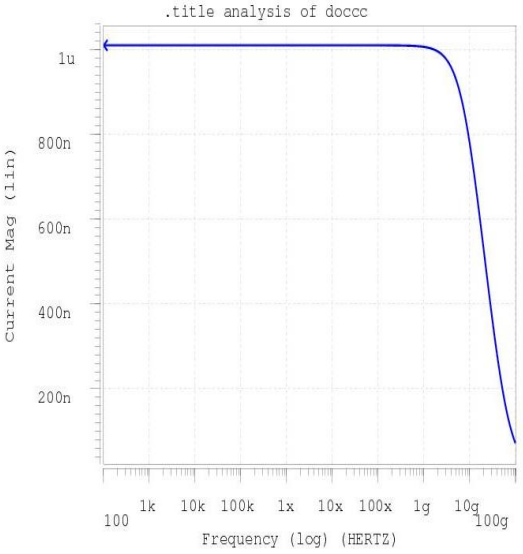

FIG. 9 AC ANALYSIS OF DOCCCII

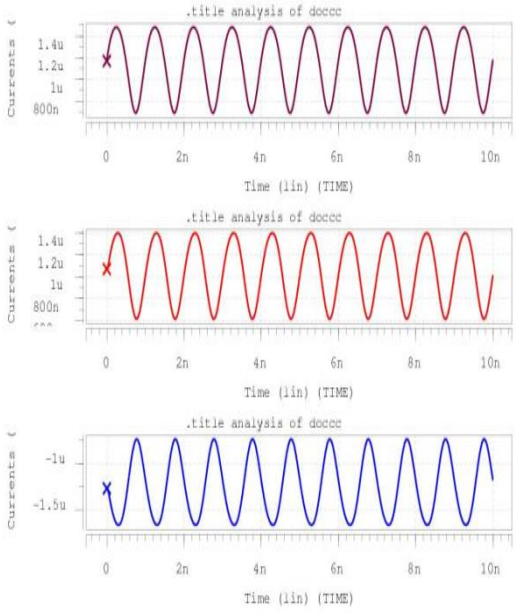

FIG. 8 TRANSIENT ANALYSIS OF DOCCCII

In FIG. 10 R_X vs. bias current variation of DOCCCII is shown.

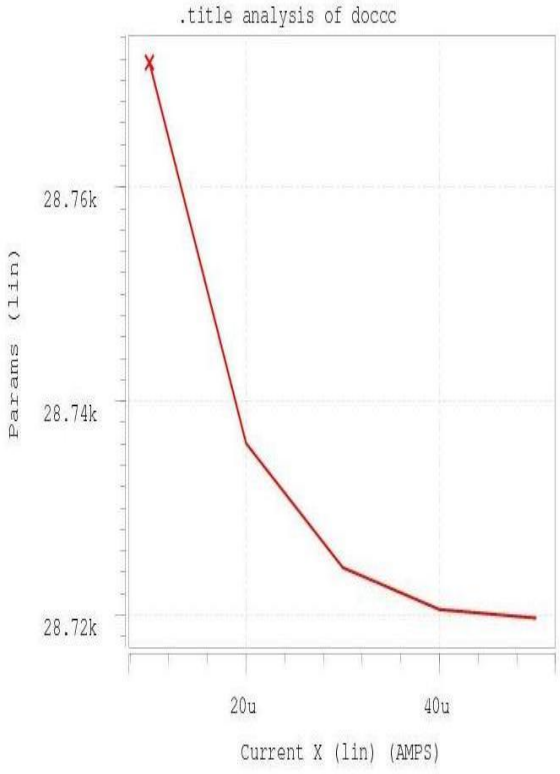

FIG. 10 RX VERSUS BIAS CURRENT VARIATION

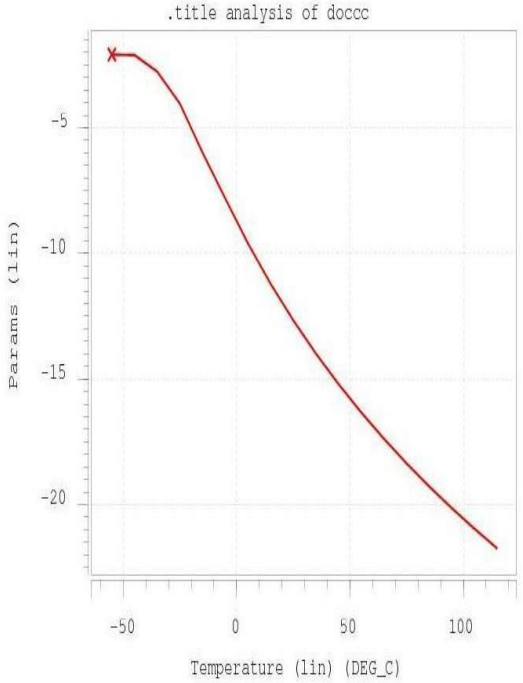

FIG. 11 TEMP STABILITY OF DOCCCII

In FIG. 11 temp stability of DOCCCII is shown.

TABLE I: CHARACTERISTICS OF DOCCCII	
Supply voltage	0.7v
Bandwidth	12.2825 KHz
Input resistance	32KOhm
Output resistance	574.236KOhm
Current gain	1.0996
Power dissipation	53.2503 **µ**watts

The AC response of CCCCTA is plotted with different values of I_{B2} and the obtained response is given in FIG. 12, 13, 14 and 15. The simulation results are summarized in TABLE II. In FIG.12 ac analysis of CCCCTA is given and in FIG.13 current gain between *Io* and I_X in dB is given against frequency.

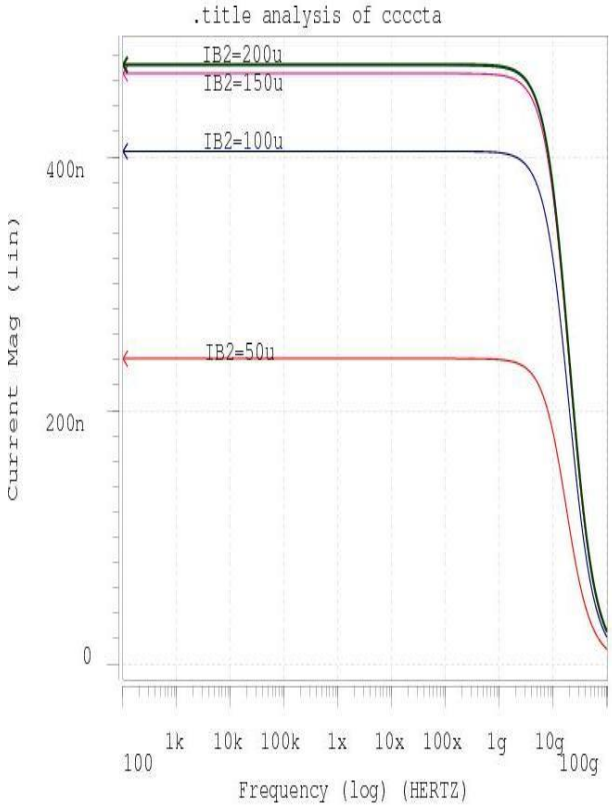

FIG .12 AC ANALYSIS OF CCCCTA

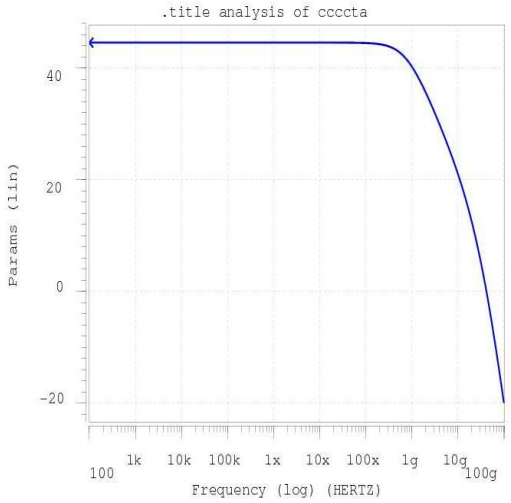

FIG .13 CURRENT GAIN OF I_0 AND I_X OF CCCCTA

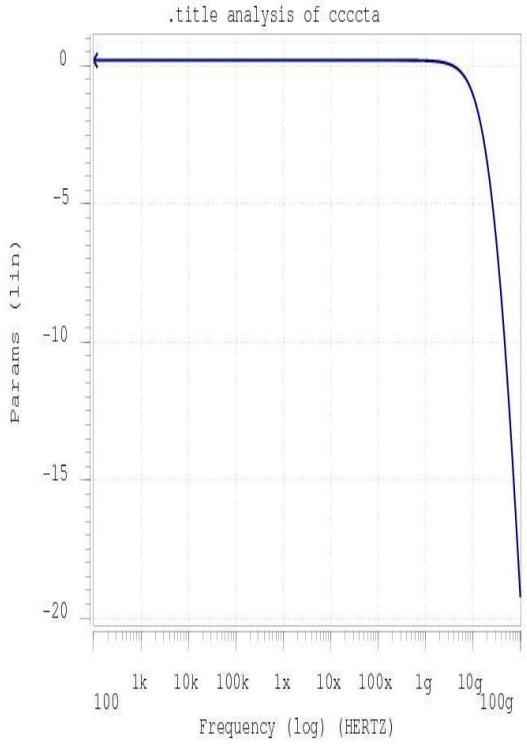

FIG .14 CURRENT GAIN OF I_Z AND I_X OF CCCCTA

In FIG .14 the current gain between I_Z and I_X in dB and in FIG .15 variation of R_X against bias current is given.

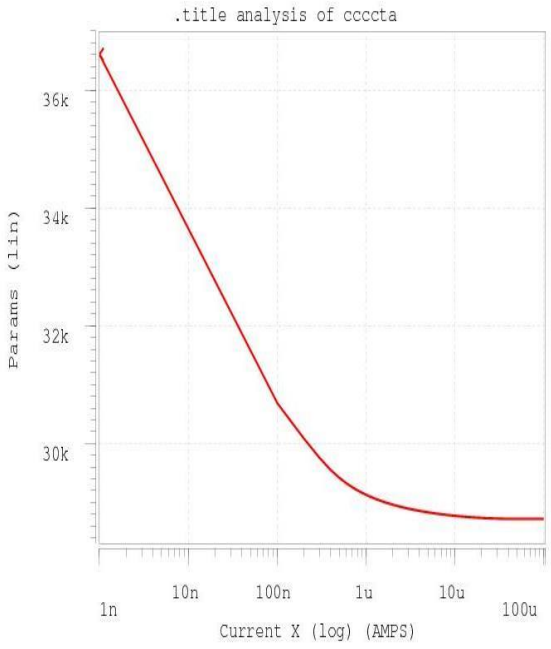

FIG .15 R_X VERSUS BIAS CURRENT VARIATION

TABLE II: CHARACTERISTICS OF CCCCTA	
Supply voltage	0.7v
Bandwidth	3.33 GHz
Output Resistance	231 KΩ
Power dissipation	182.2810μwatts

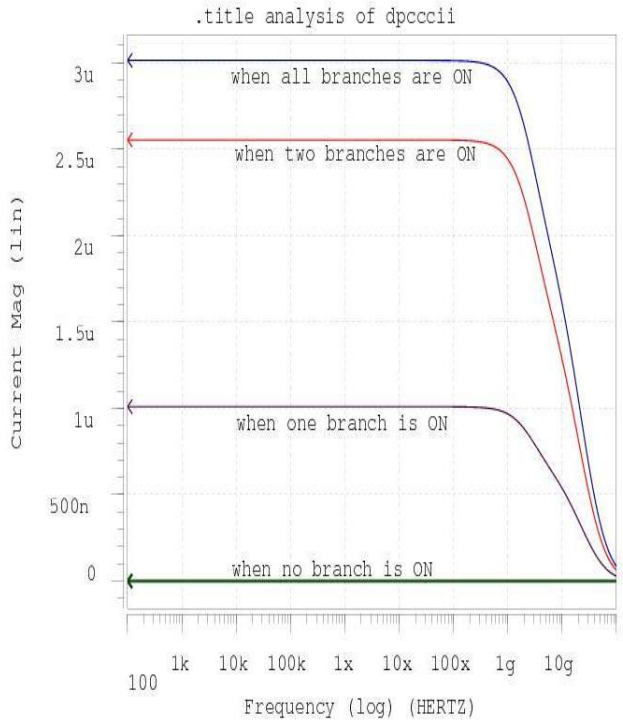

FIG .16 AC ANALYSIS OF DPCCCII

FIG.16 shows ac response of DPCCCII, in this response different gain values are obtained when different branches are ON.

TABLE III: CHARACTERISTICS OF DPCCCII	
Supply voltage	0.7v
Bandwidth	2.0314GHz
Output resistance	144.210KOhm
Input resistance	27KOhm
Current gain	8.31033

TABLE IV: COMPARISON OF TOPOLOGIES

Parameters	DOCCCII	CCCCTA	DPCCCII
Power dissipation	Low	High	Low
Tunable parameters	R_x by I_B	R_x by I_{B1} , g_m by I_{B2}	R_x by I_B I_Z by digital code words
Current gain	Unity	Tunable via I_{B2}	Tunable by digital code words

IV. CONCLUSION

The 3 topologies of CCCII are simulated and studied in 16 nm technology to point out the importance of each. The flexibility of programming of different topologies can be used to synthesize variable gain filters and oscillators with tunable frequency, voltage and current amplifiers of varying gain. These topologies can be used as a building block for field programmable analog array (FPAA).

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