A Review on Memristor MOS Content Addressable Memory (MCAM) Design Using 22nm VLSI Technology

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***Abstract*-** Large capacity content addressable memory (CAM) is a key element in wide variety of applications. A major challenge in realization of such systems is the complexities of scaling MOS transistors. Converges of different technologies, which are well-matched with CMOS processing may allow extension of Moore's law for a new years. This paper provides a new approach towards the design and modeling of memristor based CAM (MCAM) using a combination of MOS devices to form a core of a memory or logic cell that forms the building block of the CAM architecture. The non volatile characteristics and the nanoscale geometry together with compatibility of the memristor increases the packing density with CMOS processing technology , provides for the new approaches towards power management through disabling CAM blocks without loss of stored data, reduces power indulgence, and has scope for speed improvement as the technology matures.

The memristor behaves as a switch, greatly like a transistor. However, not like the transistor, it is a two terminal instead of three-terminal device and does not need power to retain either of its two states. A memristor changes its resistance between two values and this achieved via the movement of mobile ionic charge within an oxide layer. This behaviour influences the architecture of CAM systems, there is no loss of stored data even if the power supply of CAM blocks are disabled.Therefore, memristor-based CAM cells have the potential for major saving in power dissipation.

***Index Terms*-** Content addressable memory(CAM), memory,memory resistor-based CAM (MCAM),SRAM**.**

I. INTRODUCTION

The research for a new model that will attain processing speed in order of an exa flop and further into zeta flop order is a major challenge for both circuit designers and system architects. The evolutionary growth of networks such as Internet also brings about the need for realization of new components and related circuits that are compatible with CMOS process technology as CMOS scaling begins to slow down. As Moore's law becomes more complicated to fulfill, integration of considerably different technologies such like spintronics, carbon nano tube field result transistors, optical nano circuits based on meta material, and more recently the memristor, are in more focus thus creating new possibilities towards realization of innovative circuits and systems within the system on system (SOS) domain.

In this project we explore conceptualization, propose, and modeling of memory cell as a part of a memristor based content addressable memory (MCAM) architecture using a combination of switch as memristor and n-type MOS devices. A typical content addressable memory cell forms a SRAM cell that has two p-type MOS transistors. Construction of a SRAM cell that use memristor technology, which has a non volatile memory behaviour and can be fabricated as an extension to a CMOS process technology with nanoscale geometry, addresses the main thread of current CAM research towards reduction of power utilization. The design of a CAM cell is based on fourth inactive circuit element, the memristor predicted by Chua in 1971 and generated by kang. Chua postulated that a replacement circuit component outlined by the one valued relationship dø=Mdq must exist; where by current moving through memristor is proportional to the flux of magnetic field that flows through the material. So memristor-based CAM cells have the potential for vital saving in power dissipation.

A.Conventional CAM Structures:-

A content addressable memory takes a search word and returns the matching memory location. Such an approach can be considered as a mapping of the large space of the input search word of that smaller space of output match location in a single clock cycle. There are various application as well as translation look aside buffers (TLV), image coding , classifiers to forward internet protocol (IP) packets in network routers, etc. Inclusion of memristors in the architecture ensures that data is retained if the power source is removed enabling new possibility in the system design including the all important issue of power management.

B.Conventional CAM :-

To better appreciate some of the benefits of our proposed structure we provide a brief overview of conventional CAM cell using static random access memory. It comprises of the two inverters that form the latch use four transistor including two p-type transistors that normally require more silicon area. Problems such as comparatively high leakage current particularly for nano scaled CMOS technology and the need for inclusion of both VDD and ground lines in each cell bring further challenges for CAM designers in order to increase the packing density and still maintain sensible power indulgence. Thus, to satisfy the grouping ultra dense designs, low, high-performance. The SRAM cell is the focus of architectural design considerations.

For instance, one of the known problems of conventional 6-T SRAM for ultra low-power applications is its static noise margin (SNM). Fundamentally, the main technique use to design an ultra-power memory is voltage scaling that brings CMOS operation down the subthreshold rule. Verma and chandrakasan show that at very low supply voltages the static noise margin for SRAM will disappear due to process variation to address the low SNM for subthreshold supply voltage Verma and Chandrakasan proposed 8-T SRAM.This means, there is a need for significant increase in silicon area to have reduced failure when the supply voltage has been scaled down. Failure is a major issue in designing the ultra dense memories. Therefore, a range of fault tolerance techniques are usually applied. As long as the defects and failure results from the SRAM structure, a usual approach such as duplication of memory cells can be implemented. observably it causes a large transparency in silicon area which exacerbates the issue of power consumption.

II.LITRATURE REVIEW & RELATED WORK

From the rigorous review of related work and available literature, it is experimental that many researchers have designed MOS content addressable memory by applying special techniques. Researchers have undertaken special systems, processes or phenomena with consider to design and analyze MOS content addressable memory and attempted to find the unidentified parameters. Since in the real world today VLSI/CMOS is in very much in command, from the cautious study of reported work it is observed that very few researchers have taken a work for designing MOS content addressable memory with CMOS/VLSI technology.

Memristor was originally envisioned in 1971 by circuit theorist Leon Chua as a missing non-linear passive two terminal electric component relating electric charge and magnetic flux relation. Leon Chua more freshly argued that the definition should be generalized to cover all forms of 2-terminal non-volatile memory devices based resistance switching effects although some experimental evidence contradicts this claim. In 2008 team at HP labs announced the development of switching memristor based on a film of titanium dioxide this devices are intended in nano electric memory, and computer logic

On January 2009 Di ventra, Pershin, Chua extended the notion of memory system to capacitive and inductive element namely capacitors and inductors whose properties depend on the state and history of system. On April 20 Memristor-based content addressable memory (MCAM) was introduced. On June 1 Mouttet argued that the interpretation of the memristor as a fourth fundamental was incorrect and that the HP Labs device was part of a broader class of memristive systems.

On September-October 2010 Ujwala A.Belorkar has researched on application of 45nm VLSI technology to design layout of static RAM memory.

In October 2011 Tse demonstrated printed memristive counters based on answer processing, with possible applications as low-cost packaging components (no battery needed; powered by energy scavenging mechanism). On March 23, 2011 HRL laboratories and the university of Michigan announced the first functioning memristor array built on a CMOS chip for applications in neuromorphic computer architectures. On July 31, 2012 Meuffels criticized the generalized memristor concept.

On February 27, 2013 Thomas et al., designed a memristor which is easy for learning. The approach utilizes memristors as key components in a blueprint for an artificial brain. On April 23, 2013 Valov, et al., said that the current memristive theory must be extended to a whole new theory to properly.

Depict redox-based resistively switching elements (ReRAM). The main reason is the existence of nanobatteries in redox-based resistive switches which violates the memristor theory's requirement for a pinched hysteresis**.** Both the conventional CAM and MCAM circuits have been implemented using Dongbu HiTech 0.18- m technology where 1.8 V is the nominal operating voltage for the CAM. The MCAM cell is implemented with nMOS devices and memristors without the need for voltage source.

From the careful study of reported work, it is observed that researchers have planned various techniques to design the chip and to improve its characteristics and various parameters but up to the result of my survey regarding memristor based MCAM design.

It is also well known to that; VLSI technology is the fastest growing field today. And according to Moore's law which state that the number of transistors on an integrated circuit will double every 18 months. By scaling behind the technology, we can optimize the parameters like power utilization. The modern technology up to 2008 was lower range of nm technology. Hence considering the improvement of future technology and the advantage of 45 nm technology over 65 and 90 nm technology, the proposed project has been determined to do with the selection of higher order of nm technology.

Considering all this constraint about the demand of today's fast communication world, the research has been taken to design low power MCAM using 22nm VLSI technology.

III.DESIGN METHODOLOGY

Memristor is a new- found fundamental circuit element whose behaviour is predicted is using either the charge dependant function called memristance or flux dependant function called memductance. Therefore, it is important to find the memristance or memductance function of memristor. The methodology advise first doing numerous experiment with a memristor using a square-wave signal to acquire data and then using algorithm inspired by the experiment on ionic memristor. The keywords use for this design is content addressable memory (CAM), memory, memory-resistor based CAM (MCAM), memory-resistor based MOS hybrid design, modeling. Every step of design follows the design flow of microwind 3.1 software. The design methodology will be according to VLSI backend devise flow. The main objective is to design and examine the hybrid architecture of MCAM for future high performance engines .To achieve the proposed target following steps are included in the design and analysis of proposed MCAM.

1. Schematic design of proposed MCAM using CMOS transistors.
2. Performance verification of the above for different parameters.

3. CMOS layout for the proposed MCAM using VLSI backend.
4. Verification of CMOS layout and parameter testing.

If the aim is achieved for all planned parameter including detail verification, sing off for the design analysis and design will be ready for IC making.
If detail authentication of parameters would not finished then again fallow the first step with different methodology.

To achieve the proposed MCAM, different methodology and techniques can be used for research. The MICROWIND3.1 program allows to design and simulate an integrated circuit at physical description level. The package contains a records of common logic and analog ICs to analysis and simulate. MICROWIND3.1 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D method read, VERILOG compiler, tutorial on MOS devices). We can add access to circuit simulation by pressing one single key. The electric removal of circuit is mechanically performed and the analog simulator produces voltage and current curves immediately.

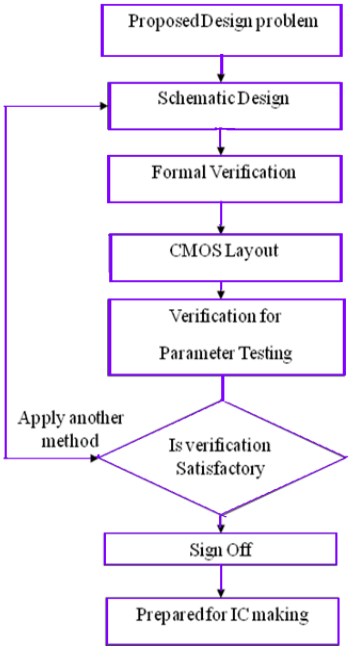

Fig 1: Design Flow Chart.

VI.CONCLUSION

To the best of our knowledge this is the first power consumption analysis of a memristor-based structure that has been presented using a behavioral modeling approach. Because the technology is better understood and matures additional enhancement in performance may be expected.

The local power supply of the read and write amplifier can be easily re- connected, resulting in both low leakage and high performance.

A complete functional and theoretical analysis is given to explain how the proposed cell operates with respect to timing, stability, variation, and cache implementation. In addition, a design methodology is presented for creating portless SRAM cells along with its associated merits compared to stan- dard 6T cell techniques.

Considering the advancement of future technology and the advantage of 22 nm technology over 65 and 90 nm technology, the future project has been decided to do with the selection of higher order of nm technology.
Considering all this constraint about the demand of today's fast communication world, the research has been taken to design low power MCAM using 22nm VLSI technology.

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