

# Dynamic simulation for Real-Time Computers through Field Signal Simulator

A.K. Asthana\*, Dr. S. Vishwanadha Raju\*\*, Sri Lakshmi Peyyala \*\*\*

\* Ex. General Manager, Control and Automation Group, ECIL, Hyderabad, India

\*\* Professor, SIT-JNTUH, Hyderabad, India

\*\*\* Technical Manager, ECIL, Hyderabad, India

DOI: 10.29322/IJSRP.12.02.2022.p12241

<http://dx.doi.org/10.29322/IJSRP.12.02.2022.p12241>

Paper Received Date: 20th January 2022

Paper Acceptance Date: 5th February 2022

Paper Publication Date: 12th February 2022

## **ABSTRACT:**

Real-Time Computer (RTC) System consisting of Fault-Tolerant dual redundant VME bus-based systems (VME-1 and VME-2) with Switch over Logic Circuit (SOLC) and its associated IFMs, SCMs, PS, etc. Each VME system consists of an ED20-CPU card and its associated input/output cards. The I/O status shall be indicated by LEDs. VME system receives the inputs through SCMs / IFMs from Field Signal Simulator (FSS). Outputs generated from VME systems are connected to the FSS through SOLS. Simulation Software completely tests the systems by simulating field inputs to all the channels of each card present in VME bins. The software also checks the healthiness of each card at every scan interval and sends the information to Display Station using TCP/IP protocol with 10/100Mbps.

RTC systems are used for control & process systems and simulation techniques are used to achieve automation by testing these RTC systems. It also includes RTC hardware and the software used for control applications. RTC Systems are deployed to check Plant Systems conditions and generate authorization outputs when all the conditions are satisfied.

## **KEYWORDS:**

Real-Time Computers, Dynamic Simulation, Field Signal Simulator (FSS), Fault-Tolerant Systems, C&I Systems.

## **1.0 Introduction**

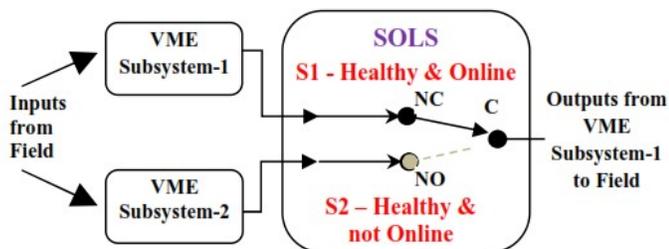
The control and Instrumentation (C & I) System in a typical Power Plant has three layers. The lower layer is the sensors and final Control Elements, the middle layer is the Control Equipment layer & the upper most layers is the Data Acquisition & Supervision Control Computer Systems, Control Panels, and the Operator Consoles.

The C&I subsystems of the Nuclear Power Plant (NPP) are categorized as Safety Critical, Safety-Related, and Non-Safety Systems. Safety-Related Systems of the Control Equipment layer constitute a major portion of the Signal Processing Electronic Systems in a plant.

Because of the Safety associated with Safety-Related Systems, these Signal Processing Electronic Systems are configured as Fault-Tolerant Dual Redundant Real-Time Computers (RTC) systems. RTC systems are VME bus-based systems (called VME sub system-1 and VME subsystem-2).

There is a Switch Over Logic System (SOLS) which allows the outputs of VME system-1 or VME system-2 to drive Final Control Elements.

Each VME system consists of an ED20-CPU card which is based on an MC68020 processor and a variety of I/O cards for Analog Inputs (AI), Digital Inputs (DI), Analog Outputs (AO), and Relay based Digital Outputs (ROP) cards, etc. The status of each I/O is indicated by an LED provided on the front fascia panel of the card.



**FIGURE1:** SOLS System

The Switch Over Logic System receives the outputs of VME system-1 and VME system-2 on 'NO' & 'NC' pins of change over contacts of latching relays. Depending upon whether system-1 is active or system-2 is active the outputs are passed on to the system output thru the common Pin 'C' of the latching relays. The SOLS system has a Logic Card that keeps track of the healthiness of VME system-1 and VME system-2 and also decides which system is active. It drives the latching relays on SOLS Relay cards. Accordingly, the contacts of latching relays are used to provide output to the field.

### 1.1 Problem Definition:

The Signal Processing Electronic System consists of an ED20 CPU card and a combination of I/O cards to meet the system functionality and to analyze the performance. To verify the functionality and performance of the system we need to test the system thoroughly. Without the

Simulator, testing is a tedious process. To simulate these heterogeneous systems we need a Field Signal Simulator to feed different types of inputs are like 0.5V to 9.5V DC, 4-20mA, Potential Free Contact, etc., and to generate outputs for monitoring on Display Station and Process Computer.

### 1.2 Existing Methodology of Testing:

The existing simulator is used as a passive simulator with Switches being provided for simulating Digital Inputs, Potentiometers for Analog Inputs, and for generating Digital Outputs LEDs were provided and DPMs for Analog Outputs. Using a passive test jig, it was a very tedious process to test the RTC systems for all input conditions and time consuming. A dynamic simulation technique was therefore proposed and a facility was established for this purpose. The proposed system is described below.

### 1.3 Proposed Methodology of Testing:

This paper introduces Simulation Techniques to simulate VME RTC Systems with Field Signal Simulator (FSS). FSS can simulate any type of Input signal like 0.5V to 9.5VDC, 4-20mA, Potential Free Contact. Inputs can feed on Simulator to VME I/O cards and generate reliable outputs to monitor on Display Station (DS). It also implements Simulation software for automating the Testing Process. The VME system software has to scan all analog and digital input signals, receive the soft inputs/commands from the Process computer. RTC System status signals are to be sent to Process Computer and Display Station. Each VME subsystem has a dual Ethernet link, which communicates with DS and FSS using TCP/IP protocol with 10/100Mbps. Figure.2 shows the connections between FSS and RTC systems.

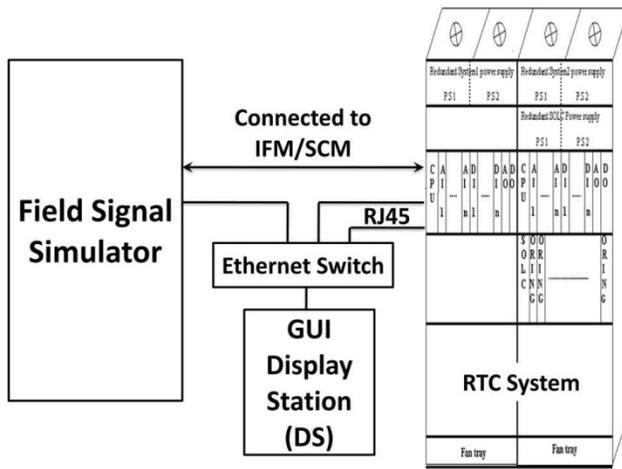


FIGURE 2: FSS for VME– RTC system testing

The system shall satisfy the following requirements:

- Scan all the input signals including soft signals
- Check diagnostics of VME system
- System operation cycle (scan time) is 1sec
- Software shall run independently without any operating system
- Latches the outputs

VME system receives the inputs through SCMs, IFMs from FSS. Outputs generated from VME systems are connected to the FSS through SOLS. Simulation Software thoroughly tests by simulating field inputs to all the channels of each card present in VME bins. VME application programs are fused fed into the EPROM of the ED20-CPU card. The software also sends the information on the healthiness of each card to the Display Station.

**2.0 Fault-Tolerant Architecture:**

RTC system is built-in fault-tolerant architecture. There is a provision to duplicate each of the input signals using Signal Conditioning Modules. The SCM’s also provide Field Signal isolation as well as isolation between output-1 to output-2. The duplicated signal is connected to the two VME systems.

Both the subsystems do the processing as per the required logic and route the outputs to routing logic. When the hardware and software function properly then the healthiness of that particular subsystem is fed to SOLC which in turn directs the routing logic to route the subsystem’s outputs. During initial power ‘ON’, when both the subsystems are healthy then VME-subsystem-1 output shall be routed to the simulator. When VME-subsystem-1 fails, VME-subsystem-2 shall be routed. When VME-subsystem-1 becomes healthy then also VME-subsystem-2 outputs shall be routed, there shall not be any change over from one subsystem to another subsystem unless the subsystem fails. When both the subsystems fail, the fail-safe output shall be routed to the Simulator.

The healthiness of ED20-CPU and I/O boards are checked in a 1-sec scan interval and updated the outputs and sent the data to the GUI display station through Ethernet. When the cards are healthy then the system shall generate two potential-free contact outputs as systems healthiness that go to SOLC.

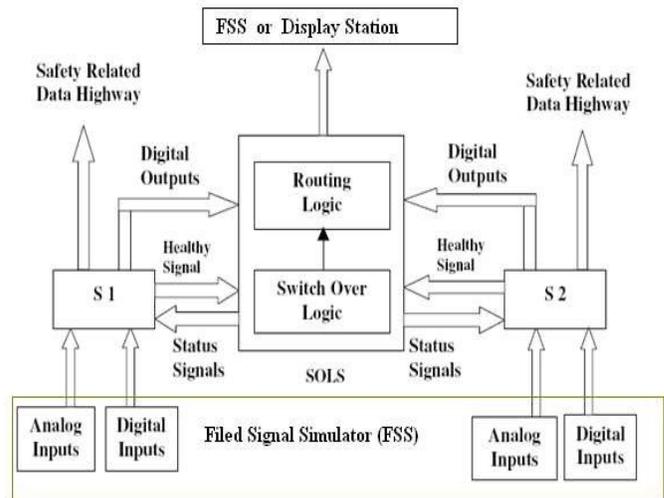


FIGURE3: Fault-Tolerant Architecture

### 3.0 VME System Configuration

VME (Versa Modular Euro) systems are located in this Electronic Cabinet. They can handle Safety-Critical as well as Safety Related signals. In the case of Safety-Critical, it is triplicated & Safety Related is duplicated. Hence dual redundant VME systems with SOLS are used for processing these signals. To connect the field input signals to both the VME systems, all digital input signals are multiplied using relays with two change-over contacts provided on IFMs. For connecting Analog signals to both the VME systems 1:2 Analog signals conditioning modules are used. Then SCMs have one input and two isolated outputs. Outputs from both the VME systems are connected to OR-ing logic cards of SOLS, which routes the healthy system's outputs to the field.

The Cabinet consists of VME-subsystem-1 and its redundant system VME-subsystem-2 along with their associated power supply units. SOLS system is also located along with its power supply unit. The ED20 and combination of I/O boards are not hot-pluggable. In case of failure of any board, power is to be switched off for the respective system, the board is to be replaced and then power is to be restored for that system. RTC system can house any combination of I/O boards based on the system requirements.

Components of the VME Systems are like:

- **VME Bus**
  - **P1-Backplane (VME-Motherboard)**
  - **P2-Backplane (I/O-Motherboard)**
- **ED20-CPU Card**
- **Analog Input Card**
- **Digital Input Card**
- **Digital Output Card**
- **Analog Output Card**
- **Synchro-Digital Conversion Card**
- **Optical Encoder Input Card etc...**

Components of SOLS System are like:

- **Switch Over Logic Card**
- **ORing Logic Card**
- **P1-Backplane**
- **P2-Backplane**

The following steps are to be carried out for VME system configuration.

- i. Place the proper programmed EPROMs in the respective places of the ED20-CPU card.
- ii. System Integration Test Procedure provides the details about the number of I/O cards required for a particular system. The maximum number of channels that each card can support is given in Table-1.
- iii. Set the I/O card addresses in the respective I/O card through jumper selection.

I/O Card	No. of Channels per card
Analog Input	30
Digital Input	30
Relay Output	15
Analog Output	4
SDC card	3
Optical encoder card	3

TABLE1: I/O Cards Capacity

In a single VME system, only one CPU card and nineteen I/O cards can be populated. Similarly, in the SOLS system, only one SOLC and nine OLC cards can be populated accordingly.

### 4.0 Field Signal Simulator

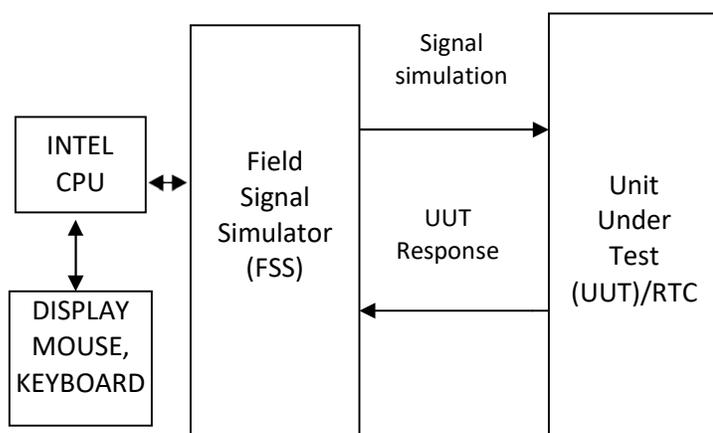
The Computer-based Control System acquires various types of physical parameters, such as temperature, pressure, flow, strain, position, and speed using electronic equipment / modules / boards.

The collected data is sent to a computer for analysis and display. The control systems also take action (control) based on the data received. Turning ON/OFF lamps, motors, valves, heaters, and fans are common functions of control. Sending out voltage, current, digital words, pulses, and waveforms are also functions of the Control systems. Embedded software running in the computer coordinates and executes these functions.

ECIL is equipped with state of art Field Signal Simulator (FSS) to perform the functional and acceptance tests before sending these types of equipment to various sites.

**FIELD SIGNAL SIMULATOR** is designed to simulate the field parameters are like:

1. Thermocouples (K-type) Output
2. Analog Output (0-10V, 0-10mV, 0-24V or 4-20mA)
3. Analog Input (4-20mA)
4. Digital Output
5. Relay Input
6. Open Collector Input
7. Leak Detection Output
8. RTD Output
9. Synchro Output
10. Encoder Output



**FIGURE 4:** Block diagram of the unit under test with Field signal simulator

#### 4.1 System Architecture

The FSS is housed in standard racks with 19”card frames. The system operates on a single-phase 230V, 50Hz, AC power supply. The instrumentation is PXI and VME based, with an Industrial computer for simulation of field signals. A high-speed Ethernet link connects the Industrial computer and the CPU module on the PXI bus. The system is designed to work up to 55 degrees Celsius. Battery back-up is provided for conducting the burn-in tests. Video graphic display, keyboard, mouse, and color printer are connected to the PXI bus-based INTEL CPU board.

#### 4.2 Data Acquisition and Control:

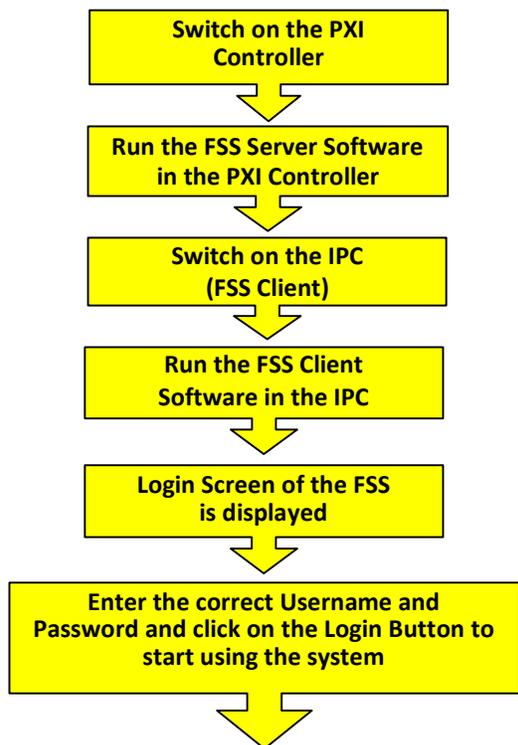
The MS Window operating system runs on the Intel Pentium CPU, on which the application software is developed using National Instrument’s LABVIEW. The application software generates the field data for the signal conditioning boards using the hardware modules. The response parameters of the unit under test are read by the CPU. The FSS generates the test reports based on the Accepted Test Procedure of the Unit under Test (UUT).

#### 4.3 I/O Connections:

FSS inputs and outputs are terminated on terminal blocks internally. All the cables are color-coded and labeled for easy identification. A separate rack is provided for storing the cable bunches, whenever the system is not in use. All inputs and outputs are available simultaneously; no multiplexing of the signals is done.

The maximum number of signals that FSS supports is given in Table-2.

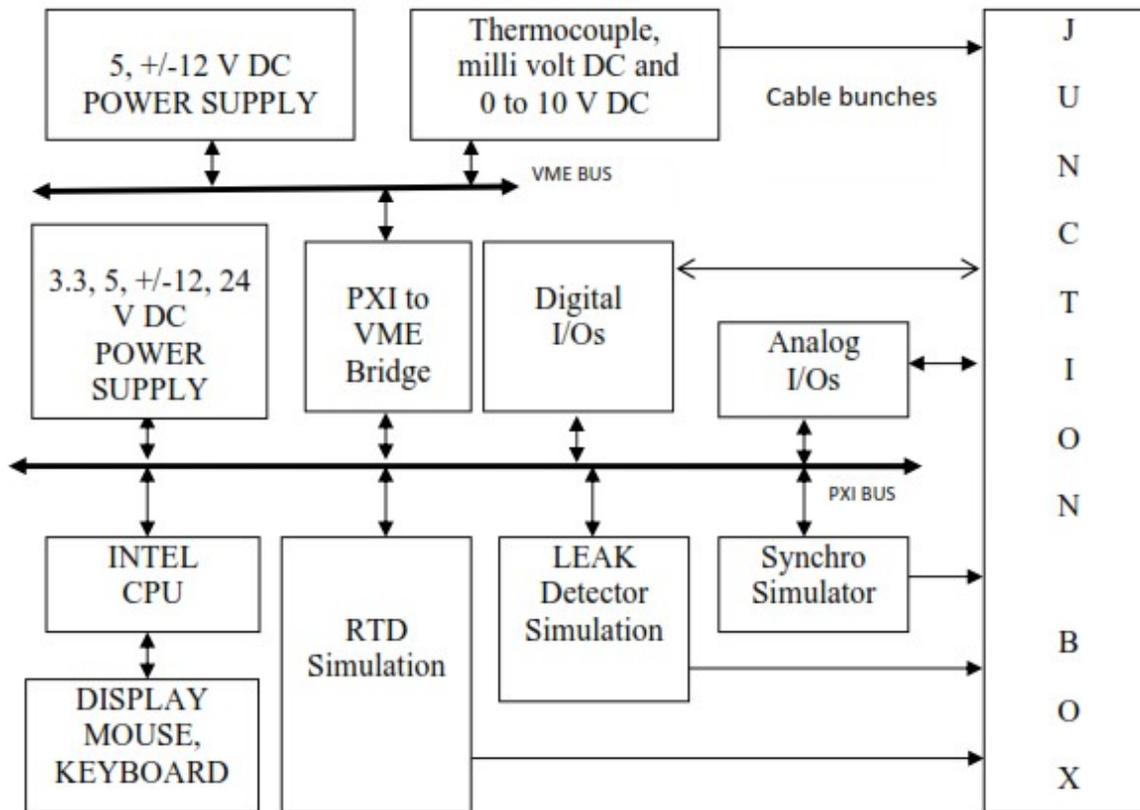
**4.4 FSS Software:**



FSS software is generic software to simulate that field signals for a Computer-based control and instrumentation system. FSS software works in conjunction with PXI, VME, and CRIO based hardware to simulate the field signals for the Computers based control and instrumentation panel. Its general-purpose nature easily extends its capabilities to build and perform specific UUT test routines.

The FSS software is built following a “Client-Server” model. The FSS system consists of a PXI controller and two IPCs. PXI controller serves primarily as the Server and IPCs as Clients. One of the IPC will be designated as the “Development Station”. Either the PXI-controller or the IPCs can be used as “Development Station”. It is recommended that PXI-Controller should not be used as a development station while it’s running the server software. Likewise, IPCs software should not be used as a development station when it’s running the client software.

**FIGURE 5:** Switch on Procedure for FSS Server & Client



**FIGURE 6:** Block diagram Field signal simulator

The server software in the PXI-controller runs in the background when it is launched. It should be launched before any client software is launched. The PXI-Controller can also act as a client in addition to being the server. Thus, we can run the client software on the PXI-controller itself which puts the usage of two IPCs as additional clients, only on a need basis.

The following are the major modules of the Client software:

- i) **Create UUT info:** Create UUT info utility allows the user to create a file that stores the information about a Unit under Test like tags, FSS Logical channels used, IP Addresses, Channel Mapping, etc. This utility reads the UUT Tag configuration from UUT terminal info file. This is an excel file with a defined format. The user will have to enter the Tags and their terminal information in this file. This utility also reads the UUT Soft Input Info file. This is also an excel file where a user enters the details of the soft input.
- ii) **I/O Explorer:** I/O Explorer allows the user to configure, read and write values for each type of channel. Users can directly update values on different channels interfaced with the VMERTC system under the testing and observe the UUT behavior and response to the Field Simulated Signal from FSS System.

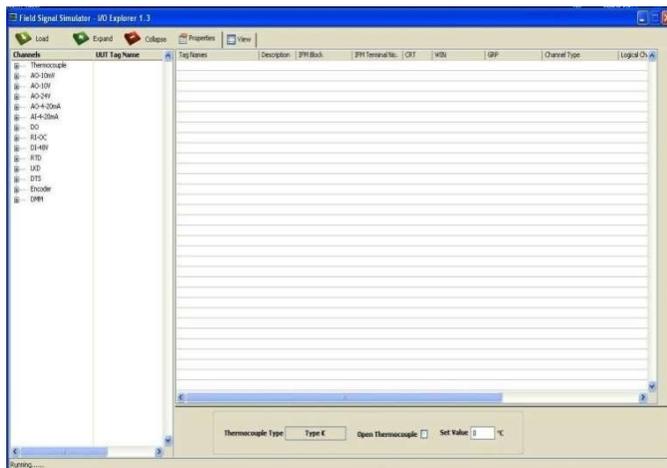


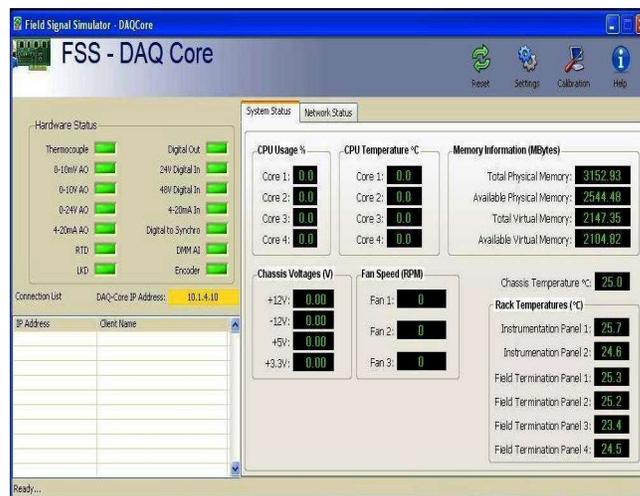
FIGURE 7: I/O EXPLORER–Home Screen

I/O Explorer also helps the user of the system to establish the integrity in signal connectivity between the FSS system and the UUT. Through the I/O Explorer user can set a value on a channel and measure the value using an external measuring device before connecting it to the appropriate channel or the terminal of the UUT. This ensures that the right channel of the FSS system is connected to the UUT.

The following are the major modules of the Server software:

- i) **DAQCore:** This module is the heart of the FSS software. DAQCore implements hardware-level interaction with the PXI, VME, and CRIO which constitutes the FSS systems. It calls the APIs built for the FSS systems and executes the commands sent by the Clients. DAQCore is a single module through which all interaction with all different types of hardware used in the FSS system is possible. DAQCore implements a common I/O read/write errors handling mechanism and it also returns the value that is set through the commands.

FIGURE 8: Server–System Status



- ii) **Command Router:** The server hosts the command router module. Command Router module is used for identification of the origin of command for the DAQCore to execute. After the command is executed by the

DAQCore the response is again routed through the Command Router to the source. The command router module also sorts the commands from various sources and segregates them based on the signal type for the DAQCore to execute. The source of the command could be anywhere.

#### 4.5 FSS Server:

The first FSS server software is launched on the PXI-controller. The server should be launched before launching the client software of the IPCs or on the PXI-Controller. The client displays an error message if the sequence is not followed. FSS Software runs on the background with its icon minimized to the windows taskbar icon tray. The Server application also displays the health parameters of the FSS systems as well as the clients that are connected. The Server module interacts with the hardware of the field signal simulation system. The server module is responsible for reading and writing to all hardware I/Os.

**Server Software:** The Server Software is mainly divided into the following module:

1. **DAQCore:** Service hardware commands from multiple modules of the main software.
2. **DAQ Engine:** Provides abstraction from hardware to other modules of the main software.
3. **Settings:** Provides settings to the user to connect using MXI or TCP/IP.
4. **Calibration:** Provides channel calibration to the user

#### 4.6 FSS Client:

After the launch of the FSS server on the PXI-controller, FSS client software is launched either on the PXI-controller or on the IPCs.

Client software has an access privilege setup. First, the user has to login to the client software with the appropriate login ID and password. According to the privileges set for logic ID, features of the client software will be available or unavailable to the user.

Based on the successful login the client application enters the home screen.

Users can initiate the system configuration as follows.

1. Create the UUT Information file
2. FSS to UUT connectivity file (Logic Channel Mapping)
3. Launch I/O Explorer
4. Test FSS and UUT connectivity
5. Generate Test Report

**Client Software:** The Server Software is mainly divided into the following module:

1. Create UUT Info
2. I/O Explore

#### 5.0 Testing

For System Integration Test, two different types of software are to be developed. One is system software runs on VME based RTC systems and second software is GUI which runs on PC / Display Station. This GUI software is user-friendly, easily configurable, enabling the tester to use the same software for different I/O configurations of the VME-RTC system without much change in the software.

Two sets of programmed EPROMs named (S1Odd, S1 Even & S2 Odd, S2 Even) are provided to test the VME-RTC systems with dual redundant architecture. One set of EPROMs are to be used for VME subsystem-1(S1) and another set of EPROMs are to be used for VME subsystem-2 (S2). GUI software is to be installed on the PC.

In GUI software, provision is available to select the number of I/O cards (AI, DI, RO & AO, etc.) as per system requirements, and the same is communicated to the VME ED20 CPU card through TCP/IP protocol. Based on the selection, VME Application software scans the inputs and latches the outputs.

Two Ethernet ports are available in each system and the scanned data are sent to both ports simultaneously. The data received from both ports can be viewed in the GUI software.



FIGURE 9: VME RTC-I/O Simulation GUI in LabVIEW



FIGURE 10: VME RTC system with I/O simulation thru FSS

The Integration and System Testing process focus on the functional externals, testing to uncover errors and to ensure that the defined input will produce actual results that agree with required results.

System Integration and testing process can be carried out as per Detailed Test cases mentioned in the Test Procedure. Test Procedure should be defined for each hardware and software to check the functional and performance requirements to be met. It should also be defined (hardware & software integration and test procedure) for assembled hardware and integrated software of each sub-system to check the integrity of both hardware and software. Test Reports should be generated accordingly. The Test results and observations shall be recorded in a document for review/audit during Verification and Validation (V&V).

Requirement for the design of online diagnostics for VME hardware/software should be specified to detect various faults in the hardware/software, data, or code corruption and to take appropriate actions. This should include identification of system resources to be checked, diagnostics on system start-up, and during run-time on detection of faults. In addition, the design must provide built-in features for online fault detection, fault indication, and driving fail-safe outputs.

All the cards designed on the VME bus incorporate extensive online diagnostics features for fault detection and health monitoring through the watchdog timer. The watchdog timer forms the heart beat of the entire computer system. Since plant outputs are controlled through the actuation of relays, watchdog features were also integrated into the Mono-shot Relay Output board. This ensures that, in case of either system power failures or the failures of the ED20 CPU software, the plant outputs terminate to fail-safe mode, thus preventing the catastrophe on the operating plant.

Sl. No	Signal Type	Signal Range	Signal Characteristics	Number of Channels
1	Analog Outputs (Signal Generation)	K-Type Thermocouple	0.5°C resolution	500
		0-10mVDC	14-bits @ 25 mV FSR (equivalent to 1.53µV Step)	16
		0-10VDC	14-bit resolution	600
		0-24VDC	14-bit resolution	20
		4-20mA	14-bit resolution	75
2	Digital Outputs (Signal Excitation)	Dry contact	24VDC, electro-mechanical	650
3	Analog Input monitoring	4-20mA	14-bit resolution	10
4	Relay Input Monitoring	Dry contact	24VDC, electro-mechanical	350
5	Open-collector monitoring	Open-collector	(VCE) SAT ≤ 1.5V	50
6	RTD (Pt-100) sensor simulation	-200°C to 850°C	Δ1°C (equivalent to 0.3Ω Step)	30
7	Leak Detector (LKD) signal simulation	Resistance arm Simulation	0Ω, 470Ω, 570Ω, Open	350
8	Encoder	Angles in degrees	0° to 360°	25

**TABLE 2:** Maximum number of Signals supports FSS system

### 6.0 Verification & Validation (V&V)

The computer-based control systems have to meet not only the functional performance but in addition they have to meet the regulatory requirements like enhanced reliability and availability. Redundancy and fault tolerance features are to be provided and the overall system design should have a high mean time between failures and low mean time to repair to achieve better reliability.

The below Figure-11, shows the design of real-time computers of both hardware and software sub-systems which are subjected to the system Verification and Validation process. At the beginning of the system development, verification plans and procedures shall be produced which shall cover hardware verification, software verification, and system validation.

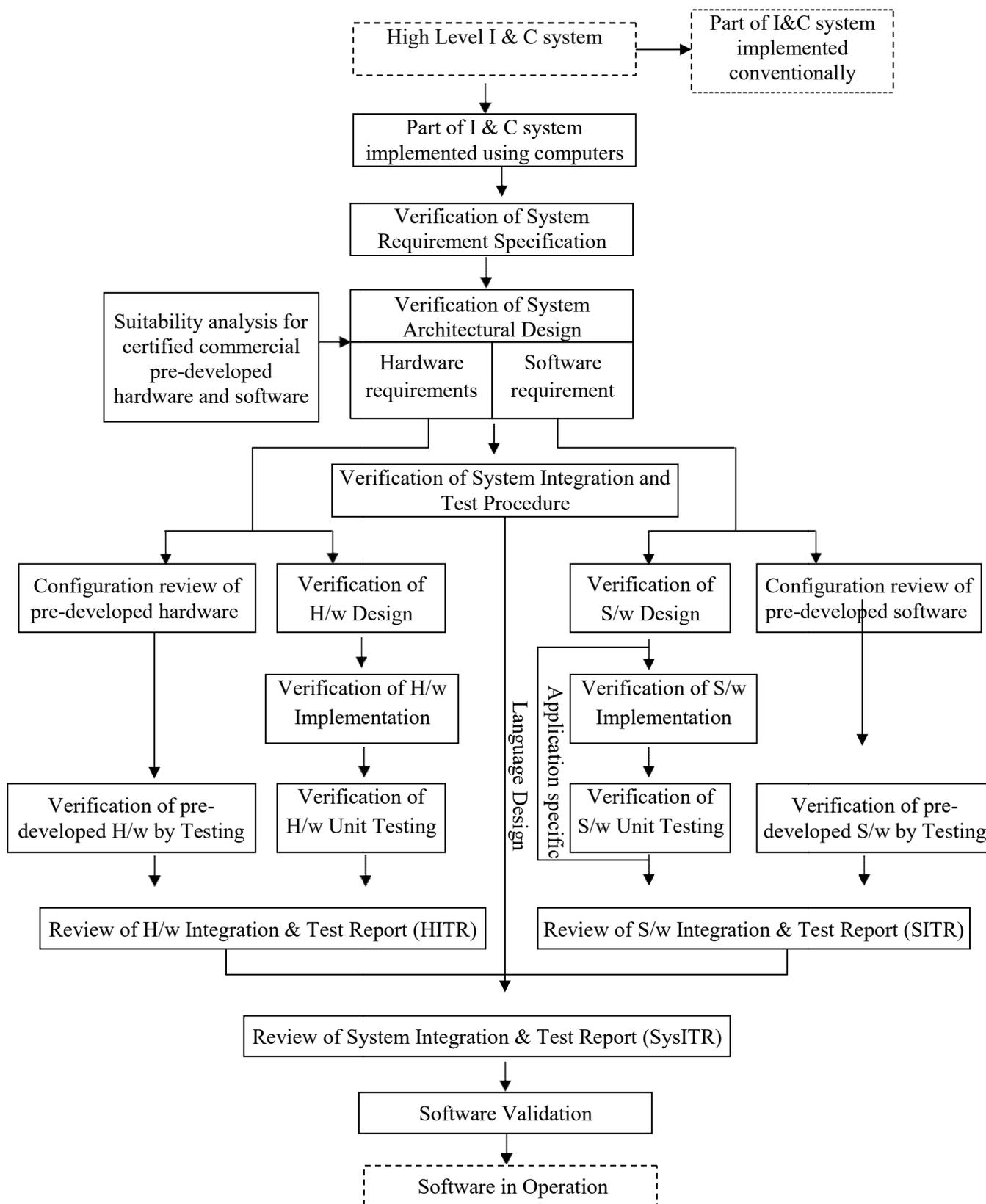


FIGURE 11: System Verification & Validation Process

## 7.0 CONCLUSION

More than 100 Real-Time Computer-based control systems for Power Plant Control & Process applications have been developed and tested with Field Signal Simulator. Dynamic testing has ensured timing cycles and speeded up the testing time drastically. This method of testing can be adopted for any Microprocessor, Microcontroller, and computer-based systems.

## 8.0 FUTURE ENHANCEMENT

The process of inter-connecting the FSS to the system under test is tedious and cumbersome since it involves the connection of discrete wires. This type of wiring gives a lot of contact problems. Tracing the problem and rectifying is a time-consuming process.

To reduce the inter-connection time, it is proposed to make suitable arrangements at FSS and the system under test so that Flat cables can be used to quickly inter-connect the systems. This requires modification of interface terminal blocks at the micro-computer system under test by providing one more IDC header on IFM. At the FSS end screwed terminals are to be inter-connected to an additional IFM with an IDC connector. Thus, the IDC connector is made available at both ends across which a Flat cable can be connected. This will ensure a drastic reduction in overall testing time and better time utilization of the FSS.

Currently, the test programs are written so that the system gives the output details for the specified inputs. The quality control engineers are expected to compare the test results with the expected values and decide whether the system has passed or failed.

In the next phase of improvement, it is proposed to modify the test programs such that the FSS by itself compares the test results with the expected values and declares to the quality control engineers whether the systems have passed or failed. This will ensure a reduction in testing time and human errors.

Currently, a limited type of signals namely Current, Voltage, Thermocouple, RTD, LKD, Synchro, and Encoder type of inputs can be tested. It is proposed to enhance this capability for other types of inputs like flow, pressure, etc.

Complex C & I system with a large number of I/Os. The I/O capacity of each signal is expected to be enhanced by the addition of boards of various types. This will be useful for testing.

## 9.0 BIOGRAPHIES



Shri. A.K. Asthana was born in Hyderabad, Andhra Pradesh, on June 09, 1955. He graduated in Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, India. He joined as a Graduate Engineer Trainee in Electronics Corporation of India Limited, Hyderabad in the year 1979. Since then, he

had been working on C & I systems for Pressurized Heavy Water and Fast Breeder Reactors. He worked as General Manager and retired in the year 2015, Control and Systems Group of Electronics Corporation of India Limited, Hyderabad. He published a paper entitled "PFBR and PHWR Reactors-C& I Perspective" in ISA – POWID – INDIA in 2010.



**Dr. S. Viswanadha Raju,** Presently he is working as Professor of Computer Science and Engineering, JNT University, KUKATPALLY, Hyderabad, India. He has completed M.Tech.in CSE from Jawaharlal Nehru Technological University, Hyderabad, India. He was awarded Ph.D. in CSE by

ACHARYA NAGARJUNA University, Guntur. He was Head of CSE, JNT University Hyderabad from September 2010 to December 2011. Director, MCA (Accredited by **NBA**), GOKARAJU RANGARAJU Institute of Engineering and Technology (GRIET), Hyderabad, from July 2009 to July 2010 and also HOD of CSE/MCA (CSE-**Twice Accredited by NBA**) from July 2003 to April 2009. Organized as Convener for International Conference on Advanced Computing Technologies (ICACT2008) at GRIET and Member governing body in GRIET from April 2009 to July 2010. He was awarded Best citizens of India from IPH, Delhi. He has attended many national and international conferences / seminars and presented papers and conducted several workshops / seminars / conferences supported by AICTE, DST, TCS, etc. He published many research articles in various national and international journals and was actively involved in research projects. He is a Life member in different Professional bodies such as ISTE, CSI, IETE, ACM-CSTA, and IACSIT. He is a Member of the Board of studies for CSE in different Autonomous Engineering colleges.



Ms. Sri Lakshmi Peyyala presently, working as Technical Manager in Electronics Corporation of India Limited, Hyderabad, India. She Graduated and Post-graduated in Computer Science Engineering (CSE) from Jawaharlal Nehru Technological University (JNTU) Hyderabad, India. She joined as a Graduate Engineer Trainee in

Control & Automation Division, ECIL Hyderabad in 2007. Since then, she has been working on C & I systems for Prototype Fast Breeder Reactor, Area Radiation Monitors and Radiation Contaminated Monitors. At present, she is pursuing doctoral research process on Project Management and Leadership impacted by ISO 9001:2015.

#### 10.0 ACKNOWLEDGEMENT

A special thanks to our Chairman & Managing Director Rear Admiral **SANJAY CHAUBEY** (Retd.), Chairman & Managing Director and **Shri Y.S. MAYYA**, Outstanding Scientist and Ex. C&MD of the Electronics Corporation of India Limited (ECIL), Hyderabad, India and **Dr. M. SREENIVASA RAO**, Professor, School of IT, JNTUH, KUKATPALLY, Hyderabad. We would like to thank all the other high executives, colleagues, staff members, teaching, non-teaching, and librarians who have extended their timely help and support to complete my task easily.

## 11.0 REFERENCES

- [1] AERB Safety Guide for Computer-based systems–  
AERB/SG/D25
- [2] PROJECT Hand Book
- [3] User Manual for Field Signal Simulator
- [4] Real-Time Computer-Based Control Systems for  
Prototype Fast Breeder Reactor
- [5] IEEE Recommended Practice for Software Design  
Descriptions – IEEE Std 1016-1998
- [6] IEEE Recommended Practice for Software  
Requirements Specifications–IEEEStd830–1998.