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Wireless Charging of Far-Field Wireless Sensor with Variable Duty Cycle

Mr. P. J. Sonawane, Prof. A. B.Sapkal

E & TC Department, SSBT's COET Bambhori Jalgaon

Abstract- This paper shows far-field wireless powering for low-power wireless sensors. Sometimes in many applications where the sensors are used, is difficult or impossible to change the batteries of sensor unit because we don't know the exact position of the sensors or sensors are mobile. Here expected radio-frequency (RF) power densities is in the range of 20–200-μW/cm^2, overall size of sensor is small which transmit data at low duty cycles. For these type of applications low-power nondirective wireless powering is appropriate for sensors. The power is provided to the sensor platform through an antenna which receives incident electromagnetic waves in the gigahertz frequency range. This antenna gives the energy to a rectifier circuit which charges a storage device (e.g., thin-film battery) through an efficient power management circuit. The entire platform, including sensors and a low-power wireless transmitters are controlled through a low-power microcontroller. For low incident power density levels, code sign of the RF powering and the power management circuits is required for optimal performance. The power management circuitry are presented with integrated antenna rectifiers operating in the 1.96-GHz cellular and in 2.4-GHz industrial – scientific – medical (ISM) bands.

Index Terms- Ractifier, Radio frequency (RF), Rectenna, Sensor, Wireless power transmission.

I. INTRODUCTION

Over 100 years ago, wireless power transmission concept began with the ideas and demonstrations by Tesla. But Tesla was not successful at implementing his wireless power transmission systems for commercial use. In the 1920's and 1930's the experiments and researchers of Tesla's in Japan and the U.S. promoted wireless power transmission. In the 1950's the modern era of wireless power transmission began with the advancement of high-power microwave tubes by Raytheon Company, Waltham, MA. A 15-kW average power-band cross-field amplifying tube was developed in 1958, which measured overall dc-to-RF efficiency of 81%. In 1960's the first receiving device is emerged for efficient reception and rectification of microwave power. A rectifying antenna, or rectenna, was developed which consist of a half-wave dipole antenna with a balanced bridge or single semiconductor diode placed above a reflecting plane. From the 1960's through the 1970's the conversion efficiency of the rectenna continued to increase at 2.45 GHz. Conversion efficiency is determined by the amount of microwave power that is converted into dc power by a rectenna element.

The greatest conversion efficiency ever achieved by a rectenna element in 1977 by Brown, Raytheon Company. A 90.6 % conversion efficiency was recorded using a GaAs–Pt Schottky barrier diode, with a 8W input microwave-power level. The dipole and transmission line of this rectenna element used aluminum bars for their construction. Later, a rectenna design was developed with a printed thin-film at 2.45 GHz where conversion efficiencies of 85% were achieved. In 1991 researchers at ARCO Power Technologies, Inc., Washington, DC, developed a 72% efficient rectenna element at 35 GHz to reduce the transmitting and rectenna aperture areas and increase the transmission range. However, components required for generating high power at 35 GHz are expensive and inefficient. To decrease the aperture sizes without sacrificing component efficiency, technology development at the next higher ISM band centered at 5.8 GHz.This frequency is attractive for beamed power transmission over 2.45 GHz due to smaller component sizes and a greater transmission range.

In many applications the electronic devices operate in conditions where it is difficult costly, inconvenient, or impossible to change a battery or provide wired power. Some examples are sensors for health monitoring of patients [1], [2], aircraft structural monitoring [3], [4], sensors in hazardous environments, sensors for covert operations, etc. This paper focuses on improving efficiency of providing power wirelessly to a low-power wireless sensor platform with an electrically small antenna.In this paper "Low power" refers to less than 200 μW/cm^2 of incident power density of an electromagnetic wave in the radio-frequency (RF) range of the spectrum [5].

We specifically consider frequencies that are in unlicensed industrial–science–medical (ISM) bands, such as 2.45 GHz. The codesign methodology for the power reception circuit and power management circuit is developed to achieve highest system efficiency. The block diagram is as shown in fig. 1 where both communication and powering were performed independently in the 2.45-GHz industrial-scientific-medical (ISM) band. Different frequencies can also be used, as in [10], where 5.8 GHz was used for powering and 2.45 GHz for data transmission. Previous work in this field ranges from very high power values, e.g., powering a helicopter for up to 10 h of flight with a high-power microwave beam [11] to reception of very low radio-wave power densities in the 5-μW/cm^2 range with large aperture antennas [12]. These and other related applications, e.g., [13]–[15], were aimed at directive power beaming where a narrow-beam antenna transmits power in a well-defined direction toward the power receiving device. The antenna arrays deliver power to a single

rectifier, whereas in the work presented here, there is one rectifier per antenna element.

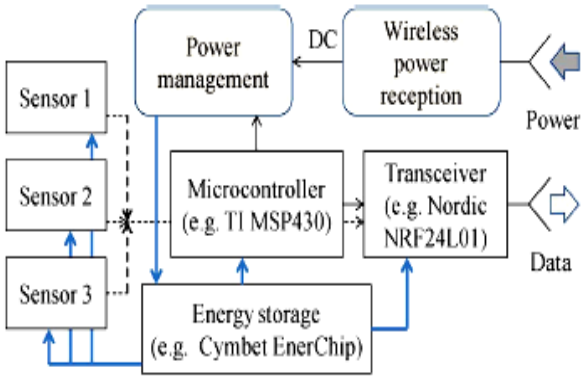

Figure 1: Block Diagram of Wireless Powering System.

As shown in the block diagram the function of antenna is to received RF power from the transmitter and provide it to the rectifier circuit. The rectifier is then rectified it i.e. to convert received RF power into DC power. The power management circuit works as a buffer between wireless power reception block and energy storage device. This circuit matches the impedance between wireless reception block and energy storage device. It receive the DC power from rectenna and provide it to the energy storage block i.e. charges the battery or capacitor available in energy storage block. The energy storage unit provides stored energy to sensor, transceiver and microcontroller unit. The function of transceiver unit is to transmit and receive the data. Here both power transmission antenna and transceiver use same frequency band i.e. 2.45 GHz ISM band. Separate frequency band can also be used. The microcontroller unit controls the operation of whole wireless powering system. It continuously check the power available in the energy storage device and power required from the power management circuit and according to that control the duty cycle of the operation and prevent the system from damaging.

Far-field powering implies plane-wave propagation between antennas at longer range. It can be done without line of sight, and is less sensitive to the orientation and position relative to the transmitting antenna. The work in this brief addresses a method for improved far-field powering efficiency at low incident power densities by the integrated design of the power reception device and the power management circuit. An antenna integrated with a rectifier is known as "rectenna" receives arbitrarily polarized radiation at one or more of the chosen frequencies at levels below 200 μW/cm^2. A digitally controlled power converter manages the dc output in such a way that it always presents close to an optimal dc load to the energy storage device, which provides power to the microcontroller, sensor, and data transceiver. Data transmission is the most power-consuming task and is not continuously done. If there is not enough stored energy, the data cannot be transmitted and there is a danger of damaging the storage device. Therefore, the available rectified RF power and the available energy stored are monitored in a closed-loop system and adjust the duty cycle of data transmission.

II. RECEPTION OF RF POWER

In the far field a plane-wave incident from a transmitter is used to deliver power remotely to the sensor. The relevant input quantity is power density S_{RF}, and the received power at the antenna terminals will be $S_{RF}.A_{eff}$, where A_{eff} is the antenna effective area, usually smaller than its geometric area. Therefore, the rectified power available to be delivered to the storage element (battery or capacitor) is

$$P_{DC}(\theta, \varphi) = \eta_{RF} - DC_{(PRF)} \cdot A_{eff}(\theta, \varphi) \cdot S_{RF}(\theta, \varphi)$$

where the rectification efficiency is a function of received RF power due to the nonlinearity of the rectification process. In addition, the above quantities depend on frequency, and the quantity should be integrated over all incidence angles (θ, φ). When the diode rectifier is impedance matched to the antenna at the predicted power level since the diode impedance varies with power level then the highest rectification efficiency is obtained. The impedance for optimal rectification is not the same as that for an optimal reflection coefficient and needs to be characterized using nonlinear modeling or measurements. In the method presented here, both a nonlinear model using harmonic balance in Agilent's ADS tool and an experimental model using a load-pull method are performed and compared. Varying RF power levels are incident on the rectifier while the RF impedance is changed with the tuner and the dc load impedance varied at a given frequency. For each RF power and dc load, contours of constant rectified dc power are measured as the RF impedance presented to the rectifying element varies from practically a short to an open one. An example of measured data for a Skyworks Schottky SMS-7630-79 diode single-ended rectifier is shown in Fig. 3 for two dc loads and constant input RF power of 0 dBm. The plots show the imaginary and real parts of the reflection coefficient of the diode referenced to a 120-Ω normalization impedance value for plotting convenience and given by:

$$\rho = (Zrectifier - 120) / (Zrectifier + 120).$$

The data in Fig. 2 are useful for optimizing the RF impedance presented to the diode for a given power level for the design of the RF portion of the circuit. However, in order to design the power management circuit that takes the variable rectified power and optimally charges a storage element, the data are plotted, as A photograph of the back side of a linearly Polarized patch antenna designed for the 1.96 - GHz cell phone band is shown in Fig. 3(a). The antenna and matching circuit is fabricated on a Rogers 4350b 0.762-mm-thick substrate, and the antenna patch dimensions are 38 mm × 39 mm, with a coaxial feed 15-mm offset from the center. A Skyworks Schottky diode is connected to the antenna with a matching circuit. The antenna is simulated using Ansoft HFSS, with good agreement to measured data. Dual-polarized antennas are also possible, as shown in [10], where each diode rectifies power received in one polarization. In a realistic outdoor multipath environment, polarization is random, thus rectifying two orthogonal polarizations independently, and adding the resulting dc power increases

overall efficiency [5]. The patch antenna ground plane results in preferential radiation in the half-space above the ground, but

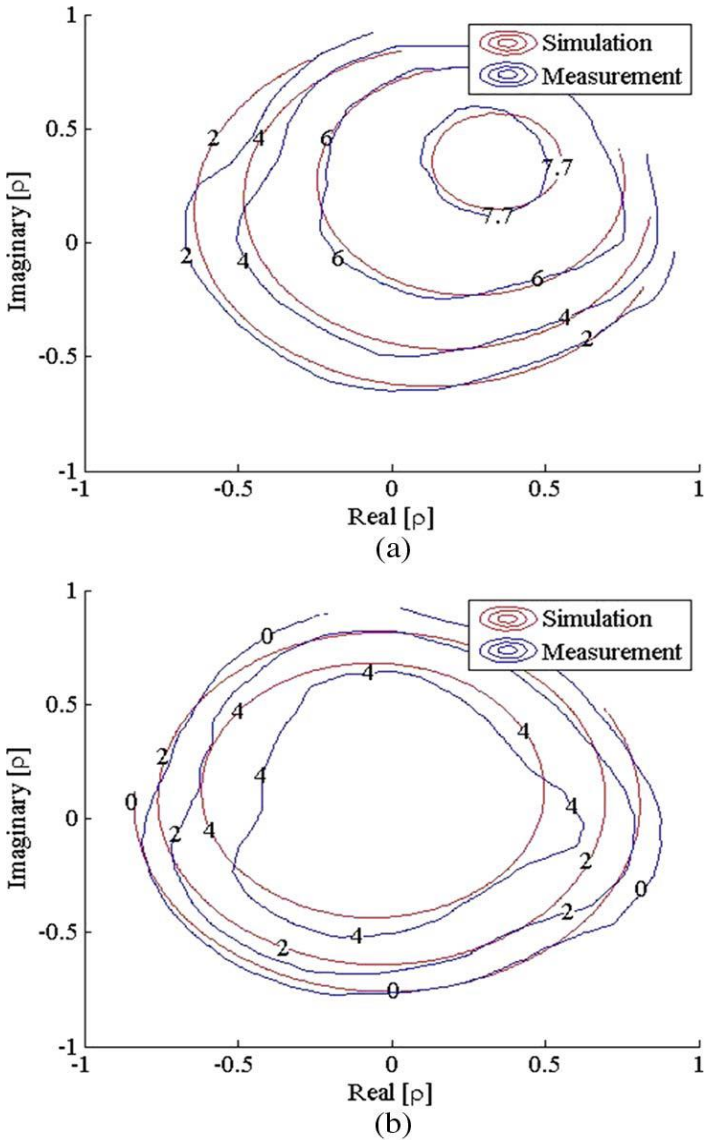

Figure 2: Measured and simulated constant dc power contours of the real and imaginary parts of the RF reflection coefficient of the diode for (a) *RL* = 460 Ω and (b) *RL* = 60 Ω.

omnidirectional arrays of dipoles such as the one shown in Fig. 3(b) are also possible although not a topic of this brief.

The measurements of the integrated rectifier and antenna are performed in an anechoic chamber. The procedure for characterizing the rectenna consists of the following steps.

1) Calibrate power densities at the plane of the rectenna with calibrated antenna of gain G_R

$$S = P_R 4\pi / \lambda_2 G_R \quad (1)$$

2) Calculate RF power incident on rectenna, assuming that the effective area is equal to the geometric area of the antenna, which is an overestimate

$$P_{RF} = S \,.\, AG \quad (2)$$

3) Measure dc power as a function of dc load resistance.

4) Calculate RF to dc conversion efficiency, which will be an underestimate

$$\eta_{RF} - DC = P_{DC(RL)} / P_{RF} \quad (3)$$

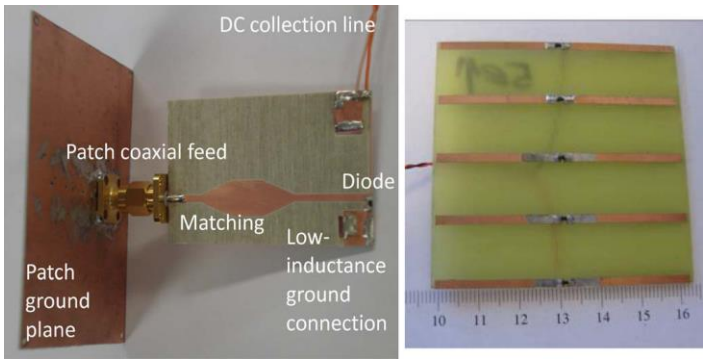

Figure 3: (Left) Photograph of a 1.96-GHz linearly polarized patch antenna with a diode connected through a microstrip matching circuit.

When quantifying rectenna efficiency for aperture-type antennas such as a patch, the total input RF power is not easy to quantify from either measurements or simulations in a free space situation. While the antenna gain, and thus effective area, can be easily found from full-wave electromagnetic simulations, the rectifier loading is not taken into account and the gain is usually calculated for a 50-Ω feed impedance value. Care must be taken when calculating the RF-to-dc conversion efficiency of rectennas since P_{DC} is a function of antenna gain.

III. Antenna Design

The design of the proposed antenna and its parameters are depicted in Fig. 4. The parameters of the antenna were obtained using finite element commercial software [16]. The square patch antenna (A = 33.6 mm) is printed on a 3.175-mm-thick Duroid 5880 (Ɛr = 2.2) top substrate. The single microstrip feeding line is printed on a 1.524-mm-thick Arlon 25 N (Ɛr = 3.38) substrate at the backside of the antenna. The crossed slots etched on the ground plane are accurately centered below the radiating element. Four coupling points localized between the patch antenna and the microstrip feed line and are serially fed by the microstrip feeding line. Due to the quarter-wavelength distance between the coupling points, a 90 phase difference appears.

The antenna is fed on Port 2. At a given time, the opposed coupling points on Slot 2 have a peak of magnetic excitation current in phase while the opposed coupling points on Slot 1 have a null of magnetic current. After a quarter-period, the excitation currents are totally inverted. Opposed coupling points have a null of magnetic current on Slot 2 and are maximum on Slot 1. This provides two linear perpendicular polarizations with a phase difference of 90. The polarization emitted by the antenna is then LHCP. The sense of the polarization is achieved by selecting one of the two excitation points, terminating the other with a 50- resistive load. The RHCP is obtained if the excitation point is located on Port 1.

The antenna is first designed separately from the rectifying circuit. Due to the superimposed layers of the antenna, an air gap of 120 m above the ground plane has been taken into account in simulations. The DCP antenna is fed using a 50- characteristic

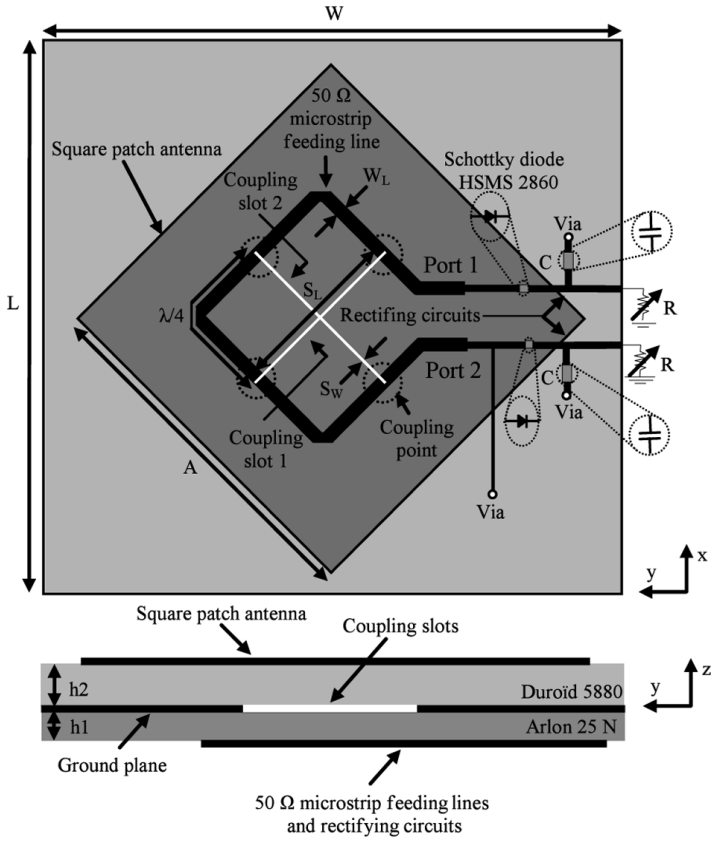

Figure 4: Layout of the DCP Rectenna.

impedance microstrip line. The measured CP antenna gain is 5.7 dB at 2.45 GHz when the RF generator is connected on Port 2. In this configuration, numerical simulations give 6.8 dB LHCP gain and -25.24 dB RHCP gain. The LHCP gain is here significantly higher than the RHCP one and then confirms the sense of the polarization emitted by the antenna. At 4.9 GHz, the simulated LHCP gain is -10.14 dB. The measured isolation between feeding ports is -20 dB, assuming that both accesses are correctly isolated.

The DCP has good circular polarization characteristics in a large range of elevation angles. This property is particularly attractive and can enhance the efficiency of the rectenna in the case of recycling ambient RF energy with arbitrary polarized radiations and angle of incidences. Radiations patterns have been measured in an anechoic chamber at 2.45 GHz in the xz plane with a linearly polarized horn antenna as an emitter. Due to the circular polarization properties, copolar and cross-polar components have nearly the same level. They exhibit a measured difference of 0.7 dB at its broadside.

IV. DESIGN OF RECTIFIER

A study of different rectifier designs is done and the voltage doubler rectifier configuration is chosen [17]. Fig. 5 and fig .6 shows the conventional voltage doubling rectification circuit and the proposed floating-gate rectification circuit. For the floating-gate rectification circuit, floating-gate devices are used to create a gate-source bias to reduce the threshold voltage loss of the MOS transistor.

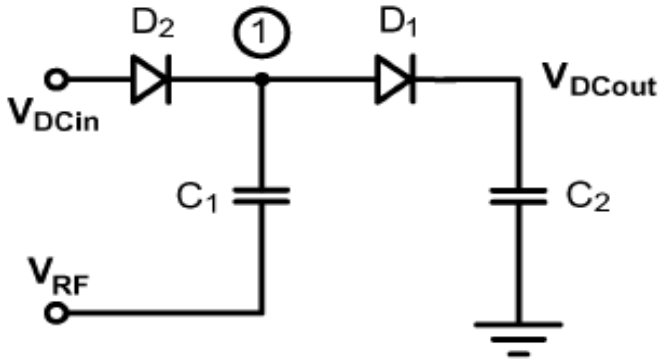

Figure 5: Conventional Voltage Doubler Rectifier.

A. Conventional Voltage Doubler Rectifier

The voltage doubler rectifier structure is considered for the design of the RF-DC power conversion system because it rectifies the full-wave peak-to-peak voltage of the incoming RF signal and it can be arranged in cascade to increase the output voltage. The voltage doubler rectifier in Fig. 5 consists of a peak rectifier formed by D_1 and C_2 and a voltage clamp formed by D_2 and C_1 . The voltage clamp and the peak rectifier are arranged in cascade configuration to provide a passive level shift in voltage before rectification. In the negative phase of the input, current flows through diode D_2 while D_1 is cutoff. The voltage across diode D_2 stays constant around its threshold voltage and the voltage at node 1 is charged to Vth_2 . At the negative peak, the voltage across capacitor C_1 is $Vamp - Vth_2$ (where Vamp is the amplitude of the input signal.) In the positive phase of the input, current flows through diode D_1 while D_2 is in cutoff. The voltage across capacitor C_1 remains the same as the previous phase because it has no way to discharge. At the positive peak, the voltage across D_2 is $2Vamp - Vth_2$. Since D_1 is conducting current to charge C_2 , the voltage at the output is a threshold voltage below that across D_2 , i.e., the voltage at the output Vout is $2Vamp - Vth_2 - Vth_1$.

B. Floating-Gate Voltage Doubler Rectifier

The floating gate devices may be designed to passively reduce the threshold voltage of the rectifier circuit. In a floating gate device, when charge is injected into the floating gate of the transistor, it remains in the gate oxide because of the high impedance provided by the oxide layer. There are previous methods designed to compensate for the threshold voltage drop in voltage rectification circuits [18], [20]. The threshold reduction method shown in [18] requires the input voltage to be sufficiently large to start up the circuit. This method also requires a bias resistor R_b which generally has resistance in the megaohm range (i.e., large physical size). Although the static power dissipated from this resistor is minimal, it causes a bias voltage much less than the desired threshold voltage. The voltage drop

across a diode tied transistor under 10 nA bias is much different than one drawing 10 A of current, this voltage difference is typically 100 mV for every decade of current difference, yielding an effective threshold of a few hundred millivolts. The threshold reduction technique in [19] suffers from the same constraint, as it

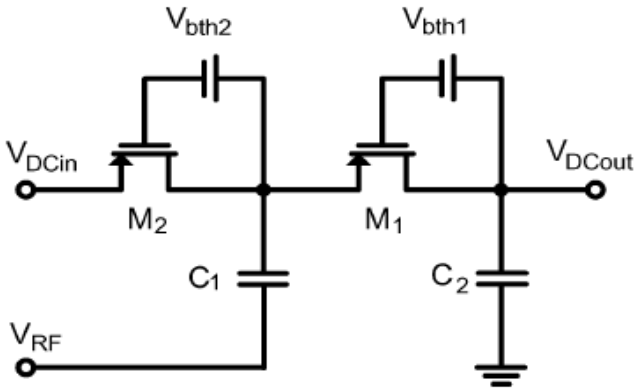

Figure 6: PMOS Floating-Gate Rectifier.

uses diode-tied transistors biased at 2 nA to generate bias voltages for diode-tied transistors drawing current in the microamp range. This method would also require extra circuitry to generate a voltage bias and differential clock which requires a secondary battery. Zero-threshold transistors may also be used for voltage rectification but they only have zero threshold for a small current range. The floating-gate rectifier technique allows the threshold of the rectifier circuits to be programmed and can be optimized to operate over a wide range of currents. For the floating-gate rectifier circuit, the overall rectifier architecture is the same as the voltage doubler rectifier circuit. The diodes D_1 and D_2 are replaced by diode-tied floating gate transistors. The gate oxide is a very good insulator which keeps the charge from leaking off in the floating gate [21]. To design a floating gate device in a standard CMOS process, a MOS capacitor is placed in series with the gate of the diode tied transistor as shown in Fig. 6. The gate of the diode-tied transistor and the gate of the MOS capacitor are connected together to form a high-impedance node to trap charges in the floating gate. The charge in the floating gate is therefore fixed which results in a fixed voltage bias across the MOS capacitor. The charges that are trapped inside the floating gate device act as a gate-source bias to passively reduce the effective threshold voltage of the transistor.

The floating-gate devices need to be initially programmed to reduce the threshold voltage of the rectifier, thus enhancing the power conversion efficiency. The charge on the floating gate can be injected via Fowler – Nordheim (F-N) tunneling when the rectifier is not operating, or it can be charged by injecting a relatively large sinusoidal signal to the input of the rectifier at any time. The F-N tunneling technique charges the floating gate to the desired voltage much faster, but the amount of charge is harder to control and also, additional circuitry is needed to inject or remove charge from the floating gate. Similar to programming a non-volatile Flash EEPROM, the programming node is driven by a high-voltage pulse to force a sharp bend in the energy band diagram of the floating-gate device. This enables charge to enter the insulated floating-gate by means other than the mechanism of F-N tunneling. The applied programming sinusoidal input voltage has amplitude larger than the threshold voltage of the transistor used for rectification. Charge is injected into the floating gate via the parasitic capacitance between the gate-source and gate-drain junction of the transistor and by hot electron effects. The large sinusoidal signal is externally generated and applied directly to the input of the rectifier until the output reaches an optimal point. If the floating-gate node is over charged, a negatively biased sinusoidal wave may bring it back to the optimal point. The sinusoidal signal can be applied in pulses with peak voltages between 5–6 V with 2.5–3.0 V DC bias or by a continuous train of signals at lower voltages and bias, depending on the duration of the pulse train. The programming pulse does not need to be sinusoidal, but as the pulse is applied to the input node which is high, the pulse will be transformed to more of a sinusoidal signal. By applying a sinusoidal signal, the amplitude of the applied pulse can be better controlled. In this work, all floating-gate programming nodes are capacitively coupled and can be programmed simultaneously from the same programming pin, with all other circuitry grounded, via a F-N tunneling technique, and by the application of the sinusoidal signal at the input nodes when the rectifier is operating. The floating-gate rectifier is programmed with iterations of 20 pulses with a 5 ms trigger, 5 V amplitude and 2.5 V DC offset and repeated until the output voltage is at the maximum point for a wide range of currents. If the floating - gate is over charged, 10 deprogramming pulses with 5 ms trigger time, - 6 V and - 3.0 V DC offset are injected at the programming node to recover charge on the floating-gates.

With the floating-gate device, the threshold voltages of the diode-tied transistors M_1 and M_2 are reduced by creating a gate-source bias. The gates of transistors M_1 and M_2 in Fig. 6 are high-impedance nodes so any charge trapped in the floating gates can be retained for a long time. Retaining charge in floating-gate devices is critical to the useful lifetime for the power conversion circuit under discussion. With the 70 angstrom oxide thickness in the 0.25 m CMOS process, the device retains charge in the floating gate in excess of 10 years for normal operation at room temperature [22]. However, the performance of the rectifier circuit may reduce slightly as charge is leaked from the floating gate. During fabrication, the residual charge trapped in the floating gate may also affect the threshold voltage of the rectifier circuit, hence the floating gate must be programmed to account for these residual charges. Removal of residual charge may be done initially with the F-N tunneling method, which is a high-voltage pulse applied to a separate control gate of the floating-gate device.

V. POWER MANAGEMENT CIRCUIT

The purpose of the power management circuit is to act as a buffer between the rectenna power source and the energy storage device to act as an ideal buffer in the harvesting application, the converter must perform three functions:-

1) create at its input port the optimal impedance match to maximize the rectenna efficiency η_R over the full range of incident power densities P_{RFinc}.

2) Transfer the harvested energy with ideally no loss to the energy storage element over the full range of rectenna output voltages Vdc and energy storage charge states.

3) monitor the energy storage and provide charge control and protection as appropriate for the energy storage used (battery or capacitor). Since the efficiency of the rectenna depends on the matching behavior of the converter, and the efficiency of the converter depends on the operating conditions of the rectenna

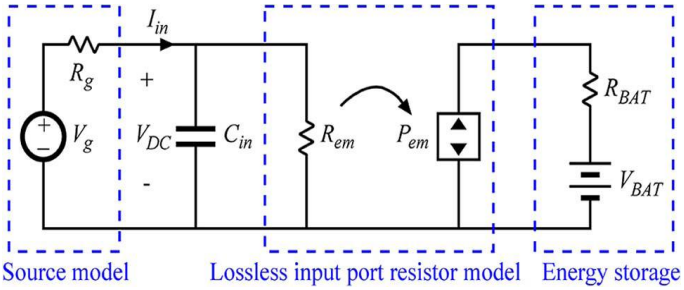

Figure 7: Ideal Lossless Input Port Resistor Model of the Power Converter.

and the energy storage device, it is best to codesign these blocks for the given application and expected condition.

A. Matching to the Rectenna

The first function of the converter is to maximize the rectenna efficiency by creating a converter input port that emulates the optimal load impedance of the rectenna. To provide a measure of the converter performance in this area, it is useful to define a matching efficiency η_M as :-

$$\eta_M = \frac{P_{R,dc}}{P_{R,dc\,max}}$$

where $P_{R,dc\ max}$ is the rectenna dc output power with an optimal load. The filter integrated in the rectenna creates a dc port and reduces the rectenna model from the perspective of the power converter to a Thevenin equivalent, and the rectenna output impedance reduces to an equivalent resistance. Thus, the optimal load to the rectenna is a dc resistance, apparent in the measurement results, where the load value at maximum rectified power is about 300 W over a wide range of incident power densities. The ideal converter behavior is depicted in Fig.7 The converter is modeled with an input port that emulates a resistor Rem and an output port that transfers all of the power from the input port to the energy storage device, shown as a battery model. This behavior is similar to that commonly used in power converters for alternating current/direct current (ac–dc) power conversion with power factor correction (PFC), although the PFC goal and the high voltage and power levels in those applications are entirely different from the harvesting application.

The challenge in the low-power harvesting application is to perform the behavior of with minimal control circuit overhead so that the control losses can be kept small when compared to the power being processed. This rules out many of the advanced control circuits and techniques commonly applied at higher power levels. A boost converter is selected to provide the required step up from typical rectenna voltages of tens to hundreds of millivolts to typical battery voltages, from 2 to 4 V.

B. Boost Converter as A Resistor Emulator

The technique applied in fig.8 is to operate a boost converter as an open-loop resistor emulator, thus allowing the converter to naturally track the rectenna MPP, $P_{rect\_out\_max}$, with very little control overhead. Once the converter has been tuned to match the optimal load resistance for the rectenna, maximum power can be harvested $P_{rect\_out\_max} \approx P_{rect\_out}$ over a wide range of incident RF power densities S_{RF} without modifying the converter behavior. The initial tuning operation to set the converter emulated

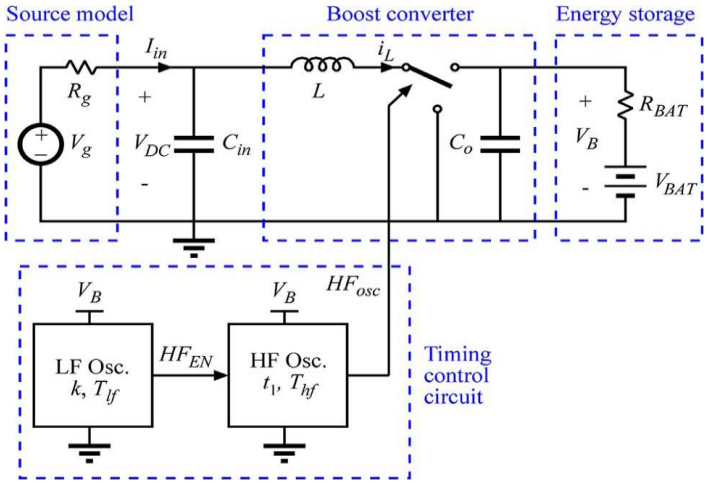

Figure 8: Boost Converter Implementation

resistance could be performed once in the manufacturing process or as an infrequent recalibration procedure. The choice of parameter settings for the given converter is based on the expected range of input power levels, desired emulated resistance, and output voltage. A power converter design example is given here together with details on each of the major design steps for providing an interface between the patch rectenna of with output characteristics shown and a 4.2-V thin-film battery.

C. Selection of Control Component

To control the converter, an HF oscillator and an LF oscillator are used with emphasis on the selection of components with the lowest power consumption. The HF resistor-set oscillator (LTC6906) has a fixed duty cycle (50%). This duty cycle ensures DCM operation for Vo/Vin > 2. When powered on at the beginning of each LF period, there is a settling time t_{settle} before the output of the oscillator is enabled. This output drives the MOSFET in the converter. Therefore, adjusting the frequency $1/T_{hf}$, changes the value $t_1 = T_{hf} / 2$ of and thus the emulated resistance seen by the input source. The power consumption of the LTC6906 HF oscillator is the value used as P_{PWM} in the power loss calculations. To perform the pulsing operation of the converter, a LF oscillator is built around a low power comparator (LMC7215). This oscillator has an adjustable positive duty cycle D_{lf} that affects the k parameter. The HF oscillator is directly powered from the LF oscillator output. Given a converter input power level , changes in power loss are calculated and are swept over a range of values and is solved for so that the approximate desired Rem = 750 ohm is achieved. After these simulations are run at different power levels, the converter efficiency $\eta_{converter}$ is analyzed as a function of t_1 and L. Next, the calculations are rerun with the fixed L to select the appropriate t_1. The value of k

is then determined by the desired Rem. The selection is optimized for the lower power levels due to the emphasis of this work on demonstrating RF energy harvesting at very low S_{RF} . Parameters t_1 and k are chosen to be 18 s and 0.06, respectively.
The key to achieving a good match to the rectenna is found in the timing control circuit and the resulting inductor current waveform iL. The boost converter operates by transferring energy through the inductor L, and as a result, the low-frequency behavior of the input and output ports is determined by averaging current waveforms. As shown in Fig. 9. two types of waveforms can be generated. In both waveforms, the converter is run in a pulsed mode, where multiple high-frequency periods T_{hf} are repeated consecutively, then the converter is turned off with no gating signals for a percentage k of a low-frequency period $T_{lf.}$ The sequence is then repeated every low-frequency period Tlf . Fig. 3.9 (a) shows a discontinuous conduction mode (DCM) waveform with a fixed T_{hf} and a third time interval t_3 where there is no current in the inductor. It is Shown the DCM mode results in an input port emulated resistance of :-

$$R_{em;DCM} = 2.L.T_{hf}.(M-1) / t_1^2. k .M$$

Where M is the ratio between the output and input voltages of the converter $M = V_B / V_{dc}$. Thus, the averaged or low frequency model of the boost converter in DCM is an emulated resistance R_{em} given by above equation, and the resistance value is controlled by the timing control circuit parameters t_1, k, and Thf .These parameters can be selected to optimize efficiency over a desired range of voltages and power levels. Fig. 3.9 (b) shows a critical conduction mode (CRM) waveform, where period Thf is defined by the zero crossing of i_L and there is no t_3. The emulated resistance in CRM is given by :-

$$R_{em,CRM} = 2. L / t_1. k$$

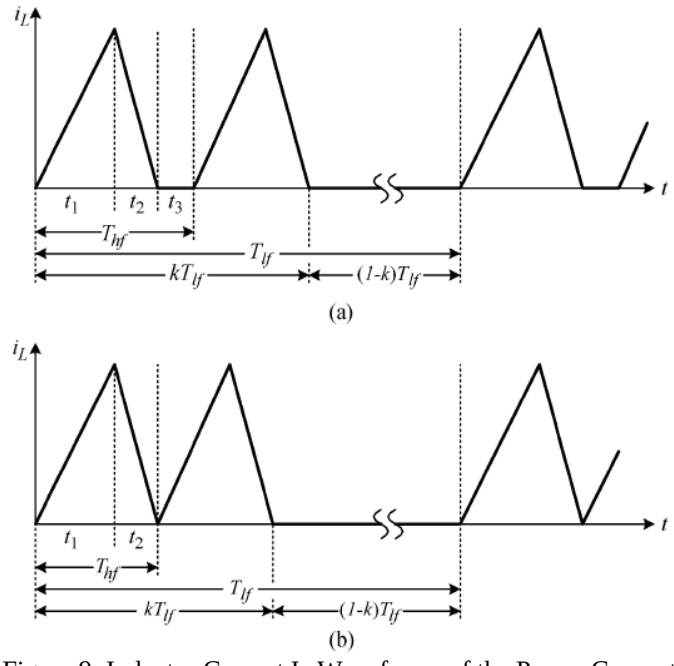

Figure 9: Inductor Current I_L Waveforms of the Power Converter for Two Operating Modes: (a) DCM and (b) CRM.

Two important results in above equation are that the emulated resistance is independent of the input and output voltages and it can be shown that with no t_3 interval the converter operation is more efficient. However, CRM operation requires either active inductor current sensing or prediction of time t_2, both of which require additional timing control circuit overhead.

VI. CONCLUSION

A rectenna design and optimization methodology utilizing reciprocity theory and combining EM simulation and harmonic balance is proposed. The Thevenin equivalent circuit parameters of the rectenna in the receiving mode are efficiently computed from EM simulation of the antenna in the transmit mode. A compact dual-polarized aperture-coupled patch rectenna was designed, able to receive arbitrarily polarized signals by combining the dc output from two voltage doublers connected at two orthogonal polarizations.

Low-power RF rectennas are shown to exhibit maximum power points at near constant optimal dc load resistance over a decade of output power. A boost converter topology operating in open-loop fixed-frequency DCM is used to achieve near constant emulated resistance with simple open-loop control based on low-power timing circuits. The converter control variables are selected based on a detailed efficiency analysis to minimize power losses and achieve the desired emulated resistance. The proposed resistor emulation approach to low-power energy harvesting provides a simple solution for maximizing output power in harvesting applications with variable source power.

Microcontroller and other discrete components can be used to construct a smart power converter capable of extracting near maximum power from a rectenna. The design can also be easily scaled to different power levels by changing the size of the rectenna array. High conversion efficiency will be maintained due to the adaptive optimization algorithms. A rectenna emulator circuit was designed to show how the developed low – frequency model can be used to emulate any rectenna design as well as in testing and debugging power management circuitry.

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AUTHORS

First Author – Mr. P. J. Sonawane, ME Ist (E & TC), SSBT’s COET Bambhori Jalgaon. Email id - prijesh.s87@gmail.com.
Second Author – Prof. A. K. Sapkal, SSBT’s COET Bambhori Jalgaon. Email id - akshadasapkal@gmail.com
Correspondence Author – Mr. P. J. Sonawane, ME Ist (E & TC), SSBT’s COET Bambhori, Jalgaon. Email id - prijesh.s87@gmail.com. +919975406185