ISSN 2250-3153

Low Power CMOS Phase Frequency Detector - A Review

Ms.Vaijayanti Lule, Prof (Ms).Vrushali G Nasre

Abstract- This paper describes a performance and comparison of different methodologies for the design of low power CMOS phase frequency detector for high speed applications like PLL. The phase frequency detector (PFD), which helps PLLs achieve simultaneous phase and frequency error detection, is an indispensable functional block and plays an important role in improving the performance of the whole PLL system. This paper also discusses two major problems in PFD, namely, the dead zone problem and the missing edge problem. The proposed design will be the CMOS phase frequency detector for high speed applications with low power dissipation. The PFD will be implemented using 0.18 µm technology. The designed phase frequency detector can be used in PLL with frequency up to 1 GHz.

Index Terms- Phase/Frequency Detectors, PFD, Phase-Locked Loops, PLL, CMOS Integrated Circuits

I. INTRODUCTION

The phase-locked loop (PLL) plays the role of generating a clock signal that is usually a multiple of a reference clock and synchronized with the reference clock in phase. The PLL is widely used in many applications such as frequency synthesis, phase modulation, phase/frequency demodulation, and clock data recovery. In most cases, the charge pump PLL (CP-PLL) is used due to its high frequency range and simple structure. In the PLL, the phase frequency detector (PFD) compares the rising edges of the reference clock and the voltage-controlled oscillator (VCO) clock, and generates a lead signal when the reference phase is leading or a lag signal when the reference phase is lagging. The phase difference detected in the PFD passes through the loop filer to control the VCO. As the phase difference critically affects the overall characteristics of the PLL such as lock-in time and jitter performance, the PFD should be designed to work accurately for any phase difference. However, the PFD suffers from two problems. The first one called the dead-zone problem occurs when the rising edges of the two clocks to be compared are very close. Due to lots of reasons such as circuit mismatch and delay mismatch, the PFD has a difficulty in detecting such a small difference. There have been many PFD structures proposed to cope with this problem. Among them, the three state PFD is widely employed because it is simple, easy to implement, and, more importantly, almost immune to the dead-zone problem. Secondly, some of the rising edges can be missed in the detection when the edges are overlapped with the reset signal internally generated in the PFD, which is called the missing edge problem. Missing edges induce wrong polarity in the PFD output, leading to incorrect behavior and making the PLL spend more time to acquire phase or frequency There have been several research works dealing with the missing edge problem, but most of the previous works require complex circuits or are dedicated to limited cases. As circuit speed increases, the possibility of missing edges increases. Therefore, the missing edge problem becomes a critical factor that determines the acquisition time.

A circuit that detects the phase and frequency differences is required to increase the acquisition range and lock speed of PLL. The output of the circuit consists of two non – complementary signals Qa and Qb. If the frequency at the input A is greater than that of input B the circuit produces output Qa =1 and Qb = 0. Similarly if frequency at the input A is less than that of input B the circuit produces output Qa = 0 and Qb = 1. While if the frequency at both the inputs A and B is equal than the circuit produces the output either at Qa or Qb with the pulse duration equal to phase difference between the two inputs. Thus the average value at the output is the phase differences between the two inputs. The state diagram for the operation of the circuit is shown in figure 1. The output of the circuit mainly depends upon the duty of the input signals; hence the circuit has to be implemented using edge triggered sequential circuits. The operation of the sequential circuit using edge triggered flip flops further depends upon on the rising and falling time of the signals.

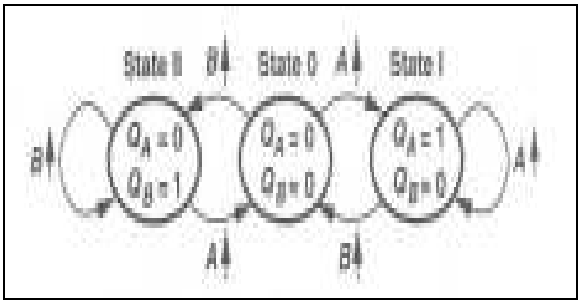

Figure 1: State Diagram

II. CONVENTIONAL PFD

An ideal phase detector produces an output signal whose dc value is linearly proportional to the differences between the phases of two periodic inputs.

$$v_{out} = k_{pd} \Delta \phi \qquad \text{--- 1}$$

Where K_{pd} is the gain of the phase detector and ΔØ is the phase difference between the input signals. PFD generates an output pulse whose width is equal to the time difference between consecutive zero crossings of the input signals.

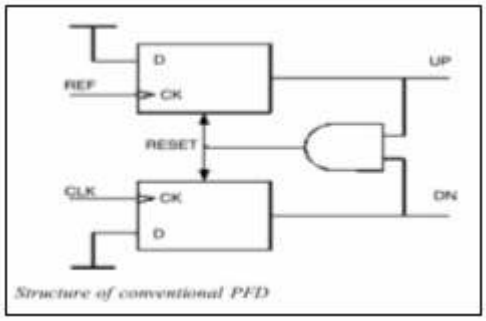

Figure 2: Conventional PFD

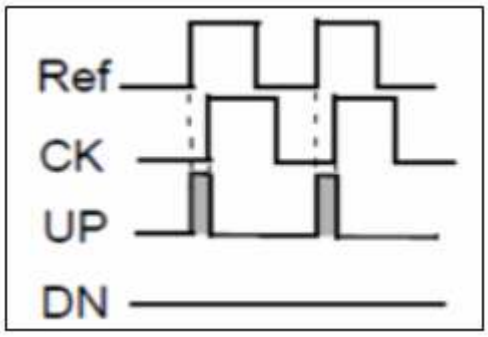

Figure 3: REF leading CK

The circuit consists of two reset table, edge triggered D flip flops with their D inputs tied to logic 1. The Ref and Clk serve as clocks of the flip flops. Suppose the rising edge of REF leads that of CLK, then UP goes to logic high. UP keeps high until the rising edge of CLK makes DN on high level. Because UP and DN, are ANDed, so RESET goes to logic high and resets the PFD into the initial state.

III. CMOS PFD REVIEW

A clock and data recovery circuit with a two exclusive-OR phase frequency detector is presented [1].This PFD generates the control signal for the voltage-controlled oscillator (VCO) in the phase locked loop by comparing different phase clocks and input data. Circuit operates an input at data rate of 800 Mbps to 1.2 Gbps under 2.5V using 0.25 µm CMOS technology.

Fast frequency acquisition phase frequency detector has only 16 transistors [2]. This PFD has linear range when the phase difference is in [0, Π], and saturates when the phase difference is in [Π, 2Π]. It completely eliminates the blind zone, speeds up the acquisition process and improves the maximum operating frequency of the PFD. The circuit topology is very simple. Results show that the circuit can operate up to 800 Meg in 0.5 µm with 5 V supply.

Falling edge phase frequency detector [3] using 12 transistors and consumes 6.6 µW power is presented in this paper. It has no dead zone operates at 2.5 GHz. The circuit can be used in high speed and low power applications. The circuit was implemented in 0.18um technology.

A high-speed CMOS Phase/Frequency Detector (PFD) for faster frequency acquisition is presented [4]. An improved CMOS D-type master-slave flip-flop is described and adopted. Higher speed is attributed to the reduced node capacitances. Charge-sharing phenomena are circumvented. An input delay scheme is employed to achieve faster acquisition.

A new phase frequency detector (PFD) is presented to enable fast frequency acquisition in the phase-locked loop (PLL). To cope with the missing edge problem, the proposed PFD [5] predicts the reset signal and blocks the corresponding input signal during the reset time. The blocked edge is regenerated after the reset signal is deactivated. The PFD works correctly for the entire phase difference and achieves 42.1% speed-up in the acquisition time when it is applied to the conventional charge pump PLL implemented in a 0.18µm CMOS technology.

IV. COMPARATIVE STUDY

Parameters	**[1]**	**[2]**	**[3]**	**[4]**	**[5]**
Technology	0.25 µm	0.5 µm	0.18 um	0.18 µm	0.18 µm
Operating Frequency	800 Mbps to 1.2 Gbps	800 Mbps	2.5 GHz	1.2 to 1.8 GHz	2.3 GHz
Power dissipation	-	300mW	6.6uW	-	1.56 mW
VDD	2.5V	5V	1.8V	-	1.8V

V. PROPOSED METHODOLOGY

The proposed design will be the CMOS phase frequency detector for high speed applications with low power dissipation. The PFD will be implemented using 0.18 µm technology. The designed phase frequency detector can be used in PLL with frequency up to 1 GHz.

REFERENCES

[1] D. H. Kim, et al, "Clock and data recovery circuit with two exclusive OR phase frequency detector", in IEEE Electronics Letters, vol. 36, no. 16, Aug. 2000, pp 1347 – 1349.
[2] W. Hu, et al, "Fast frequency acquisition phase frequency detector with zero blind zone in PLL", in IEEE Electronics Letters, vol. 43, no. 19, Sep. 2007.
[3] N. M. H. Ismail, et al, "CMOS phase frequency detector for high speed application", in 4th International Design and Test Workshop, Nov 2009.
[4] R. Y. Chen, et al, "A high speed fast acquisition CMOS phase frequency detector for MB-OFDM UWB", in IEEE Transaction on Consumer Electronics, vol. 53, no. 1, Feb. 2007, pp 23 - 26.
[5] K. Park, et al, "Fast frequency acquisition phase frequency detector with prediction based edge blocking", in IEEE International Symposium on Circuits and Systems, 2009, pp 1891 - 1894
[6] B. Razavi, "Design of Analog CMOS Integrated Circuits" , Prentice Hall, 1998.

First Author – Vaijayanti Lule, B.D.C.O.E,Sevagram,Wardha, Address- Opposite Indira Market, Wardha-442001,(MH)India, Mobile no.-9271633936, vaiju_lule@yahoo.co.in

Second Author – Prof (Ms).Vrushali G Nasre, Assistant Prof. P. G. Department of Engineering, B.D.C.O.E. Sevagram, Wardha, Address- Ram Nagar, Wardha – 442001, (MH), India, Mobile no.- 9373201856, vrushnasre@gmail.com.