

Folded Cascode OTA Using Self Cascode Technique

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Abstract- Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Many low voltage design techniques have been developed to meet the needs of present era of low power portable electronic equipment, which drove the analog designers to look for innovative design techniques like self cascode MOSFETs [1-5]. In this paper, we have investigated the merits and demerits of self cascode approach. For this aim in mind we designed a Folded Cascode using self cascode technique and analyzed its various properties through the Spice simulations for 0.13 micron CMOS technology from TSMC and the supply voltage 1.8V.

Index Terms- folded cascode OTA, self cascode, gain, low power.

I. INTRODUCTION

In 2004, Comer [6,7] discussed the effects on the overall composite cascode circuit performance with one device operating in the sub threshold and the other device operating in the active region and suggested that this approach may result in a very high gain stage for use in op-amps, along with low power dissipation too [8,9]. To have high output impedance and thereby high gains, cascoding is done, where two MOSFETs are placed one above the other [10, 11–13]. The regular cascode structures are avoided as their use increases the gain of the structure. Self-cascode is the new technique, which does not require high compliance voltages at output nodes. It provides high output impedance to give high output gain and so it is useful in low-voltage design. Folded cascode OTA is used for high speed applications thanks to its capability to provide high gain and large bandwidth [14]. A self-cascode is a 2-transistor structure as shown in figure1 [1], which can be treated as a single composite transistor. The composite structure has much larger effective channel length and the effective output conductance is much low. The lower transistor M1 is equivalent to a resistor, whose value is input dependent. For optimal operation, the W/L ratio of upper transistor M1 is kept larger than that of lower transistor M2, i.e., $m \gg 1$. For the composite transistor to be in saturation region M2 have to be in saturation and M1 in linear region.

II. SELF CASCODE TECHNIQUE

The effective g_m for the composite transistor is approximated as

$$g_m(\text{effective}) = \left(\frac{\sum g_m}{m} \right) = g_{m1} \quad (1)$$

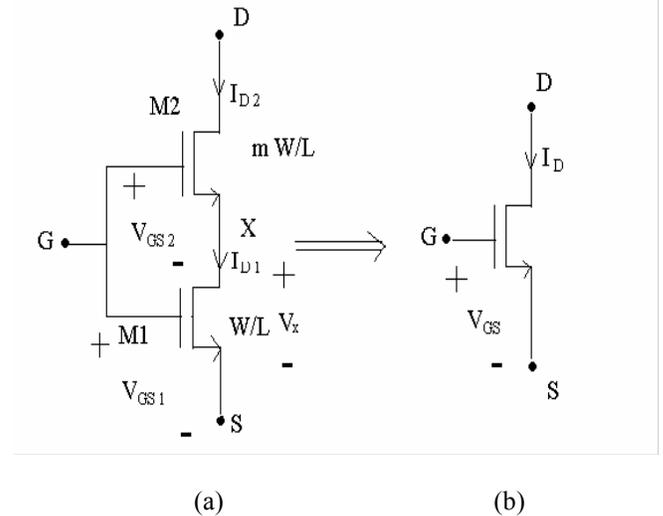


Figure 1 (a) Self Cascode NMOS transistor. (Left)
(b) Equivalent NMOS transistor. (Right)

For the composite transistor to be in saturation region M2 have to be in saturation and M1 in linear region. For these transistors, the currents I_{D1} and I_{D2} are given as

$$I_{D1} = \beta_1 (V_{in} - V_{TN} - (V_X/2)) V_X \quad (\text{Ohmic}) \quad (2)$$

$$I_{D2} = (\beta_2/2) (V_{in} - V_X - V_{TN})^2 \quad (\text{Saturation}) \quad (3)$$

and from this we get

$$I_{D2} = \left[\frac{(\beta_2 \beta_1)}{2(\beta_2 + \beta_1)} \right] [V_{in} - V_{TN}]^2 \quad (4)$$

$$\beta_{\text{effective}} = (\beta_2 \beta_1) / (\beta_2 + \beta_1) \quad (5)$$

for

$$\beta_2 = m \beta_1 \quad (6)$$

$$\beta_{\text{effective}} = [m/(m+1)] \beta_1 = [1/(m+1)] \beta_2 \quad (7)$$

and for $m \gg 1$,

$$\beta_{\text{effective}} \approx \beta_1 \quad (8)$$

where $\beta = \mu C_{ox}(W/L)$ and is called the trans-conductance parameter.

M1 operates in linear region, while M2 operates in saturation or linear region. Hence voltage between source and drain of M1 is small. There is no appreciable difference between the V_{Dsat} of composite and simple transistors and a self-cascode can be used in low voltage operation.

For a self-cascode

$$V_{Dsat} = V_{Dsat-M2} + V_{DS-M1} \quad (9)$$

The operating voltage of regular cascode is much higher than that of self-cascode and hence a self-cascode structure can be used in the low voltage design. The advantage offered by self-cascode structure is that it offers high output impedance similar to a regular cascode structure while output voltage requirements are similar to that of a single transistor.

III. PROPOSED FOLDED CASCODE OTA

The Proposed Folded Cascode OTA is shown in figure2. At input terminals self cascode is not used but on rest of the circuits self cascode is used because this whole circuit works as load. In this proposed circuit we take the value of $m=2$. In this circuit each transistor splits into two so that upper transistors are working in saturation region while other is in linear region to work this circuit properly. The simulation results are shown in Table I. The amplifier device sizes are shown in Table II.

IV. SIMULATION RESULTS FOR SELF CASCODE FOLDED CASCODE OTA

The simulations are done with 1.8V power supply. The simulations are done with the help of Tanner EDA tool T-SPICE and waveforms are analyzed on W-Edit. All designs are done using 130nm TSMC MOSIS Level-3 model file.

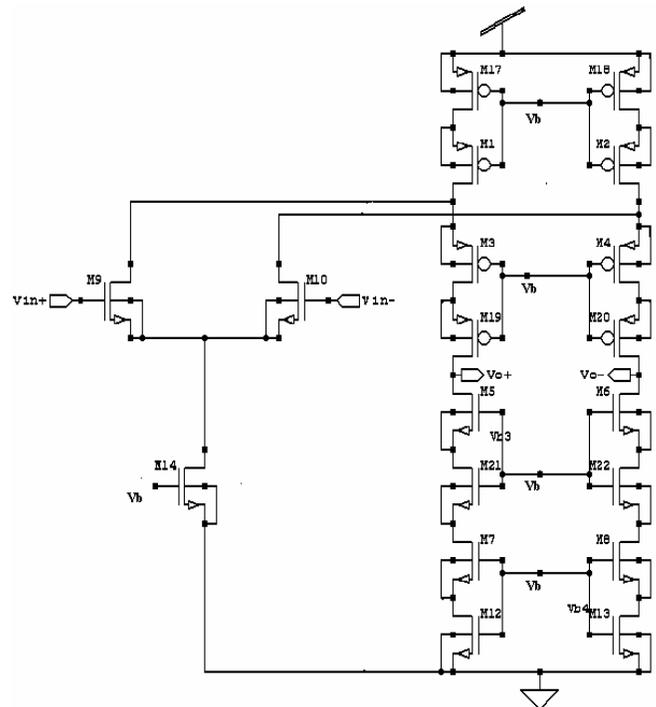


Figure 2: Proposed Folded Cascode OTA

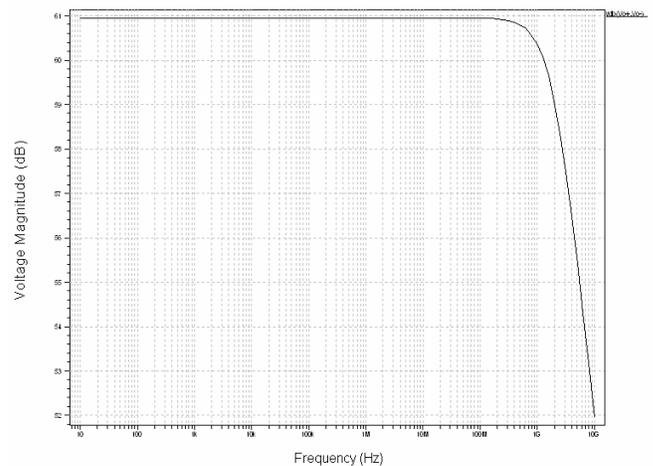


Figure 3: Voltage Gain of Proposed Folded Cascode OTA

V. CONCLUSION

In this paper, we have presented techniques which promise low voltage design with high gain. By using self cascode technique the gain of proposed folded cascode is increased about 19db as shown in figure3 with decrease in power consumption. The regular cascode structures are avoided as their use increases the gain of the structure, but decreases the output signal swing. Self-cascode is the new technique, which does not require high compliance voltages at output nodes. It provides high output impedance to give high output gain and so it is useful in low-voltage design. By increasing the value of m , we can further increase the gain of the folded cascode OTA with low power

consumption. But the condition of self cascode should be maintained. The effect of temperature is comparatively less in comparison to the conventional folded cascode OTA as shown in figure4. Noise effect is also less in proposed Folded Cascode OTA. This folded cascode circuit have been employed in a variety of situations -from increasing the gain in amplifiers with medium available bandwidth. The channel lengths and widths of the two transistors can be optimized for the largest increase in the output resistance.

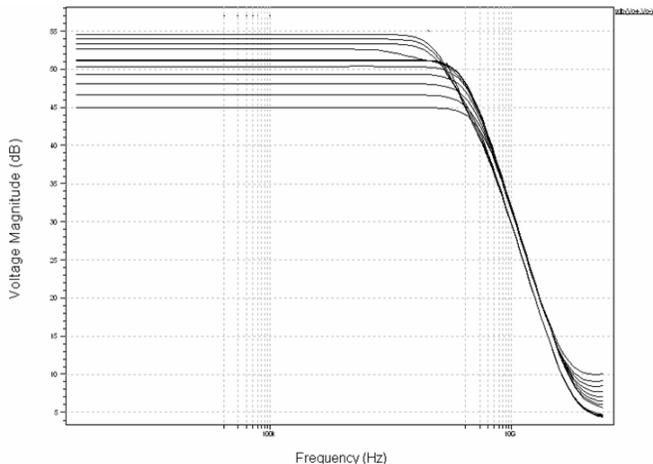


Figure 4: Effect of Temperature on Proposed Circuit.

Table I: Simulated Results of Proposed Folded Cascode OTA

Characteristics	Simulated results
Power Supply	1.8V
Power consumption	1.038075e-002 W
Open loop gain	60.96 dB
Temperature Effect	Less

Table II W/L for various transistors (μm)

DEVICE	Type	Proposed FCA
M1/M2	PMOS	105.6/0.5
M3/M4	PMOS	105.6/0.5
M5/M6	NMOS	28/0.5
M7/M8	NMOS	20.8/0.5
M9/M10	NMOS	10/0.18
M12/M13	NMOS	10.4/0.5
M14	NMOS	19.8/0.5
M17/M18	PMOS	211.2/0.5
M19/M20	PMOS	52.8/0.5

M21/M22	NMOS	14/0.5
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They can extensively be used where power supply requirements are not the constraint and that high gain is of utmost importance.

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