Implementation and Analysis of Power, Area and Delay of Array, Urdhva, Nikhilam Vedic Multipliers

Ch. Harish Kumar

International Institute of Information Technology, Pune , India

Abstract- The performance of the any processor will depend upon its power and delay. The power and delay should be less in order to get a effective processor. In processors the most commonly used architecture is multiplier. If the power and delay of the multiplier is reduced then the effective processor can be generated. The architectures for multipliers are mainly Array and Vedic multipliers. In Vedic multipliers there are two types of techniques for multiplications based on Urdhva Triyagbhyam and Nikhilam sutras. In this paper the comparison of these architectures is carried out to know the best architecture for multiplication w.r.t power and delay characteristics. The design of architectures are done in Verilog language and the tool used for simulation is Xilinx 10.1 ISE.

Index Terms- Vedic multiplier; Array multiplier; Urdhva Triyagbhyam; Nikhilam;

I. INTRODUCTION

The ancient system of Vedic Mathematics was re-introduced to the world by Swami Bharati Krishna Tirthaji Maharaj, Shan-karacharya of Goverdhan Peath. "Vedic Mathematics" was the name given by him. Bharati Krishna, who was himself a scholar of Sanskrit, Mathematics, History and Philosophy, was able to reconstruct the mathematics of the Vedas. According to his re-search all of mathematics is based on sixteen Sutras, or word-formulae and thirteen sub-sutras [10,5]. Vedic mathematics reduces the complexity in calculations that exist in conventional mathematics. Generally there are sixteen sutras available in Vedic mathematics. Among them only two sutras are applicable for multiplication operation. They are Urdhva Triyakbhyam sutra (literally means vertically and cross wise) and Nikhilam Sutra (literally means All from 9 and last from 10). The logic behind Urdhva Triyakbhyam sutra is very much similar to the ordinary array multiplier [7].

The power of Vedic mathematics is not only confined to its simplicity, regularity, but also it is logical. Its high degree of eminence is attributed to the aforementioned facts. It is these phenomenal characteristics, which made Vedic mathematics, become so popular and thus it has become one of the leading topics of research not only in India but abroad as well. Vedic mathematics' logics and steps can be directly applied to problems involving trigonometric functions, plane and sphere geometry, conics, differential calculus, integral calculus and applied mathematics of various kind.

The advantage of Vedic mathematics lies in the fact that it simplifies the complicated looking calculations in conventional mathematics to a simple one in a much faster and efficient manner. This is attributed to the fact that the Vedic formulae are claimed to be based on the "natural principles on which the human mind works". Hence this presents some effective algorithms which can be applied to various branches of engineering [11].

Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application [6].

In this paper the two sutra's which are used for the multiplication i.e Urdhva Triyakbhyam and Nikhilam Sutra are compared. The architecture of basic 2X2 multiplier, 8X8 multiplier for Urdhva Triyakbhyam and Nikhilam Sutra are discussed. The results are compared for 8X8, 16X16 and 32X32 multipliers. Array multiplier is also taken which is to compare the results between Vedic and conventional multipliers. The results are compared in terms of power, delay and area.

Vedic multipliers are to be the best compared to conventional ones as we know that from the earlier. Compared to Nikhilam Sutra architecture Urdhva Triyakbhyam is efficient one.

II. ARRAY MULTIPLIER

Array multiplier is an efficient layout of a combinational multiplier. In array multiplier, consider two binary numbers A and B, of m and n bits. There are mn summands that are produced in parallel by a set of mn AND gates. n x n multiplier requires n (n-2) full adders, n half-adders and n2 AND gates. Also, in array multiplier worst case delay would be (2n+1) td. Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical .Thus, it is a fast multiplier but hardware complexity is high[2] .

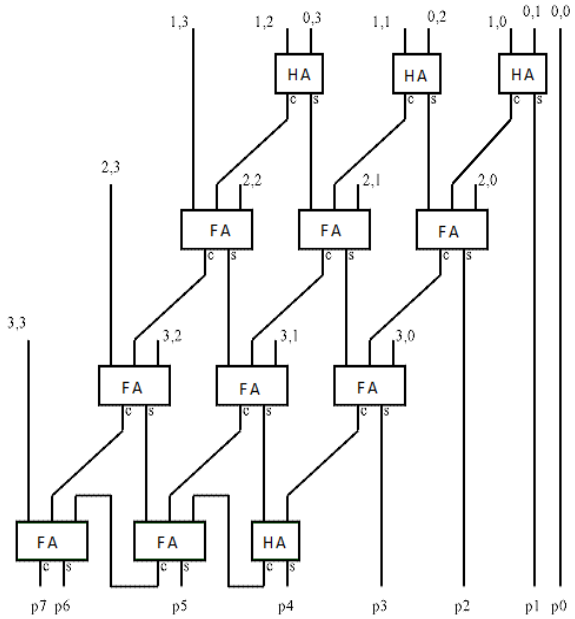

Figure 1. Array Multiplier

III. VEDIC MULTIPLICATION

A. General 2X2 Vedic Multiplier[3] :

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Figure 2. Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit of the final product.

$s0 = a0b0$; (1)
$c1s1 = a1b0 + a0b1$; (2)
$c2s2 = c1 + a1b1$; (3)

The final result will be *c*2*s*2*s*1*s*0. This multiplication method is applicable for all the cases. The 2x2 bit Vedic multiplier (VM) module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Figure 3.

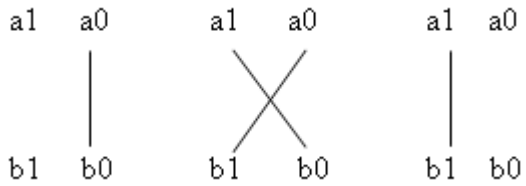

Figure 2: The Vedic Multiplication Method for two 2-bit binary numbers

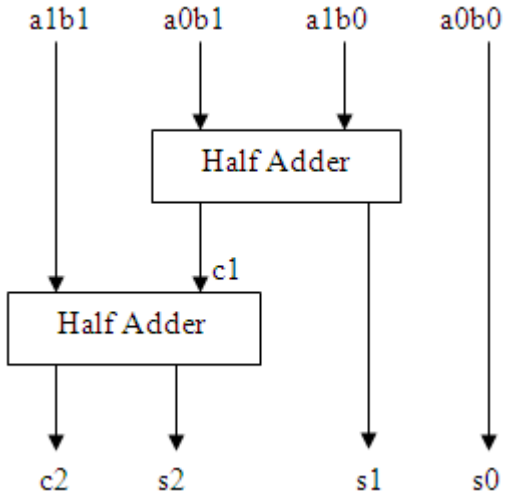

Figure 3: Block Diagram of 2x2 bit Vedic Multiplier (VM)

The same method can be extended for higher no. of input bits (say 4). But a little modification is required as discussed in section 3.2. This section illustrates the implementation of 4x4 bit VM which uses 2x2 bit VM as a basic module.

Divide the no. of bits in the inputs equally in two parts. Let's analyze 4x4 bit multiplication, say multiplicand A=A3A2A1A0 and multiplier B= B3B2B1B0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let's divide A and B into two parts, say "A3 A2" & "A1 A0" for A and "B3 B2" & "B1B0" for B. Using the fundamental of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block.

B. Urdhva Tiryakbhyam Sutra:

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done and then, concurrent addition of these partial products can be done. Thus parallelism in generation of partial products and their summation is obtained using Urdhava Tiryakbhyam. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. While a higher clock frequency generally results in increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It will enhance the ALU unit also. As a result the mathematical operation which

employs multiplication is demonstrated that this architecture is quite efficient in terms of silicon area/speed.

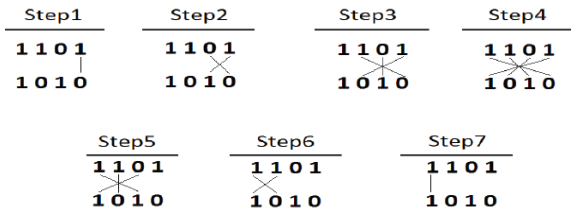

Figure 4: Using Urdhava Tiryakbhyam for binary numbers

4X4 Multiply Block:

The 4X4 Multiplier is made by using four 2X2 multiplier blocks. The multiplicands are of bit size n=4 where as the result is of 8 bit size. The input is broken into smaller chunks of size n/2= 2, for both inputs, that is a and b. These newly formed chunks of 2 bits are given to 2X2 multiplier block to get the 4 bit result. The same method is followed for the multipliers of higher bits like 8,16 and 32 bits.

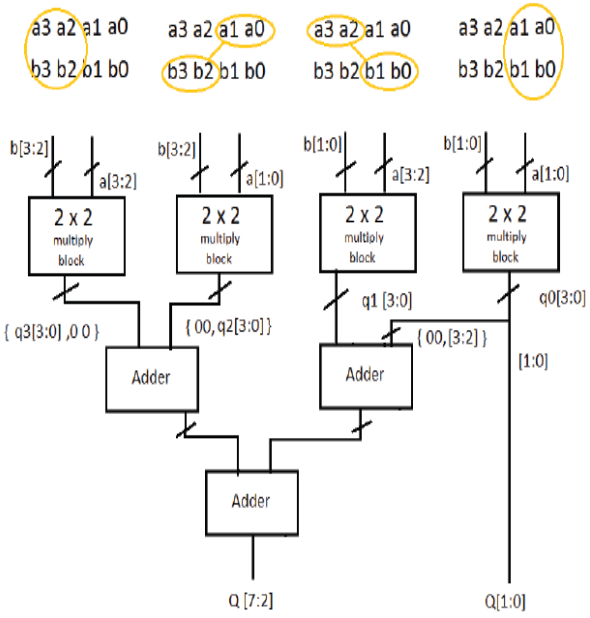

Figure 5: 4X4 Multiply Block

The equations of the 4X4 Vedic multiplier are

X = a3 a2 a1 a0

Y = b3 b2 b1 b0

P0 = a0.b0

P1 = a1.b0 + a0.b1

P2 = a2.b0 + a1.b1 + a0b2 + P1(1)

P3 = a3.b0 + a2.b1 + a1.b2 + a0.b3 + P2(2 to 1)

P4 = a3.b1 + a2.b2 + a1.b3 + P3(2 to 1)

P5 = a3.b2 + a2.b3 + P4(2 to 1)

P6 = a3.b3 + P5(2 to 1)

Product =P6 & P5(0) & P4(0) & P(3) & P(2) & P(1) & P(0)

& - Concatenate

C. Nikhilam Sutra :

The example of nikhilam multiplication is shown in the below figure6. Here the nearest base is chosen first. The multiplicand and the multiplier will be subtracted from the nearest base, which is equivalent to taking two's complement. Then the product of the two's complement and the common difference will give the final result [2].

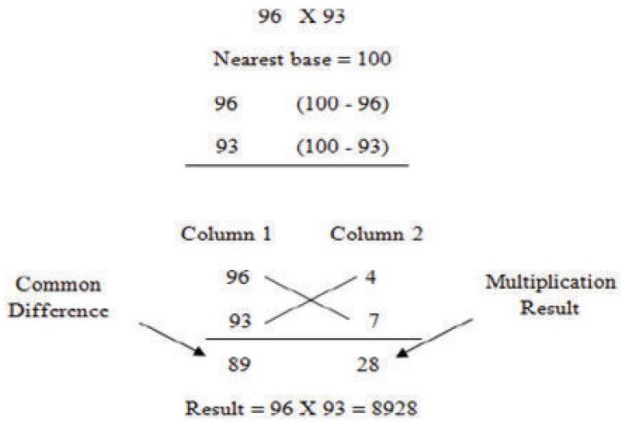

Figure 6: Multiplication using Nikhilam

The nikhilam multiplier architecture is shown in the below figure7. Here the two inputs are first complimented and those complimented results are multiplied. Here the multiplier used also plays an important role in calculating delay. We can use either vedic multiplier or array multiplier. Then the multiplier output is added to the two inputs a and b. The right hand side result of the multiplier is the R.H.S of the original product and the L.H.S result of the adder is the L.H.S of the original product.

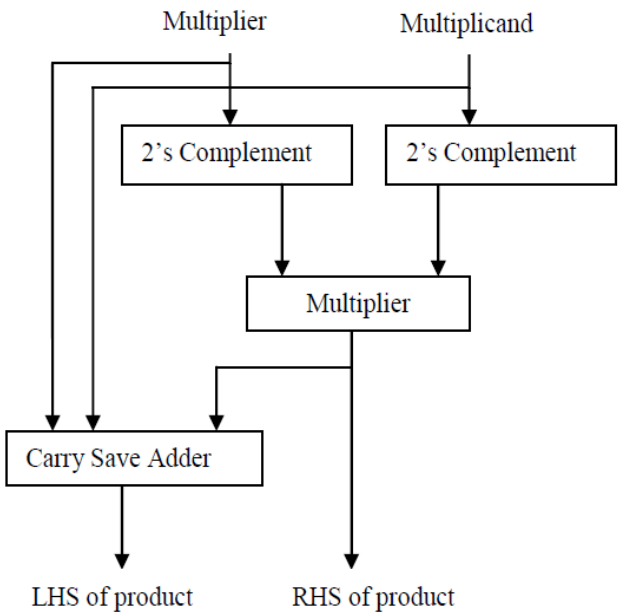

Figure 7: Nikhilam Multiplier's Architecture

IV. RESULTS

The waveforms of the multipliers of 8, 16 and 32 bits are shown in the figures 8,9,10 respectively at the bottom of the paper.

The tabular form which compares the results of power, delay and area of the array multiplier, urdhava tiryakbhyam multiplier and nikhilam multiplier are shown in the below tabular form.

Type of Unit (8-Bit)	Power (mW)	Delay (nS)	Memory (kb)
Array Multiplier	168	26.825	162752
Urdhava Tiryakbhyam	99	23.079	162752
Nikhilam	148	27.878	165824

Table 1: Results of 8-bit multiplier

Type of Unit (16-Bit)	Power (mW)	Delay (nS)	Memory (kb)
Array Multiplier	250	53.276	175168
Urdhava Tiryakbhyam	118	41.350	178752
Nikhilam	118	51.323	198528

Table 2: Results of 16-bit multiplier

Type of Unit (32-Bit)	Power (mW)	Delay (nS)	Memory (kb)
Array Multiplier	382	107.128	263232
Urdhava Tiryakbhyam	315	72.332	233344
Nikhilam	315	90.747	251776

Table 3: Results of 32-bit multiplier

V. CONCLUSION

Hence Urdhava Tiryakbhyam multiplier is the best multiplier compared to array and nikhilam's multiplier when compared to delay and power calculations.

ACKNOWLEDGMENT

I would like to acknowledge my mentor G. Vengal Rao Sir and Soma Bhanu Tej who supported me during the period in calculating my results and verifying codes.

REFERENCES

[1] M.B. Damle, Dr. S. S. Limaye, " Low-power Full Adder array-based Multiplier with Domino Logic," IOSR Journal of Electronics and Communication Engineering (IOSRJECE), ISSN : 2278-2834 Volume 1, Issue 1 (May-June 2012), PP 18-22.

[2] Sumit R. Vaidya, D. R. Dandekar, "Performance Comparison of Multipliers for Power-Speed Trade-off in VLSI Design," RECENT ADVANCES in NETWORKING, VLSI and SIGNAL PROCESSING, ISSN: 1790-5117, ISBN: 978-960-474-162-5.

[3] Pushpalata Verma, K. K. Mehta, " Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool," International Journal of Engineering and Advanced Technology (IJEAT), ISSN: 2249 – 8958, Volume-1, Issue-5, June 2012.

[4] Manoranjan Pradhan, Rutuparna Panda, Sushanta Kumar Sahu, "Speed Comparison of 16x16 Vedic Multipliers," International Journal of Computer Applications (0975 – 8887),Volume 21– No.6, May 2011.

[5] G.Ganesh Kumar, V.Charishma, " Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques", International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012 1 ISSN 2250-3153.

[6] Soma BhanuTej, "Vedic Algorithms to develop green chips for future", Volume 2, Issue ICAEM12, February 2012, ISSN Online: 2277-2677 ,ICAEM12,Jan20,2012,Hyderabad,India.

[7] Sree Nivas A, Kayalvizhi N, " Implementation of Power Efficient Vedic Multiplier", International Journal of Computer Applications (0975 – 8887) Volume 43– No.16, April 2012.

[8] Sumit Vaidya, Deepak Dandekar, "DELAY-POWER PERFORMANCE COMPARISON OF MULTIPLIERS IN VLSI CIRCUIT DESIGN", International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, July 2010.

[9] Pushpalata Verma, " Design of 4x4 bit Vedic Multiplier using EDA Tool", International Journal of Computer Applications (0975 – 888) Volume 48– No.20, June 2012.

[10] Krishnaveni D., Umarani T.G., " VLSI IMPLEMENTATION OF VEDIC MULTIP-LIER WITH REDUCED DELAY", International Journal of Advanced Technology & Engineering Research (IJATER) National Conference on Emerging Trends in Technology (NCET-Tech), ISSN No: 2250-3536 Volume 2, Issue 4, July 2012.

[11] Ramachandran.S, Kirti.S.Pande, " Design, Implementation and Performance Analysis of an Integrated Vedic Multiplier Architecture", International Journal Of Computational Engineering Research / ISSN: 2250–3005.

[12] V.Vamshi Krishna, S. Naveen Kumar, "High Speed, Power and Area efficient Algorithms for ALU using Vedic Mathematics", International Journal of Scientific and Research Publications, Volume 2, Issue 7, July 2012 ,ISSN 2250-3153.

[13] P. Saha, A. Banerjee, A. Dandapat, P. Bhattacharyya, " Vedic Mathematics Based 32-Bit Multiplier Design for High Speed Low Power Processors", INTERNATIONAL JOURNAL ON SMART SENSING AND INTELLIGENT SYSTEMS VOL. 4, NO. 2, JUNE 2011.

AUTHORS

First Author – Ch. Harish Kumar, M.Tech-VLSI, International Institute of Information Technology, Pune , India, e-mail: harish.chhk@gmail.com

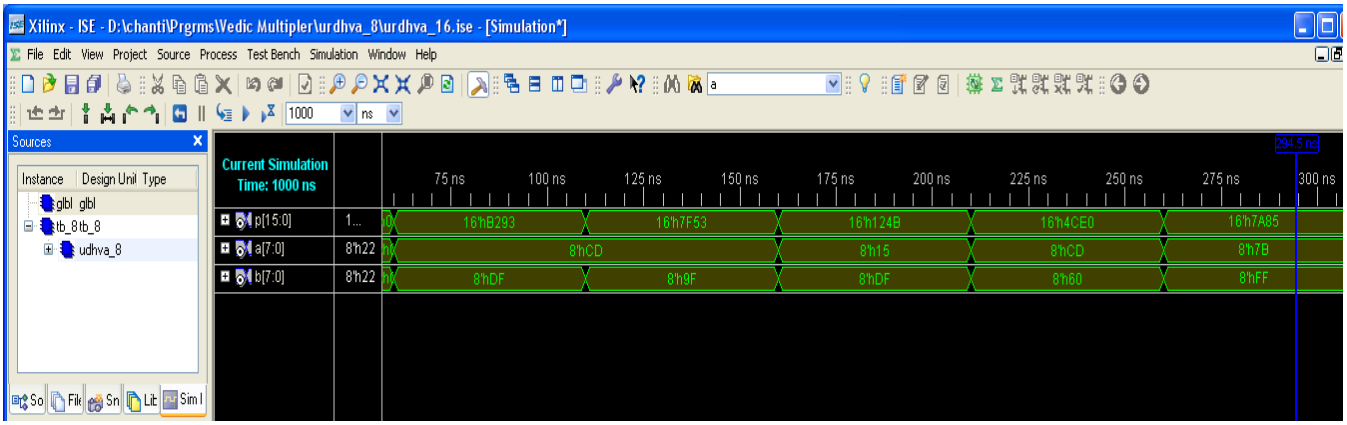

Figure 8: Waveform of 8-bit multiplier

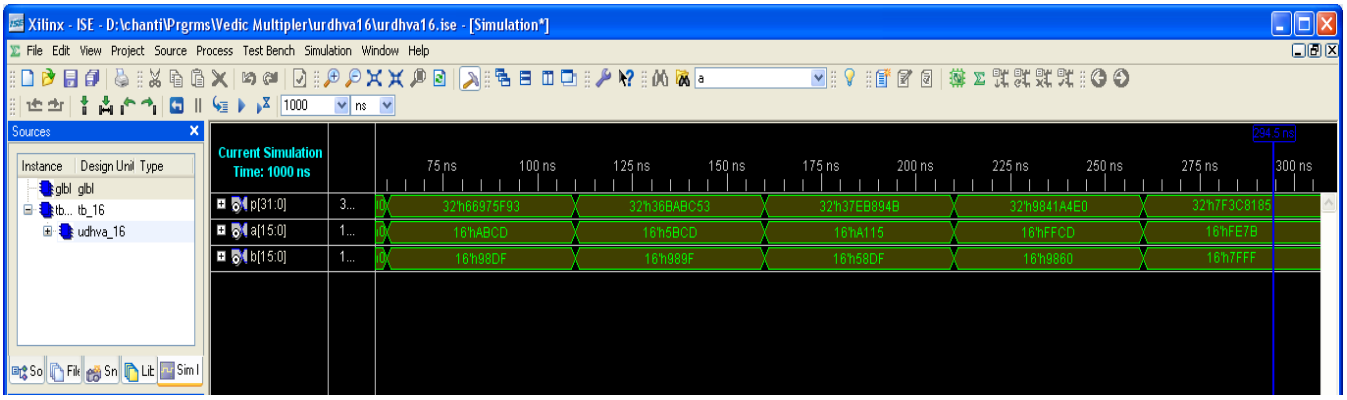

Figure 9: Waveform of 16-bit multiplier

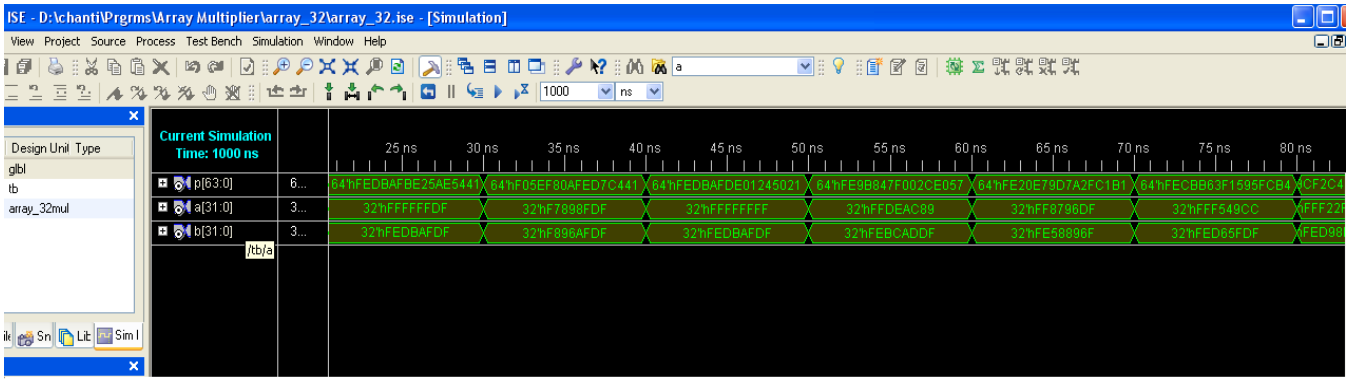

Figure 10: Waveform of 32-bit multiplier