Design and Implementation of A 24-Hour, Minutes and Seconds Display Digital Clock

Auwal Mustapha Imam

Department of Physics with Electronics, Federal University, Birnin Kebbi

Abstract- This paper presents the design of a Digital Clock that displays 24-hours, minutes and seconds. A time-based oscillator containing a 555 timer Integrated Circuit (IC) in an astable mode with a frequency of 1Hz provides the clock pulses for the seconds display. On each of the Dual Seven-Segment (7-Segment) displays for hours, minutes and seconds, Binary Coded Decimal (BCD) counters converts each clock pulse received into a 4 bit 8421 synchronous logic output. Display decoders/drivers connected to each 7-Segment display decodes the 4-bit 8421 logic and converts it to a 7-Segment display codes. The dual-7-Segment displays of each of the hours, minutes and seconds output the figures 0 to 9 according to the set time. The clock is designed to work with the stabilized 9V DC voltage power supply.

Index Terms- Astable, Binary, Clock, Digital, Display, Integrated-Circuit, Logic, Output, Pulse, Timer, 7-Segment.

I. INTRODUCTION

Changes in time keeping technology have influenced the character of scientific observation, aided the development of other machine technologies and brought significant revisions in the way people think about and behave in time. Electronic clocks have predominantly replaced the mechanical clocks. They are much reliable, accurate, maintenance free and portable [1].

Despite that the cost of producing digital clocks is higher than that of analog clocks; digital clocks are more common and independent of external source. Analog clocks in most cases uses scale and a pointer, due to this, it is susceptible to parallax and human errors while taking readings which make it less accurate. Digital clocks eliminate parallax error and reduce human error, thereby giving a high level of accuracy in the readings. The Light Emitting Diodes (LEDs) in the 7-Segment displays encourages the use of digital clocks even in the dark which analog clocks do not have.

This digital clock makes use of a 555 timer IC wired in an astable mode and designed to give output pulse of 1Hz i.e. one second for one complete cycle. The pulse signal otherwise known as clock is fed into a BCD counter which gives a synchronous 8421 (4 bit) output *see figure 1* which 1 is the least significant bit LSB. This synchronous output if fed into a BCD-to- Seven Segment Decoder/Driver which will drive the seven segment display. The BCD counters are cascaded and various processes are undergone. The use of BCDs allows two BCD digits to be stored within a single byte (8-bits) of data [2], allowing a single data byte to hold a BCD number in the range of 00 to 99. A 4-bit BCD input (0011) representing the number 3 is shown in figure 1.

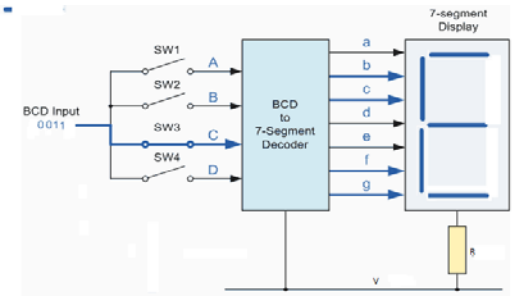

Figure 1: 4-Bit BCD input epresenting the number 3

The 1s and 0s otherwise known as logic levels or logic states HIGH and LOW respectively. With this bits, it is easier for computer to process data and gives out the required output because it is only dealing with 1 and 0 values [3]. This makes it possible to design a digital clock that will display time in the form of figures instead of scale and pointer as to the case of an analog clock.

II. DESIGN METHODS AND PROCEDURES

An astable circuit produces a 'square wave'; this is a digital waveform with sharp transitions between low (0V) and high (+Vs) [4][5]. The durations of the low and high states may be different, but in this digital clock the high state duration and the low state duration are the same. That is what makes the circuit an astable; the output is continually changing between 'low' and 'high'.

The timing period is therefore calculated as;

$$T = 0.7 \times (R1 + 2R2) \times C1 \quad (1)$$

And the frequency is calculated as;

$$F = \frac{1}{(R1 + 2R2) \times C1} \quad \frac{1.4}{f} \quad (2)$$

In the 555 time based oscillator;
T = time period in seconds (s)
f = frequency in hertz (Hz)
R1 = resistance in ohms =6.8KΩ
R2 = resistance in ohms =68KΩ
C1 = capacitance in farads (F) =10μF

Thus;

$$F = \frac{1.4}{(6800 + 2(68000))\ 10\ X\ 0.000001}.$$

F= 1Hz

The 1Hz astable clock pulse provided by the 555 timer oscillator is fed into each BCD counter of the seconds' stage. The BCD counter provides a 4 bit 8421 synchronous logic output for every clock pulse received as shown in table 1.

Table 1: 8421 synchronous logic output for numbers 0 - 9.

	8	*4*	*2*	*1*	
pulses	*output D*	*output C*	*output B*	*output A*	*Display output*
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9

The unit of the seconds is enabled via pin 5 of the BCD counter and it begins to count from 0 – 9.

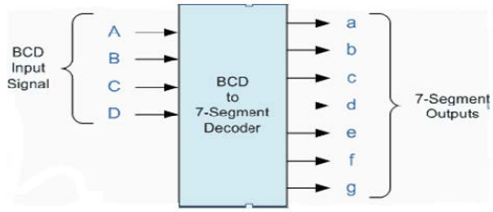

Figure 2: BCD to 7-Segment decoder

The BCD output is then fed into the decoder (as in figure 2) and the display which outputs the figures as shown in table 2.

Table 2: output of the BCD to 7-Segment driver.

Pulse	BCD	A	B	C	D	E	F	G
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	0	0	1	1

As soon as it counts 9, it resets itself on the count of 10 and in turn enables the BCD counter of the Tens stage via pin 7 (carry out) and pin 5 (enable) of the BCD counter of the Units and Tens display. This makes the clock to display 00 – 99. The counter is then shortened by the use of AND gate which resets the counter at the count of 00 – 59. When the BCD counter resets, it gives a clock pulse to the Unit of the minutes display. The minutes counts from 00 – 59 and gives a clock pulse to the Unit of the hours. The hours count from 00 to 23 and then reset itself on the count of 24.

III. CIRCUIT DIAGRAM AND PRINCIPLE OF OPERATION

Whenever we are designing any electronic system, the area, speed, power consumption and cost are the main parameters [6]. Thus, we start with the consideration of the power consumption of the clock. The clock is designed to work with the regulated power supply. It contains a transformer which steps down the voltage from 220V to 12V. It also contains a rectifier which converts the AC to DC, a voltage regulator which stabilizes the voltage to 9VDC. There is also need for a battery backup system that will allow the digital clock to run when there is no power supply or when the supply is interrupted. When the supply is interrupted, data is lost because it contains no memory. One needs to reset it when the supply is restored.

Once the clock is turned ON by pressing the power switch, the 555 timer oscillator which is wired in an astable mode will provide 1Hz clock pulse. The clock pulse is fed into each BCD counter of the seconds' stage. The BCD counter provides a 4 bit 8421 synchronous logic output for every clock pulse received. The BCD counter will enable the units of the seconds and it begins counting from 0 – 9. The BCD output flows into the decoder and the display which shows the counting of the seconds, minutes and hours.

As soon as it count 9 it resets itself on the count of 10 and in turn enables the BCD counter of the Tens stage via pin 7 and pin 5 of the BCD counter of the Unit and Tens display. This makes the clock to display 00 – 99. The counter is then shortened by the

use of AND gate which resets the counter at the count of 00 – 59. When the BCD counter resets, it supplies clock pulse to the Unit of the minutes display. The minutes counts from 00 – 59 and gives a clock pulse to the Unit of the hours. The hours count from 00 to 23 and then reset itself on the count of 24. This process is being repeated every day and the rest is a digital clock. The complete circuit diagram of the clock is shown in figure 3.

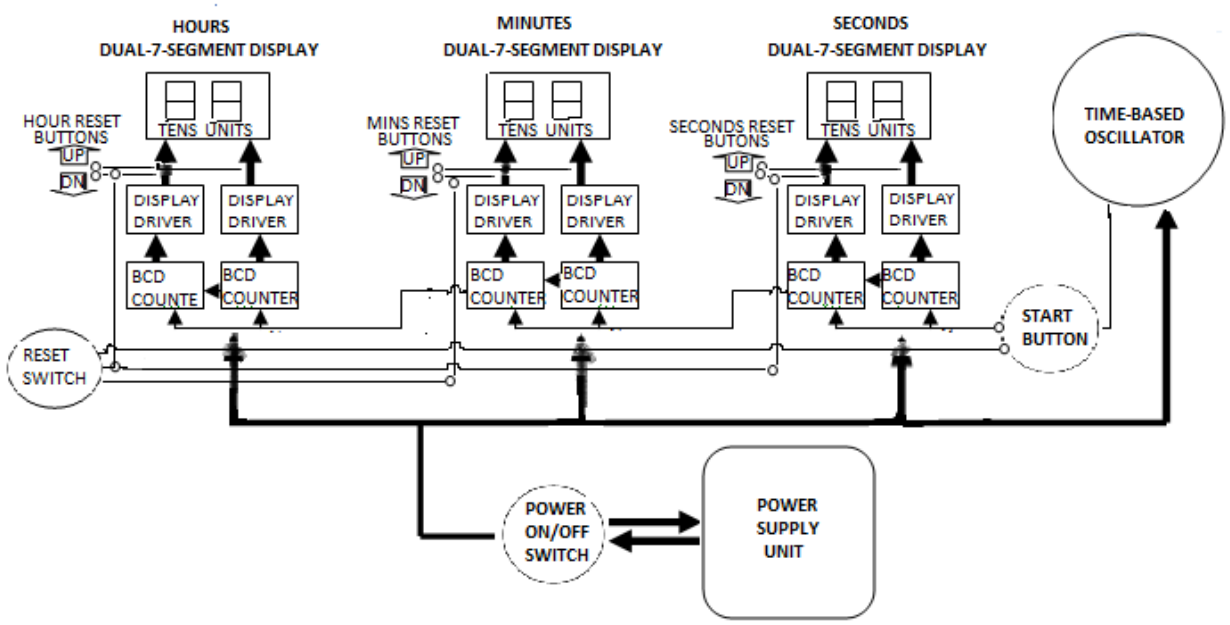

Figure 3: Digital clock circuit diagram

IV. TESTING AND RESULTS

After the design, the required components were purchased and the digital clock was constructed. its performance was found to suit the purpose of the design. all the parts and components functions as required.

Below is the summary of the testing results and the performance characteristics.

Performance characteristics

Accuracy

When the system was initialized and compared with another clock to count down thirty minutes, the clock is faster than the other clocks with two minutes. Thus, the measured time is 32 minutes and the true time is 30 minutes.

Therefore, the relative accuracy = $1 - \left|\frac{32-30}{32}\right|$

= 0.94

And the percentage accuracy is given by;

Percentage accuracy = relative Accuracy $\times 100$

Percentage accuracy = 0.94 × 100

Percentage accuracy = 94%

Error

Absolute error $= measured\ value - true\ value$

The average measured value is taken by using three clocks to determine the error. The average measured value is 32.

Absolute error = 32 − 30

Absolute error = 2

The percentage error is calculated using equation below;

Percentage error = $\frac{measured\ value - true\ value}{measured\ value} \times 100$

Percentage error = $\frac{32-30}{32} \times 100$

Percentage error = 6.25%

Table 2 summary of the results:

Input Voltage	9V DC
Frequency	1 Hz
Visibility	30 feet
Operating temperature	-17^0 to 190^0F
Humidity	0% to 95% non-condensing
% Accuracy	93.7
% Error	6.25
Recommendation	Good

V. CONCLUSION

Despite that the cost of producing digital clocks is higher than that of analog clocks; digital clocks are more common and independent of external source. Analog clocks in most cases uses scale and a pointer, due to this, it is susceptible to parallax and human errors while taking readings which make it less accurate. The design of this digital clock can be altered to perform many applications and can be later changed when improvement are required. This saves both time and money when a field upgrade is required. However, there are limitations with respect to processing power and memory. This digital clock makes use of a 555 timer IC wired in an astable mode and designed to give

output pulse of 1Hz i.e. one second for one complete cycle. The BCD counters are cascaded and various processes are undergone. The use of BCDs allows two BCD digits to be stored within a single byte (8-bits) of data, allowing a single data byte to hold a BCD number in the range of 00 to 99.

REFERENCES

[1] Pan, T. (2008), Development and Implementation of Microcontroller-based Digital Clock, Journal of Academy of Science and Technology, Vol III, Myanmar.

[2] Nachum, A. (2011), Basic Electronics Technology (Series), Scientific Education Systems, SES, Rishon-Lezion 75151 Israel.

[3] G.S.M Galadanci, etal (2015), Design and Deveelopment of a Microcontroller-Based Timing System, Bayero Journal of Physics and Mathematical Sciences, 4:2:91.

[4] Shetty, D. and R. A Kolk, (1997), Mechatronics System design, 2nd Edition, PWS Publishing Company, Boston, MA.

[5] Farcas, etal, (2005), Transparent Distribution of Real-Time Components Based on Logical Execution Time, 1:1, Department of Computer Science, University of Salzburg, Austria.

[6] Aggarwal, etal, (2012), Comparative Implementation of Automatic Car Parking System with least distance parking space in Wireless Sensor Networks, International Journal of Scientific and Research Publications, Volume 2, Issue 10.

AUTHORS

First Author – Auwal Mustapha Imam, Department of Physics with Electronics, Federal University, Birnin Kebbim mustaphaimamauwal@gmail.com, +2348034647088