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Designing of Controller for DVR to Reduce Harmonics in DFIG Wind Turbine

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Abstract- This work presents a control strategy of a dynamic voltage restorer (DVR) to improve the doubly fed induction generator (DFIG) based wind turbine in case of fault. The application of a dynamic voltage restorer (DVR) connected to a doubly fed induction generator (DFIG) based wind-turbine-driven is investigated.Voltage in faulty line can be compensated using DVR, while nominal operation of DFIG wind turbine is continued as demanded in actual grid codes.

A dynamic voltage restorer based on the dqo algorithm is discussed. The proposed control scheme is very effective to detect any disturbance or fault in distribution systems. Simulation results for a 1.5 MW wind turbine using Matlab/Simulink are presented to verify the effectiveness of the proposed scheme.

Index Terms- Doubly fed induction generator (DFIG), dynamic voltage restorer (DVR), Voltage Sag,Reactive Power Compensation,dq0 transformation..

I. Introduction

WIND energy is gaining popularity all over the world as it is environment-friendly renewable energy source . It has advantage over other renewable energy sources like solar energy ,as cost per kilowatt-hour (kWh) is high in later .The contribution of these renewable energy systems to the power system has been increased rapidly. DFIG based wind turbine offer several advantage over Fixed speed induction generator (FSIG)[1]-[4]. Advantages are variable-speed operation, independent control of active [6] and reactive power[5], and its partially rated power converter. It has low converter costs and reduced power losses [6],[7]. Fig. 1 shows the schematic diagram of a DFIG-based wind turbine.

Simple induction generators with rated power converters and the DFIG with partial rating power converters (slip power rating) are the widely preferred topologies for the variable speed operation. DFIG based wind turbine is the most popular option due to varying nature of the wind speeds., Total energy output is 20%–30% higher in case of DFIG-based wind turbine due to variable speed operation, so the cost per kWh energy is reduced

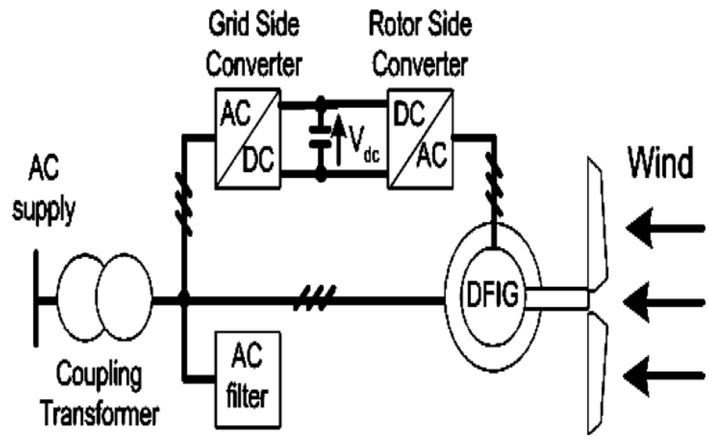


Fig. 1. Schematic diagram of a DFIG-based wind generation system

Fault ride-through capability is the most demanding requirement for doubly fed induction generators (DFIGs) based wind farms. Transmission system must be remain connected when a voltage dip occurs in the grid [8],[9].

A DFIG is a wound-rotor induction generator, where grid and stator are directly connected, and the Rotor windings are fed through a partially rated variable frequency ac/dc/ac converter (VSC), which handles around 24% of the machine rated power while the range of the speed variation is 33% around the synchronous speed [10]. The VSC consists of a rotor-side converter (RSC) and a grid-side converter (GSC) connected back-to-back by a dc-link capacitor. Effective operation in both sub- and super-synchronous speed modes is ensured by controlling rotor current injection using fully controlled bi-directional PWM converters [10].control of both active and reactive powers using the vector control is already discussed [3], [11].Generally the direction of this power flow through the rotor circuit is dependent on the wind speed. Below the synchronous speed, active power flows from the grid to the rotor side and at the time rotor side converter (RSC) acts as inverter while the grid side converter (GSC) acts as a rectifier but above the synchronous speed rotor side converter (RSC) acts as the rectifier, and grid side converter (GSC) acts as the inverter. Other proposed solutions for fault ride-through of a DFIG based wind farms include a series dynamic resistance in the rotor in [12] or in the stator in [13] or using a series grid side converter (GSC) topology as in [14].

Any disturbances in grid voltage has severe effect on DFIGs, as described in [6] and [7] for balanced and unbalanced voltage sag, and requires an extra protection for the rotor side converter. When a voltage sag occurs, sudden change in stator voltage cause unexpected variation in stator flux. As rotor keeps rotating and a high slip occurs, and an overvoltage and overcurrent in the rotor circuit occurs. Higher overcurrents and overvoltages is produced because of asymmetrical faults .as there is negative sequence component in the stator voltage and the slip of this negative sequence component is very high [15]..Wind farms connected to transmission system have to stay connected whenever a voltage sag occurs in the grid, [9].Objective is that disconnection of the DFIG during grid voltage sag is avoided. Various crowbar topologies can be selected, as it is explained in [2]-[4].Crowbar is a resistive network connected to the rotor circuit, in case of rotor overcurrents and disable the rotor side converter (RSC) as described in [15],.Machine draws a high short circuit current whenever the crowbar is activated, and power network draws large amount of reactive power, which is not acceptable according to actual grid code requirements. So,various other methods for protection have to be investigated for fault ride-through of a DFIG.

II. DFIG MODEL

The actual behavior of the DFIG is investigated with dynamic equation which is considered for more realistic observation. The dynamic behavior of the DFIG in synchronous reference frame can be represented by the Park equations where the rotor quantities are referred to the stator side. The stator and rotor voltages in synchronous reference frame are expressed as follows:

$$\left.\begin{aligned} V_{ds} &= R_s i_{ds} + \frac{d\varphi_{qs}}{dt} - \omega_s \varphi_{qs} \\ V_{qs} &= R_s i_{qs} + \frac{d\varphi_{ds}}{dt} + \omega_s \varphi_{ds} \\ V_{dr} &= R_r i_{dr} + \frac{d\varphi_{qr}}{dt} - (\omega_s - \omega_r)\, \varphi_{qr} \\ V_{qr} &= R_r i_{qr} + \frac{d\varphi_{dr}}{dt} + (\omega_s - \omega_r)\, \varphi_{dr} \end{aligned}\right\} \quad (1)$$

The flux linkage equations of the stator and rotor can be related to their currents and are expressed as follows:

$$\left.\begin{aligned} \varphi_{ds} &= L_s i_{ds} + L_m i_{dr} \\ \varphi_{qs} &= L_s i_{qs} + L_m i_{qr} \\ \varphi_{dr} &= L_r i_{dr} + L_m i_{ds} \\ \varphi_{qr} &= L_r i_{qr} + L_m i_{qs} \end{aligned}\right\} \quad (2)$$

Equations (1) to (2) are the set of differential equations which represent a fourth order model for describing the dynamic behavior of DFIG.

III. DYNAMIC VOLTAGE RESTORER (DVR)

Dynamic Voltage Restorer (DVR) is a series connected solid state device which injects voltage into the system and regulate the load-side voltage. It is normally installed in between the supply and the feeder in a distribution system. In the event of a disturbance it boost up the load-side voltage and avoid any power disruption to that load . There are various control schemes and circuit topologies that can be used to implement a DVR. DVR is used to compensate voltage sags and swells, as well as it can compensate line voltage harmonics, reduce transients in voltage and fault current limitations. DVR consists of an injection / booster transformer, a harmonic filter, a voltage source converter (VSC), DC charging circuit and a control and protection system as shown in Figure 2.The DVR injects active power into the distribution line in sag correction techniques during the compensation period . Hence, for long duration sags the capacity of the DC link or energy storage unit become a limiting factor in the disturbance compensation process.

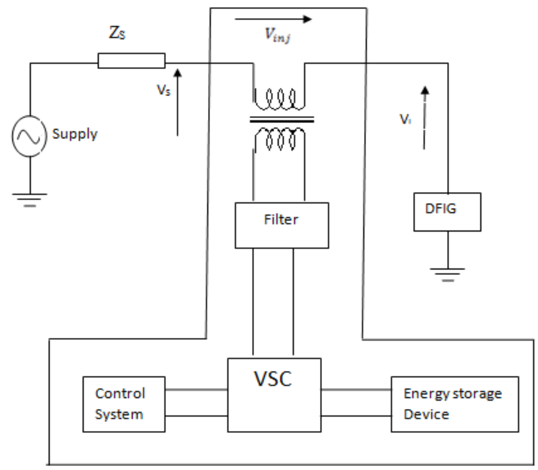


Figure 2.Dynamic Voltage Restorer (DVR) schematic diagram

A .Equivalent Circuit Of DVR:

The DVR does not depend upon the type of fault or any event that happens in the system, but the whole system must be in connection with the grid, i.e. the line breaker does not trip. By compensating the positive economical design can be achieve .Because of infinite impedance for this component. the zero sequence part of a disturbance will not pass through the step down transformer. The equivalent circuit of the DVR is shown in Fig. 3.

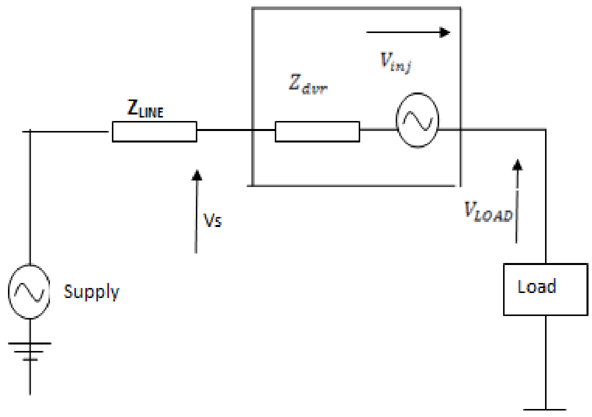


Figure 3 Equivalent circuit of DVR

When the source voltage drops or increases, the desired load voltage magnitude V_L can be maintained by injecting a series voltage V_{inj} through the injection transformer and this is done by DVR The series injected voltage of the DVR can be written as:

$$V_{inj} = V_L + V_S$$

Where, V_L is the magnitude of desired load voltage.

V_S is the source voltage during sags / swells condition.

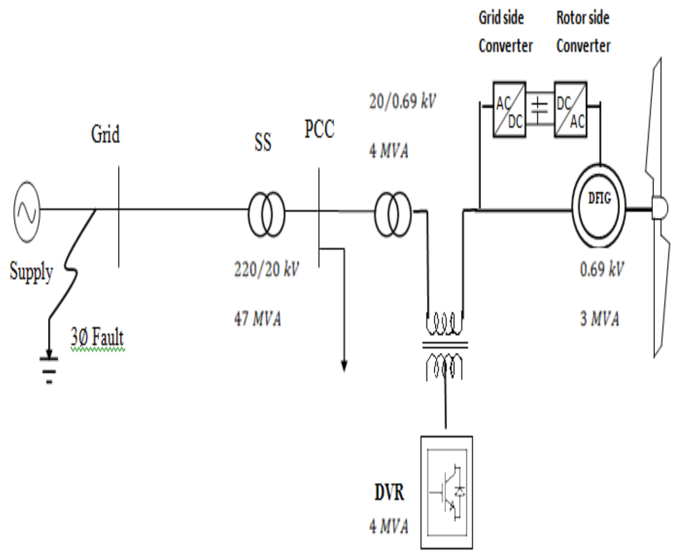
The load current I_L is given by:

$$I_L = \frac{P_L \pm J * Q_L}{V_L}$$

P_L is active power and Q_L is reactive power

IV. PROPOSED METHOD

Figure-4 shows the configuration of the proposed DVR design using single line diagram, where the outputs of a three-phase half-bridge inverter are connected to the utility supply via wye-open connected series transformer.



SS – Substation
PCC – Point of common coupling

Figure 4.: Single Line diagram of test system with DVR

In case of voltage sag/swell, with the aid of dqo transformation based control scheme, the inverter output can be steered in phase with the ac source while the load is maintained constant. Filtering scheme is provided in the proposed method, output of inverter is installed with capacitors and inductors. Task of the filter is to keep the harmonic voltage content generated by the voltage source inverter to the permissible level

The dqo method gives the sag depth and phase shift information with start and end times. The quantities are expressed as the instantaneous space vectors. Firstly convert the voltage from a-b-c reference frame to d-q-o reference. For simplicity zero phase sequence components is ignored.

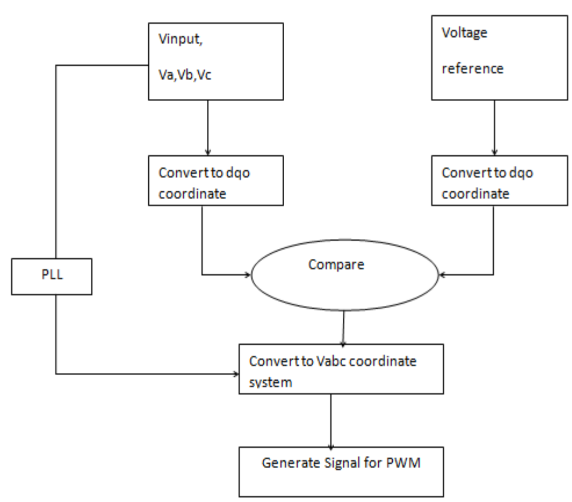


Figure 5: Flow chart of feed forward control technique for DVR based on dqo transformation

Figure-5 illustrates a flow chart of the feed forward dqo transformation for voltage sags/swells detection. The detection is carried out in each of the three phases. The control is based on the comparison of a voltage reference and the measured terminal voltage (Va,Vb,Vc).

The error signal is used as a modulation signal that allows generating a commutation pattern for the power switches (IGBT's) constituting the voltage source converter. The commutation pattern is generated by means of the sinusoidal pulse width modulation technique (SPWM); voltages are controlled through the modulation.

The block diagram of the phase locked loop (PLL) is illustrated in Figure-5. The PLL circuit is used to generate a unit sinusoidal wave in phase with mains voltage.

Simulink diagram of control system is shown in Figure-6.PI controller is used and whose output is fed to PWM generator. The controller may also be used to shift the inverter into rectifier mode to charge the capacitors in the DC energy link in the absence of voltage sags/swells. The dqo transformation or Park's transformation is used to control of DVR.

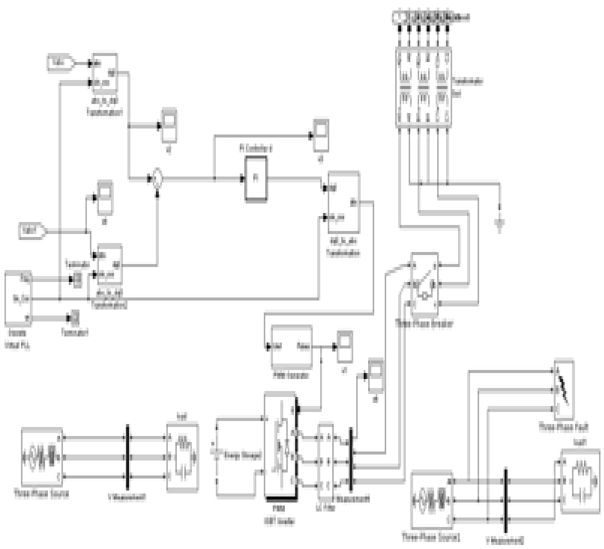


Figure 6 Simulink diagram of control system

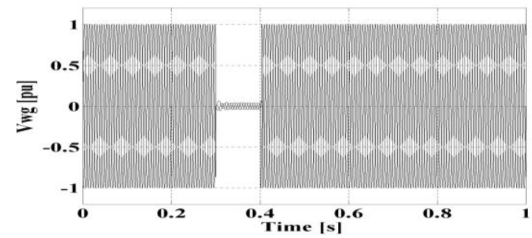
V. SIMULATION RESULT AND DISCUSSION

The Performance of DVR in voltage sag mitigation using the proposed controller, a simple distribution network is simulated using MATLAB/SIMULINK It is assumed that the voltage magnitude of the load bus is maintained at 1 p.u during the voltage sags condition. The results of the most important simulations are represented in Figures. The first simulation of three phase voltage sag is simulated and a three-phase voltage at the utility grid, voltage across DC link in DFIG, Active Power and Reactive power generation of DFIG with 3-Ø fault without DVR is shown in Figure 6.1 (a) -6.1 (d) respectively and three-phase voltage at the utility grid, voltage across DC link in DFIG, Active Power and Reactive power generation of DFIG with 3-Ø fault, with DVR is shown in Figure 6.2 (a) -6.2 (d) respectively. Voltage sag initiated at 0.3s and it is kept until 0.4s, with total voltage sag duration of 0.1s As a result of DVR, the load voltage is kept at 1 pu.

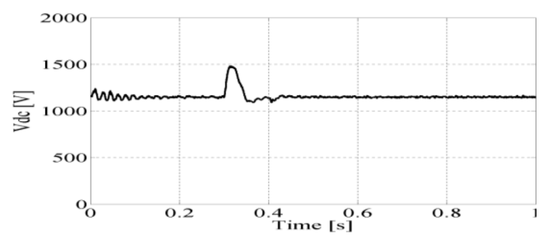
The parameters of the DVR system are as follows (Table-5.1):

TABLE 5.1 SYSTEM DATA

Supply Voltage	480 V
System Frequency	60 H_Z
Series transformer turns ratio	1:2
DC link Voltage	500V
Filter Inductance	0.5H
Filter capacitance	0.5F



(a)



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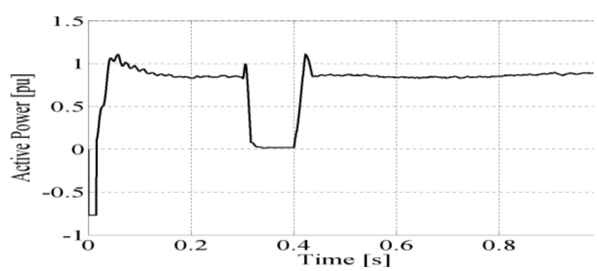

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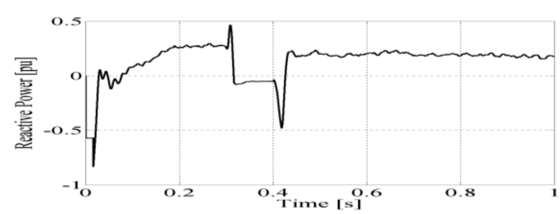
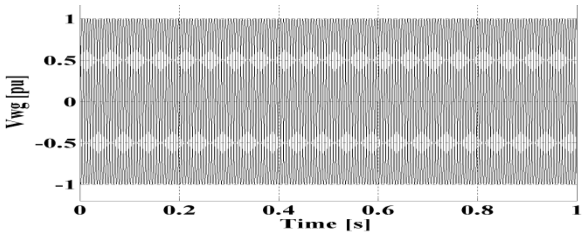


(d)

Figure 6.1: (a) Three-Phase voltage at Load (b) Voltage across DC link in DFIG (c) Active Power of DFIG (d) Reactive Power of DFIG with three phase fault without DVR



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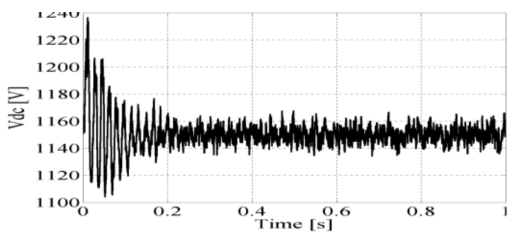

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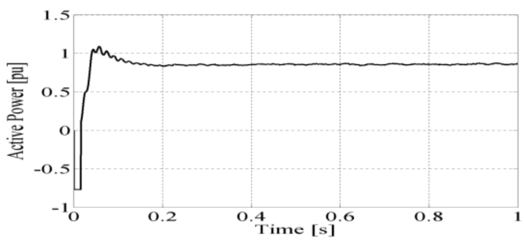

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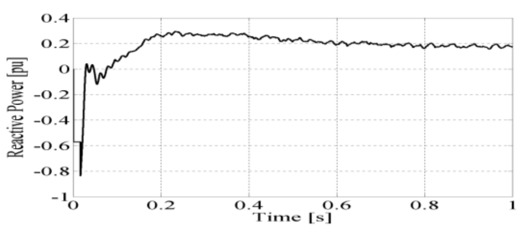

(d)

Figure 6.2: (a) Three-Phase voltage at Load (b)Voltage across DC link in DFIG (c) Active Power of DFIG (d) Reactive Power of DFIG with three phase fault with DVR

VI. CONCLUSION

The modeling and simulation of a DVR using MATLAB/SIMULINK has been presented. A control system based on dqo technique which is a scaled error of the between source side of the DVR and its reference for sags/swell correction has been presented. The simulation shows that the DVR performance is satisfactory in mitigating voltage sags/swells.

The main advantage of this DVR is low cost and its control is simple. It can mitigate long duration voltage sags/swells efficiently. This paper has presented the power quality problems such as voltage dips, swells, distortions and harmonics. Compensation techniques of custom power electronic devices DVR was presented. The design and applications of DVR for voltage sags and comprehensive results were presented. A PWM-based control scheme was implemented.

REFERENCES

[1] S. Muller, M. Deicke, and R. W. De Doncker, “Doubly fed induction generator systems for wind turbines,” IEEE Ind. Appl. Mag., vol. 8, no.3, pp. 26–33, May/Jun. 2002.

[2] H. Akagi and H. Sato, “Control and performance of a doubly-fed induction machine intended for a flywheel energy storage system,” IEEE Trans. Power Electron., vol. 17, no. 1, pp. 109–116, Jan. 2002

[3] R. Pena, J. C. Clare, and G. M. Asher, “Double fed induction generator using back-to-back PWM converter and its application to variable speed wind-energy generation,” Proc. Inst. Elect. Eng. B, vol. 143,no. 3, pp. 231–241, 1996

[4] M. Yamamoto and O. Motoyoshi, “Active and reactive power control for doubly-fed wound rotor induction generator,” IEEE Trans. Power Electron., vol. 6, no. 4, pp. 624–629, Oct. 1991

[5] M.Kayikci and J. Milanovic, “Reactive power control strategies for DFIGbased plants,” IEEE Trans. Energy Convers., vol. 22, no. 2, pp. 389–396, Jun. 2007.

[6] J. Lopez, E. Gubia, P. Sanchis, X. Roboam, and L. Marroyo, “Wind turbines based on doubly fed induction generator under asymmetrical voltage dips,” IEEE Trans. Energy Convers., vol. 23, no. 1, pp. 321–330, Mar. 2008.

[7] M. Mohseni, S. Islam, and M. Masoum, “Impacts of symmetrical and asymmetrical voltage sags on dfig-based wind turbines considering phaseangle jump, voltage recovery, and sag parameters,” IEEE Trans. Power Electron., to be published.

[8] P. S. Flannery and G. Venkataramanan, “A fault tolerant doubly fed induction generator wind turbine using a parallel grid side rectifier and series grid side converter,” IEEE Trans. Power Electron., vol. 23, no. 3, pp. 1126–1135, May 2008

[9] Y. Lei, A. Mullane, G. Lightbody, and R. Yacamini, “Modeling of the wind turbine with a doubly fed induction generator for grid integration studies,” IEEE Trans. Energy Convers., vol. 21, no. 1, pp. 257–264, Mar. 2006.

[10] A. Tapia, G. Tapia, J. X. Ostolaza, and J. R. Saenz, “Modeling and control of a wind turbine driven doubly fed induction generator,” IEEE Trans. Energy Convers., vol. 18, no. 2, pp. 194–204, Jun. 2003

[11] L. Xu and W. Cheng, “Torque and reactive power control of a doubly fed induction machine by position sensorless scheme,” IEEE Trans. Ind. Appl., vol. 31, no. 3, pp. 636–642, May/Jun. 1995.

[12] J. Yang, J. Fletcher, and J. O’Reilly, “A series-dynamic-resistor-based converter protection scheme for doubly-fed induction generator during various fault conditions,” IEEE Trans. Energy Convers., vol. 25, no. 2, pp. 422–432, Jun. 2010

[13] A. Causebrook, D. Atkinson, and A. Jack, “Fault ride-through of large wind farms using series dynamic braking resistors (march 2007),” IEEE Trans. Power Syst., vol. 22, no. 3, pp. 966–975, Aug. 2007.

[14] P. Flannery and G. Venkataramanan, “Unbalanced voltage sag ridethrough of a doubly fed induction generator wind turbine with series grid-side converter,” IEEE Trans. Ind. Appl., vol. 45, no. 5, pp. 1879–1887, Sep./Oct. 2009.

[15] S. Seman, J. Niiranen, and A. Arkkio, “Ride-through analysis of doubly fed induction wind-power generator under unsymmetrical network disturbance,” IEEE Trans. Power Syst., vol. 21, no. 4, pp. 1782–1789, Nov.2006.

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