

FPGA-Based Quad Transmit/ Receive Module (QTRM) Controller Design

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Abstract- Ultra- small size transmit/ receive module is reported with regard to active phased arrays by the application of GaAs MMIC technique. This makes possible the production of Quad TRMs, while satisfying the basic requirements for transmit/ receive modules- wide band, high output power, low noise figure, small size and weight and low cost and sufficient gain in both transmit and receive. This paper focuses on the control of one such X-band QTRM using FPGA.

Index Terms- Active Electronically Scanned Array (AESA); GaAs MMIC; Quad Transmit Receive Module (QTRM); Field Programmable Gate Array (FPGA)

I. INTRODUCTION

The active transmit/ receive (T/R) modules are essential elements for the construction of active phased array antennas with a broad range of applications for radars, communications and electronic warfare systems. The control circuit has following functions^[1]:

- Receives control data from external beam steering unit
- Controls six-bit phase shifter and attenuator
- Controls pulse operation of the T/R amplifier
- Controls the T/R switching
- Controls the timing sequences for the above operations

Earlier, control circuits consisted of dedicated gate array LSI IC for interface. As technology evolved, various methods have been employed for the purpose. The QTRM discussed in this paper operates in the X- band and uses ACTEL FPGA Fusion device AFS600 256 FPGA as controller. It operates at a clock frequency of 160 MHz, serial data transfer rate of 20 Mbps. Figure 1 shows the basic TR module block diagram.

II. PROJECT IMPLEMENTATION

A. Current Problem

A variety of technical problems face one looking to equip an airplane with X radars. Modern radars systems are often implemented as active electronically scanned arrays (AESA) with hundreds of transmit/receive modules aligned in an array. One advantage of an active electronically scanned array is that it can perform radar scans without physically turning the radar array. This is accomplished by altering the phase of the transmitted radars. By synchronizing^{[2],[3]} the phases of each of the transmit/receive modules, the beam transmitted points in a different direction. However, in order to change the direction of

the radar beam (i.e., the main lobe) the transmitted radars must be packed close enough together to work in unison.

X band radar^{[4],[5],[6]}, is transmitted at approximately 10-12 GHz. Because such high frequencies are being used, the transmit/receive modules must be packed very tightly. In an active electronically scanned array, the lattice spacing must be approximately half of the wavelength of the highest frequency used. Thus, the demanded space requirements are too small for the current size of transmit/receive modules.

In addition to the size of the modules, a designer must also contend with the size of the connections to and from modules. Prior art designs require bulky connectors connecting a module to a radiating element. Prior art designs also require a connector from the module to a manifold interconnect.

Thus we are now into the generation of integrating TR modules so as to have common control and interface units for them. One such stage is that of the QTRM. For the four TR modules bound together, the control code now has to be optimized and the health of the board has to be monitored for power and temperature.

B. Functional Flow of TR Module

Figure 2 depicts the handling of data by the control logic. Data from the Plank Controller arrives at the SPI slave block @ 20 Mbps through SPI communication protocol. This data consists of a header, phase and attenuation information for each TRM of the QTRM, mode and parity check byte (total 19 bytes). The SPI_SLAVE block checks for header error and passes the data to PARITY_CHECK block if no error, else data is discarded. Similarly, the PARITY_CHECK block checks for errors in the data received by bitwise- XORing of the bytes, and discards the received data if error is detected. An indication of the error and location of the error is also recorded in the status information. Otherwise the data moves into the PARSER section.

The PARSER section extracts phase and attenuation information for each TRM from the received data, and the mode and latches on to this data when the Start of Burst (SOB) signal goes HIGH. Now the mode is analyzed for generating the control signals for the different components on board. The mode, along with the Pulse Repetition Time (PRT) signal determines the control of the on-board limiter (Lim), low-noise amplifier (LNA), power amplifier (PA), Tx/Rx switch (Sw), core-chip power amplifier (Core_PA) and core-chip low-noise amplifier (Core_LNA).

At the same time, the status bytes are prepared to be sent back. This is done by the STATUS_COLLECTOR block. It receives error indications from PARITY_CHECK block and PRT block, and analog data recorded from board. Analog data includes temperatures from two on-board temperature sensors, and voltages converted to digital data by the on-board ADC.

Other blocks include the RC_OSC which is the on-board clock generator that supplies clock to the different blocks. PRT block makes sure that the incoming PRT signal has ON-time and duty cycle as per specified requirements only; else it modifies PRT and reports it through the status information.

8 modes of operation have been implemented in the project:

- Normal: The received phase and attenuation data are routed to the respective TRMs
- PPFA (Pulse-to-pulse Frequency Agility): This mode is used to battle clutter interference.
- Receive Calibration: One TRM, specified in the information received, would receive its phase and attenuation data for receive mode while the other TRMs would have all set to 0.
- Transmit Calibration: One TRM, specified in the information received, would receive its phase and attenuation data for transmit mode while the other TRMs would have all set to 0.
- Receive Isolation: All TRMs in OFF condition.
- Transmit Isolation: All TRMs in OFF condition.
- Link status: This mode is used to verify the data flow. Dummy values are sent into the QTRM and if all goes well, a pre-decided status format is sent back.
- Reset: This mode resets the QTRM board.

The control operation can be reset-ed either by an on-board reset or by specifying RESET mode in the external command coming in.

FIFO structures have been used for the PPFA mode so as to store phase and attenuation values for 4 TRMS for 32 PRT pulses; at each pulse a fresh value would be loaded. This would cause rapid changes in phase and attenuation values loaded into the antenna elements and lessen probability of external agents interfering with this data.

C. Implementation Details

The programming was done in VHDL language using ACTEL board AFS600. Simulation was done on ModelSim and results were verified using ChipScope and Oscilloscope.

Figure 3 shows the hardware set-up and figure 4 shows the final results achieved. Resource utilization was reported to be 37% (Core cell usage was found to be 5176.) I/O cells used were 88 and 20 out of 24 Block RAMS were used. The maximum clock frequency is 100 MHz and serial communication rate is 20 Mbps. The static power consumption was found to be 46.74 mW and dynamic power consumption is 165.444 mW.

D. Limitations

A possible improvement to the logic for the upcoming designs could be a more efficient means of parity checking rather than bitwise-XORing. A number of efficient and secure algorithms are today available in the market that can be used.

E. Figures

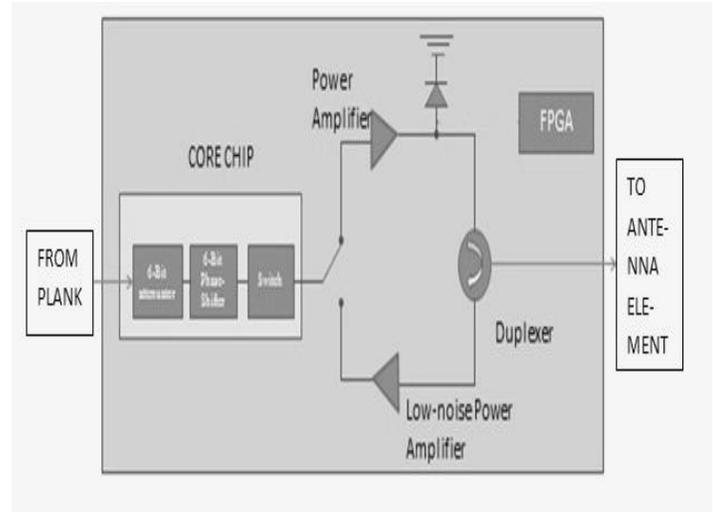


Figure 1: Basic TR Module block diagram

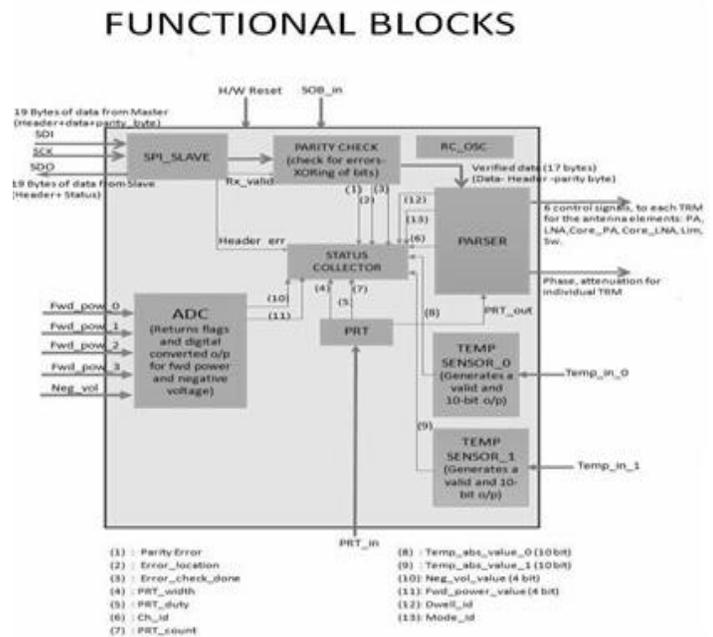


Figure 2: Functional Flow

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