Modified Multilevel Inverter Topology with Reduced Switch Count and a Novel PWM Control Scheme

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Abstract- Multilevel converters offer high power capability, associated with lower output harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. This paper proposes a single-phase seven- level inverter for grid connected PV systems, with a novel pulse width-modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels from the dc supply voltage. This paper proposes a new multilevel inverter topology using an H-bridge output stage with two bidirectional auxiliary switches. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output using the Asymmetric Cascade configuration.

Index Terms- Asymmetric cascade configuration, H-Bridge, multilevel inverter, pulse width Modulation.

I. INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [3].

Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3], [4]. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped [5]–[10], flying capacitor or multicell [11]– [17], cascaded H-bridge [18]–[24], and modified H-bridge multilevel [25]–[29].

This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

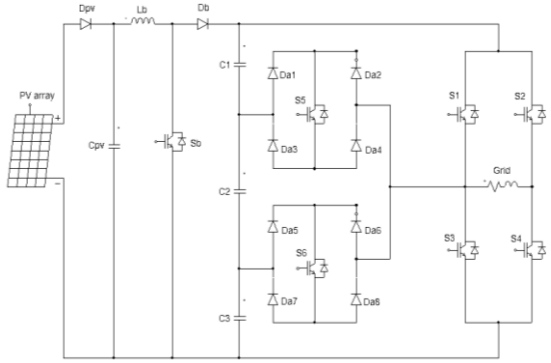

Fig 1: Proposed single-phase seven-level grid-connected inverter for photovoltaic systems.

II. PROPOSED SYSTEM

The proposed single-phase seven-level inverter was developed from the five-level inverter in [25]–[29]. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C_1, C_2, and C_3, as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance *Lf* was used to filter the current injected into the grid. Proper switching of the inverter can

produce seven output-voltage levels (V_{dc}, $2V_{dc}/3$, $V_{dc}/3$, $0, -V_{dc}, -2V_{dc}/3, -V_{dc}/3$) from the dc supply voltage. The proposed inverter's operation can be divided into seven switching states, as shown in Fig. 2(a)–(g). Fig. 2(a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig. 2(b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage. The required seven levels of output voltage were generated as follows.

1) Maximum positive output (V_{dc}): S_1 is ON, connecting the load positive terminal to V_{dc}, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is V_{dc}. Fig. 2(a) shows the current paths that are active at this stage.
2) 2) Two-third positive output ($2V_{dc}/3$): The bidirectional switch S_5 is ON, connecting the load positive terminal, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $2V_{dc}/3$. Fig. 2(b) shows the current paths that are active at this stage.
3) One-third positive output ($V_{dc}/3$): The bidirectional switch S_6 is ON, connecting the load positive terminal, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $V_{dc}/3$. Fig. 2(c) shows the current paths that are active at this stage.
4) Zero output: This level can be produced by two switching combinations; switches S_3 and S_4 are ON, or S_1 and S_2 are ON, and all other controlled switches are OFF; terminal *ab* is a short circuit, and the voltage applied to the load terminals is zero. Fig. 2(d) shows the current paths that are active at this stage.
5) One-third negative output ($-V_{dc}/3$): The bidirectional switch S_5 is ON, connecting the load positive terminal, and S_2 is ON, connecting the load negative terminal to V_{dc}. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}/3$. Fig. 2(e) shows the current paths that are active at this stage.
6) Two-third negative output ($-2V_{dc}/3$): The bidirectional switch S_6 is ON, connecting the load positive terminal, and S_2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-2V_{dc}/3$. Fig. 2(f) shows the current paths that are active at this stage.
7) Maximum negative output ($-V_{dc}$): S_2 is ON, connecting the load negative terminal to V_{dc}, and S_3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is $-V_{dc}$. Fig. 2(g) shows the current paths that are active at this stage.

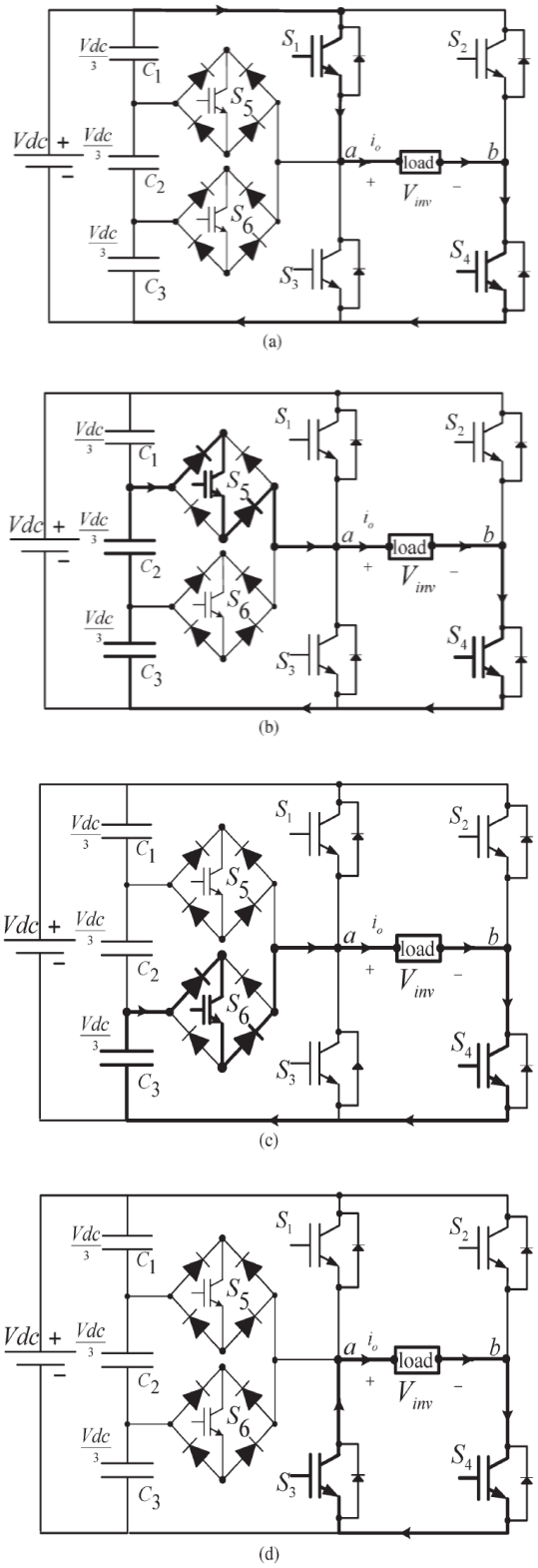

Fig. 2. Switching combination required to generate the output voltage (V_{ab}). (a) $V_{ab} = V_{dc}$. (b) $V_{ab} = 2V_{dc}/3$. (c) $V_{ab} = V_{dc}/3$. (d) $V_{ab} = 0$.

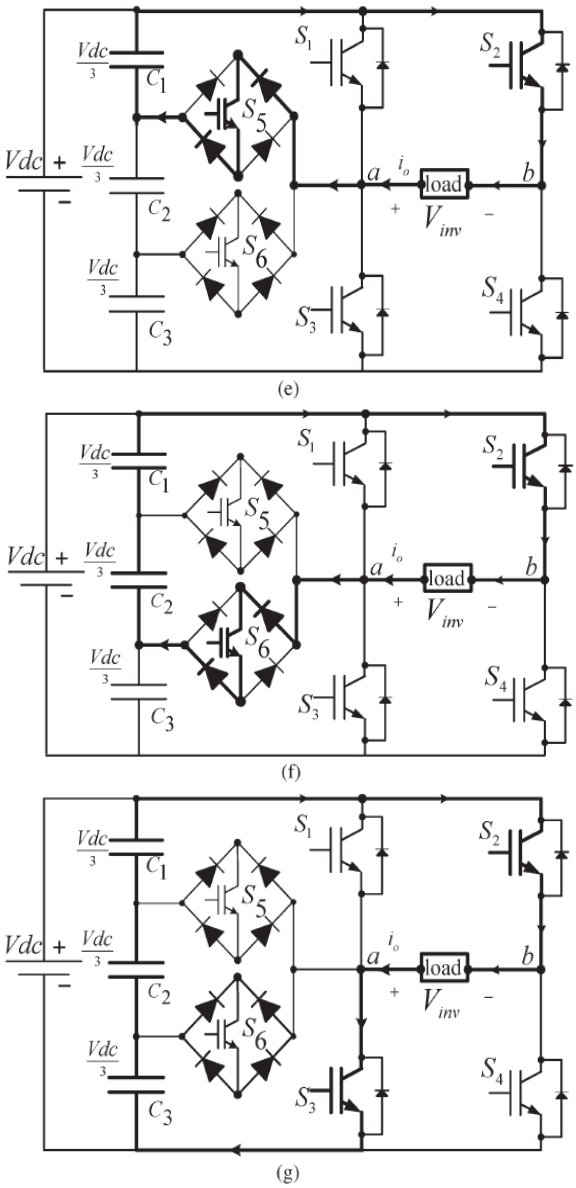

Fig. 2. (*Continued*.) Switching combination required to generate the output voltage (V_{ab}). (e) $V_{ab} = -V_{dc}/3$. (f) $V_{ab} = -2V_{dc}/3$. (g) $V_{ab} = -V_{dc}$.

TABLE I
SWITCHING CONDITION

v_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	on	off	off	on	off	off
$2V_{dc}/3$	off	off	off	on	on	off
$V_{dc}/3$	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
$-V_{dc}/3$	off	on	off	off	on	off
$-2V_{dc}/3$	off	on	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off

III. PWM MODULATION

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (*V*ref1, *V*ref2, and *V*ref3) were compared with a carrier signal (*Vcarrier*). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If *V*ref1 had exceeded the peak amplitude of *V*carrier, *V*ref2 was compared with *V*carrier until it had exceeded the peak amplitude of *V*carrier. Then, onward, *V*ref3 would take charge and would be compared with *V*carrier until it reached zero. Once *V*ref3 had reached zero, *V*ref2 would be compared until it reached zero. Then, onward, *V*ref1 would be compared with *V*carrier. Fig. 3 shows the resulting switching pattern. Switches *S*1, *S*3, *S*5, and *S*6 would be switching at the rate of the carrier signal frequency, whereas *S*2 and *S*4 would operate at a frequency that was equivalent to the fundamental frequency.

IV. CONTROL SYSTEM

The control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current generation, and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics.

The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it.

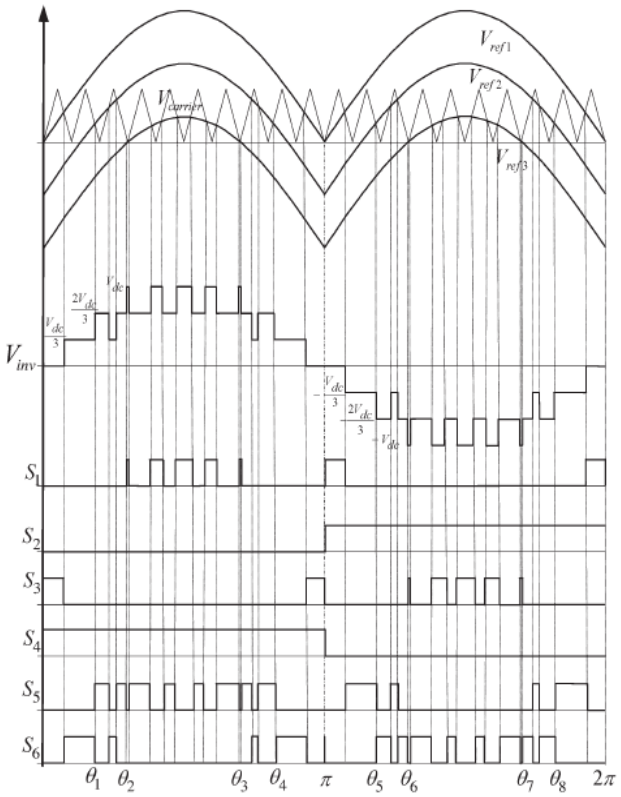

Fig. 3. Switching pattern for the single-phase seven-level inverter.

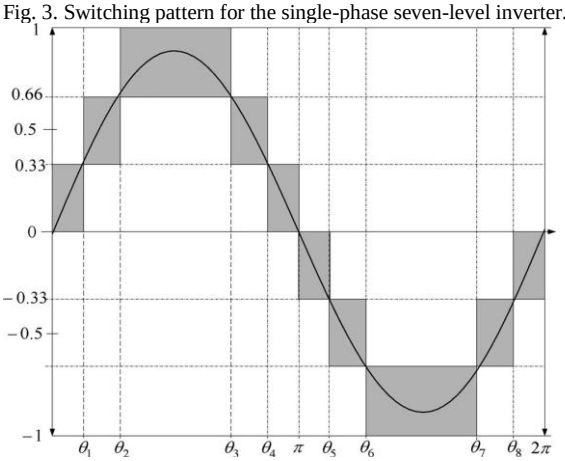

Fig. 4. Seven-level output voltage (V_{ab}) and switching angles.

The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage *V*dc was controlled in the dc–ac seven level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc–dc boost converter (*V*dc) constant by comparing *V*dc and *V*dc ref and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the *V*dc can be maintained at a constant value and at more than √2 of *V*grid to inject power into the grid.

A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current *I*grid, was sensed and fed back to a comparator that compared it with the reference current *I*gridref . *I*gridref is the result of the MPPT algorithm. The error from the comparison process of *I*grid and *I*gridref was fed into the PI controller.

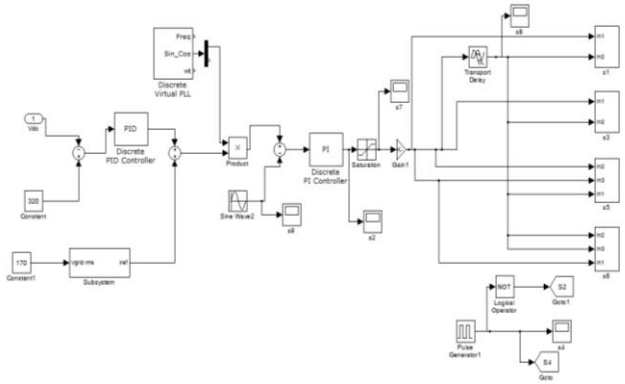

Fig.5.Control system block.

The output of the PI controller, also known as *V*ref , goes through an antiwindup process before being compared with the triangular wave to produce the switching signals for *S*1–*S*6. Eventually, *V*ref becomes *V*ref1; *V*ref2 and *V*ref3 can be derived from *V*ref1 by shifting the offset value, which was equivalent to the amplitude of the triangular wave. The mathematical formulation of the PI algorithm and its implementation in the DSP are discussed in detail in [28].Control system block is shown in figure 5.

V. SIMULATION RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (*V*ref1, *V*ref2, and *V*ref3) against a triangular carrier signal. Subsequently, the comparing process produced PWM switching signals for switches *S*1– *S*6.

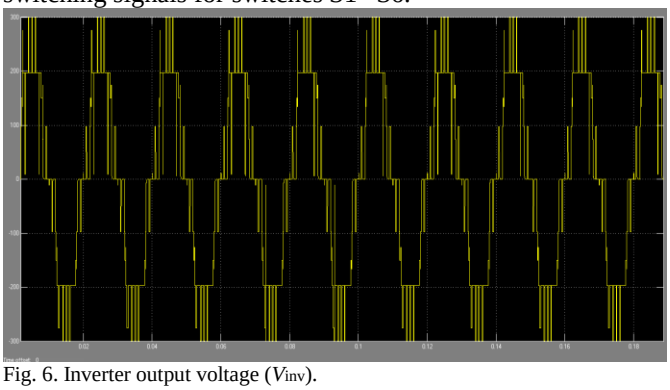

Fig. 6. Inverter output voltage (V_{inv}).

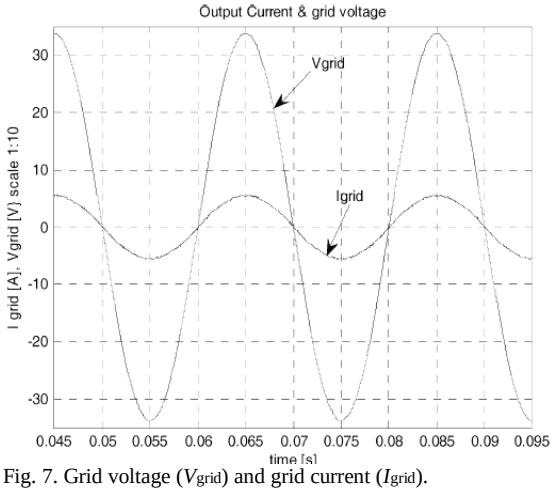

Fig. 7. Grid voltage (V_{grid}) and grid current (I_{grid}).

One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches *S*5 and *S*6 also operated at the rate of the carrier signal. Fig. 6 shows the simulation result of inverter output voltage *V*inv. The dc-bus voltage was set at 300 V (> √ 2*V*grid; in this case, *V*grid was 120 V). The dc-bus voltage must always be higher than √ 2 of *V*grid to inject current into the grid, or current will be injected from the grid into the inverter. Therefore, operation is recommended to be between *Ma* = 0.66 and*Ma* = 1.0. *V*inv comprises seven voltage levels, namely, *V*dc, 2*V*dc/3, *V*dc/3, 0, −*V*dc, −2*V*dc/3, and −*V*dc/3. The current flowing into the grid was filtered to resemble a pure sinewave in phase with the grid voltage (see Fig. 7). As *I*grid is almost a pure sinewave at unity power factor, the total harmonic distortion (THD) can be reduced compared with the THD in [28].

VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The less THD in the seven-level inverter compared with that in the five- and three-level inverters is an attractive solution for grid-connected PV inverters.

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