Design of Sample & Hold Circuit

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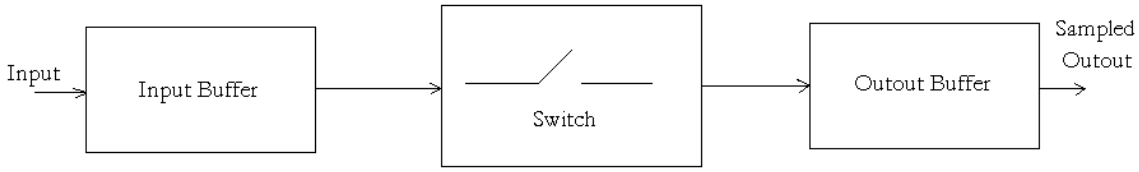
Abstract- This paper describes the design of a high-speed CMOS Sample and Hold circuit in front of an analog to digital converter (ADC). Sample and hold (S/H) circuit employs linear source follower buffer at input and output. Synopsys cosmosSE software tool has been used for schematic design, H-spice for Simulation and Cscope for waveform performance. Complete S/H circuit has designed with tsmc035 (Taiwan semiconductor manufacturing corporation) technology, with 2.5V power supply. Power consumption of 5 mW for 8 MHz at 53 MS/s.

Index Terms- sampling and hold circuit analog to digital converter

I. Introduction

ADC is an essential component for DSP because most signals in the natural world such as voltage, current, and voice are analog. Sample and Hold circuits are required in front of high speed ADCs to improve their performance [1]. Also its CMOS implementation is very important because of its low cost and single-chip integration of analog and digital parts is possible. We have designed a high-speed CMOS S/H circuit. High-speed S/H circuits for low voltage operation have already been implemented with BiCMOS and bipolar technologies [2, 3].



II. Design & Implementation

The basic elements of a sample & hold circuit are a storage element and a switch. These are generally implemented by using a capacitor (for storing) and a MOSFET for sampling through a CLK control signal. But as a single MOSFET may not pass the positive and negative voltages in the same way, it is replaced with a Tx gate. The sizing of this Tx gate will decide the ON resistance of the switch and this will decide the RC time constant for charging the capacitor. Two buffers are used to avoid the loading on the source when sampling, and to avoid the charge discharge through the capacitor when it is in the hold mode. These buffers are implemented with an OPAMP in a voltage follower configuration as shown in the figure2

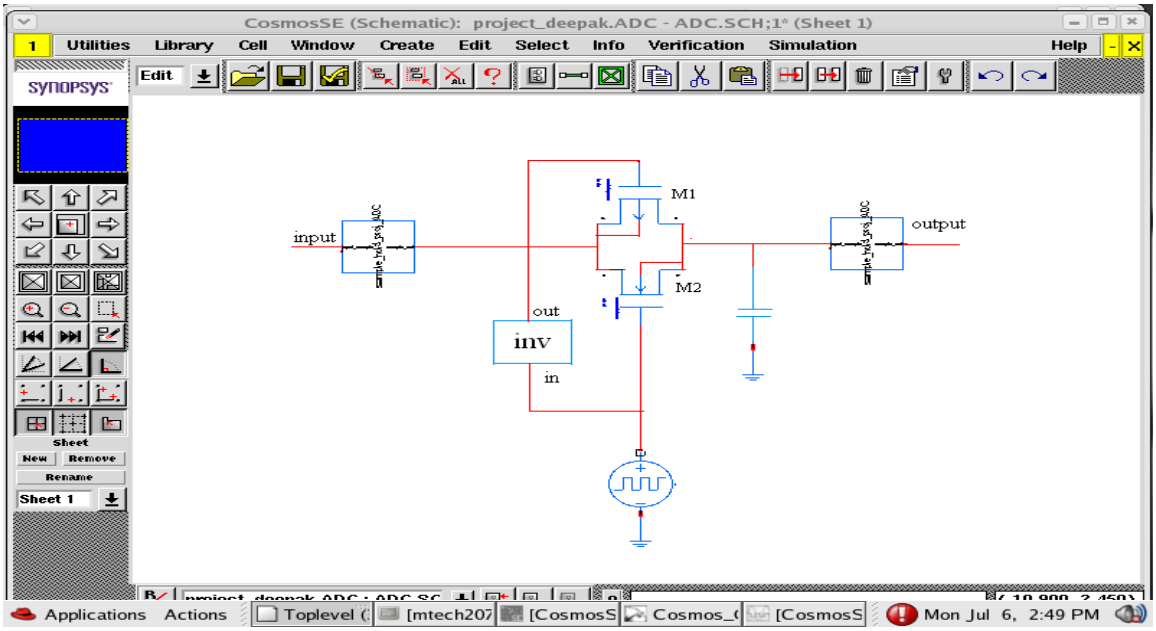


Figure 2 Schematic of Sample & hold Circuit

The sampling CLK is given to the CONTr of the Tx gate. When the CLK is high the input signal is sampled through the 1st buffer and the capacitor is charged to the input level. When once the CLK goes to LOW, then the path from the input is open circuited and the sampled voltage is maintained constant and given to the preceding block for conversion. For a better sampling the sampling rate should be at least 2 times to that of the input signal frequency

III. Sampling Strategy

The sampling period is kept small as compared to holding period; this is kept so that the output of the OPAMP will get settled, two clocks of same period but nonoverlapping in nature are used one for sampling the analog voltage and other is used to latch the converted data. This method is chosen because, if the output is directly taken from the comparator the output of ADC will oscillate and so that output of DAC which will result in cumulative error and thus a flip-flop is put in front of comparator so as to convert the settled value from S/H amplifier

IV. Simulation Result

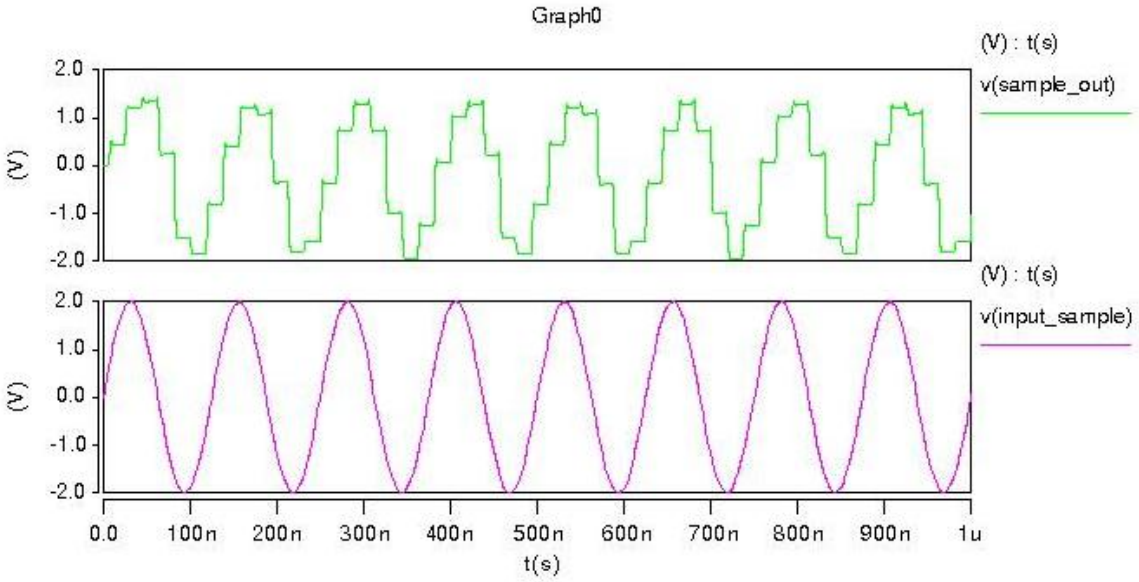


Figure 4 shows the transient result of sample and hold circuit

V. Conclusion

It is a high speed with high sampling rate Sample and hold circuit. It's indispensable circuit for analog to digital converter. It has no loading affect at the input due to source and it not suffers from the charge discharge through the capacitor when it is in the hold mode.

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