Dual Edge Adaptive Pulse Triggered Flip-Flop for a High Speed and Low Power Applications

S. Harish*, Dr. M. Satyanarayana**

* Department of ECE, MVGR College of Engineering
** Department of ECE, MVGR College of Engineering

Abstract- Pulse-triggered flip-flops are mainly used to improve speed of operation (pipeline speed), though flip-flop robustness and system timing closure are challenging in a wide range of supply voltages. Usually pulse-triggered flip-flops have specific structures and transistor sizes to optimize the system performance. The transistor size, topology, and threshold voltage of the flip-flop make the timing characteristics sensitive to the supply voltage. The transparent windows generated and required in a pulse-triggered flip-flop may have mismatch under different supply voltages (scaling), which is likely to result in system timing and functional failures. in single edge adaptive pulse trigger flip-flops the latching speed is less, no of transistors are more and power dissipation also high so to overcome these limitations dual edge adaptive pulse triggered flip flop is proposed. Proposed structure improves the robustness of adaptive pulse-triggered flip-flops and promises this high-speed clocked element for wide range of supply voltages so data latching speed is increase, numbers of transistors were reduced and power dissipation also reduced. Transistor driving-strength mismatches are considered and overcome by Dual edge adaptive pulse trigger flip flop implemented in 130nm technology**.**
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Index Terms- *Flip-Flop, Process variation, Standard cell, Sub threshold circuit*

I. INTRODUCTION

The Flip flops are basic memory elements which are used to store one bit memory. Flip flops are used to design sequential circuits. Similarities have been observed between high-speed and sub threshold circuits, such as having serious timing un certainty and high sensitivity to process variations. Therefore, an important clocked storage element, an adaptive pulse triggered flip-flop, is introduced from gigahertz pipelines to boost the speed of sub threshold operations. High-performance processors employ pulse-triggered flip-flops that have low latency means time interval between simulation and the result. High performance processors help to mitigate the influence of clock uncertainty however super- and sub-threshold circuits have critical differences in transistor models. Circuit topologies, transistor sizes, and threshold voltages have strong impacts on the circuit delay in near- and sub-threshold regions. Multi threshold circuit is nothing but single circuit consists of both high and low threshold transistors. These transistors are used to reduce the leakage problem especially high threshold transistors are used to suppress the sub threshold leakage current and low threshold transistors are used to achieve high performance. The flip-flop delay, setup time, and hold time have a nonlinear shift when he dynamic voltage scaling (DVS) Covers super-threshold and sub threshold voltages; therefore, timing closure is complicated. Sub threshold pulse-triggered flip-flops are less robust than sub threshold master–slave latches because the transparent window is hard to control. Prior works have surveyed and analysed conventional flip-flops operated at sub threshold voltages. Pulse-triggered flip-flops usually require structural revisions to be operated in the sub threshold region. In contrast, master–slave latches can use transistor sizing for the same robustness.

Pulse-triggered flip-flops have a positive hold time that maybe close to the clock-to-Q delay. Internal race immunity (IRI)is thus a major issue for sub threshold pulse-triggered flip-flops. IRI may be negative when the hold time increases faster than the clock-to-Q delay during DVS. Process variations are also factors that cause negative IRI. Simply reducing the hold time cannot solve the internal-race problem because short hold time indicates a narrow transparent window, which causes a lack of robustness to capture data. In contrast, master–slave latches are relatively stable with respect to the internal race since their hold time is close to zero or a negative number. However, master–slave latches are slow when a processing Element requires high performance at a high voltage. Pulse-triggered flip-flops reduce latency on critical paths and benefit the operating speed. Therefore, robust pulse-triggered flip-flops help processing elements to achieve high performance at near- to super-threshold voltages, while the sub threshold mode is still available to save energy. Above consideration motivates this work.

System performance has been known to be sensitive to the supply voltage selected for logic synthesis and optimization. The delay of each standard cell, including flip-flops, has individual sensitivity with respect to the supply voltage. Static timing analysis then becomes complicated because timing violations should be checked in a wide range of supply voltages. Optimization of flip-flops thus has to include both conventional performance-based objectives and new timing closure criteria considering possible operating voltages. Challenges of voltage-scalable pulse-triggered flip-flops and a novel structure are detailed in this brief, introducing a

solution for robust pipelines operated in a wide range of voltages. Section II discusses the major issues of single edge pulse-triggered flip-flop and proposes a novel structure.

II. CONVENTIONAL TRANSMISSION GATE FLIPFLOPS

Conventional transmission gate flip flops are single edge pulse trigger flip flops. Every flip flop is driven by the pulse generators. The operation of any flip flop mainly depends upon the clock generators.a standard explicit-pulsed transmission-gate flip-flop (TGFF), which usually uses a pulse generator consisting of an odd-stage inverter chain. The inverter chain creates a phase difference; the overall circuit generates a positive pulse at node C_1 and a negative pulse at node C_2 every clock rising edge.

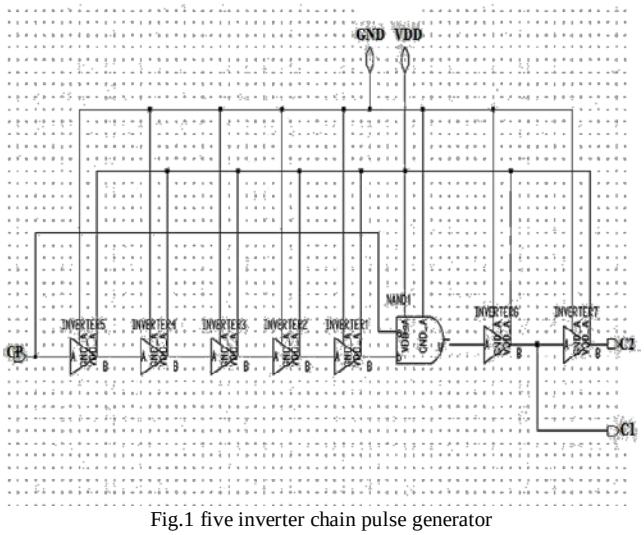

Fig.1 five inverter chain pulse generator

In this conventional pulse trigger flip flops mainly discuss about three inverter chain pulse generator flip flops, five inverter chain pulse generator flip flops, seven inverter chain pulse generator flip flops and replica path pulse generator flip flops. In three inverter chain pulse trigger flip flops due to insufficient delay unable to get exact simulation results. For getting exact simulation results need to increase number of buffer circuits (inverters) by increasing number of inverters due to these adding inverters produce exact simulation results. Even though got exact simulation results in both five inverter chain and seven inverter chain flip flops number of transistor is increase. These increase in number of transistors causes increase in area this is not good for any sequential circuit design. While coming to fourth one replica path pulse generator in this pulse generator uses transmission gate instead of inverter chains and in this some slight changes are happen.

The relation between the TGFF and D-Q delay and the pulse width. The flip-flop delay rapidly increases when the pulse width is narrow .The proper zone for the transparent window. A narrow transparent window increases the error rate of data latching and pipeline timing. Although a wide transparent window seems riskless for flip flop functions, it increases the hold time. A large hold time may lead to negative IRI and require extra delay cells to satisfy the minimum pipeline delay Wide-voltage-range operations thus introduce challenges in the design and optimization of pulse circuits. The transparent window optimized under a given supply voltage cannot guarantee error-free timing at a different supply voltage. Circuit optimization in the sub threshold region is quite different from that in the conventional super-threshold region.

Near- and sub threshold circuits have additional strategies to allocate transistor sizes and circuit topologies. A transistor with a long channel length may increase the driving strength due to the reverse short channel effect. The inverse narrow width effect another factor. Serial-connected structures have much weaker driving strength at lower voltage due to the stacking effect. The transparent windows generated and required in a flip flop may have mutual mismatches due to different circuit topologies between the pulse generator and flip-flop data path. For instance, the transmission gate delay in a TGFF has a time constant related to the drain capacitance and stacked transistors, different from that of an inverter chain. The stacking effect increases the DFF delay, while the pulse created by an inverter chain cannot simply reflect. Furthermore, the circuit optimization can be much more complicated because part of the transistors may have long channel lengths or multiple threshold voltages, and these specific elements are hard to simulate using an inverter chain.

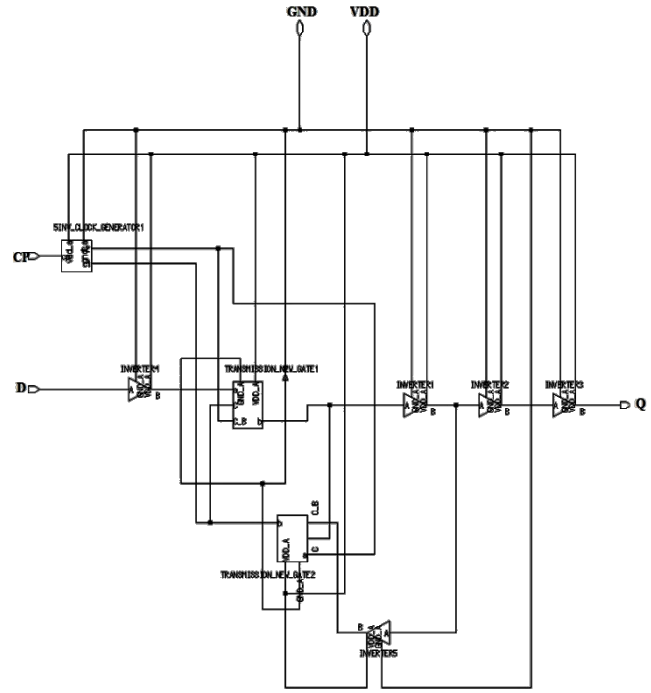

Fig.2 Five inverter chain pulse triggered flip-flop

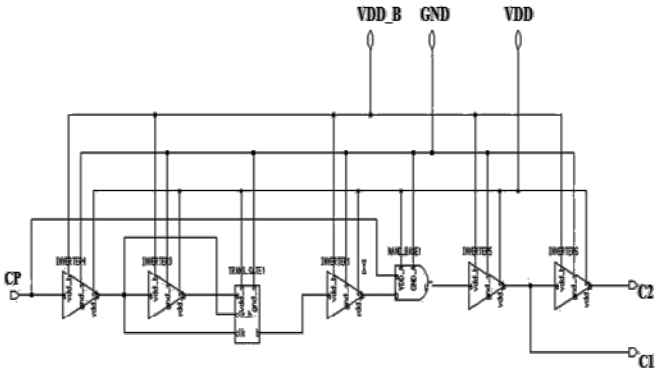

Fig.3 Replica path pulse generator

A replica-path pulse-triggered flip-flop is thus proposed to simplify design effort and achieve robust timing characteristics. The idea is to let the pulses generated and required have a high correlation in a wide range of operating voltages a replica delay circuit copies part of the critical path of the flip-flop, including the circuit topologies, transistor sizes, and threshold voltages. The replica simulates the latency of the flip-flop after being triggered, and the transparent window is guaranteed to open during the data propagation period. The proposed replica-path pulse-triggered flip-flop. The replica path requires simplification because there is no more pulse signal for the replica. Therefore, the replica transmission gate is fed by a signal from the front inverter to simulate the signal slew rate.

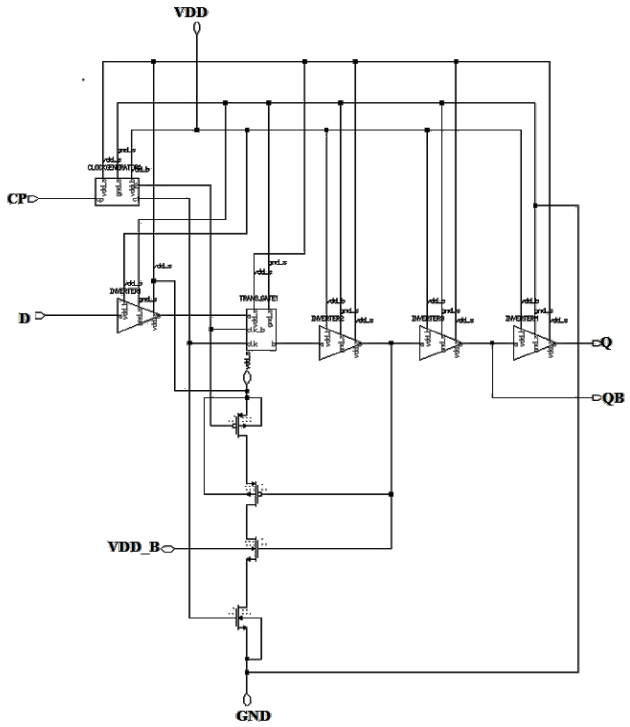

Fig.4 Replica path pulse trigger flip flop

This simplified replica path achieves an approximate flip-flop D-Q delay, especially similar to the D-Q falling delay. Therefore, balancing the rising and falling D-Q delay helps this replica to be more effective. The transistors of the proposed flip-flop are assigned with different threshold voltages based on the feature of a 130 nm technology, in which a standard-threshold-voltage (SVT) PMOS has lower driving strength than an SVT NMOS, and as does the relation between a low-threshold-transistor (LVT) PMOS and an LVT NMOS. The threshold voltages of SVT and LVT of this technology are about 0.4 V and 0.3 V respectively.

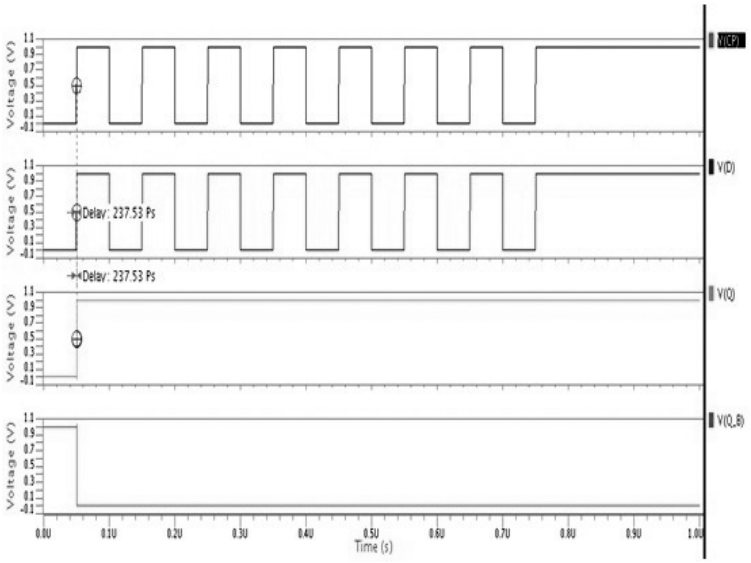

Fig.5 Simulation wave forms

III. PROPOSED DUAL EDGE ADAPTIVE FLIPFLOP

Dual-edge triggering, Data latching or sampling is used at both the rising and falling edges, usually allows the clock routing network to consume less power. For a system with at throughput of one operation per cycle and a clock frequency, double-

edge triggering results in two operations being executed in one cycle, if we use half the frequency, we can maintain the same throughput of the original system. With half the frequency, the clock switching activity is reduced by half, which leads to considerable power savings in the clock routing network. Dual edge triggered flip-flop design is used to reduce leakage current, it can receive input signal at two levels of the clock dual edge triggered flip-flop has ideal logic functionality, simple structure lower delay time, and higher maximum data rate compared to other existing flip. The figure 5 contains two transmission gates and five inverters. The overall circuit generates positive pulse at both rising and falling edge of pulse at C_1 and generates negative pulse at both rising and falling edge of pulse at C_2.

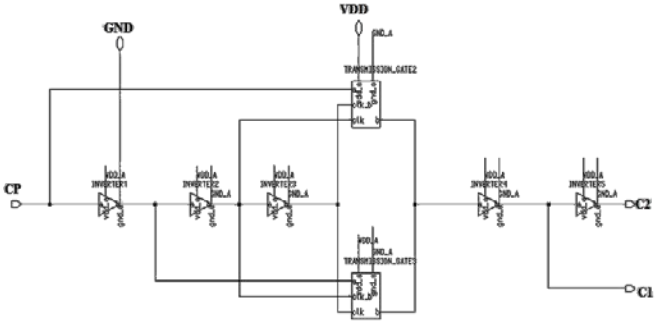

Fig.6 Dual edge pulse generator

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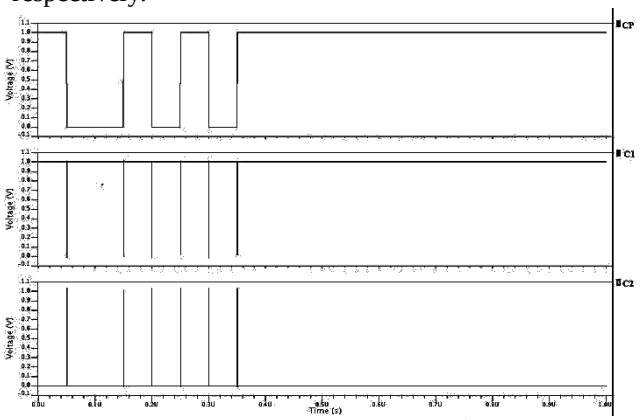

Fig.7 Dual edge simulation wave forms

A. Body bias concept:

In figure 8 The threshold voltage of the transistor changes by applying proper body voltage to the body terminal of the transistor. The body voltage of the transistor changes based on our threshold voltage requirement. Inverter contains PMOS threshold voltage (SVT) 0.4v and NMOS threshold voltage (LVT) 0.3vthe threshold voltage of all the transistors which are used in the flip flop fixed with 0.3v.For SVT PMOS case the threshold voltage is 0.4v so need to change the threshold voltage of the transistor by applying proper body voltage mentioned as VDD_B and VDD_B1.The transistors of the proposed flip-flop are assigned with different threshold voltages based on the feature of a 130 nm technology, in which a standard-threshold-voltage (SVT) PMOS has lower driving strength than an SVT NMOS, and as does the relation between a low-threshold-transistor (LVT) PMOS and an LVT NMOS. The threshold voltages of SVT and LVT of this technology are about 0.4 V and 0.3 V respectively.

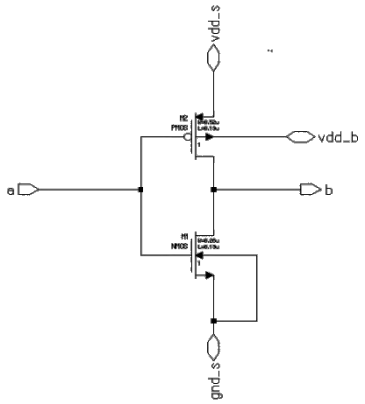

Fig.8 Inverter with body bias

An intrinsic mismatch in driving strength is one of the DVS limitations. Sizing transistor to compensate for this intrinsic mismatch is area-consuming and ineffective. Small and identical-sized LVT PMOS and SVT NMOS transistors are found to have a similar driving strength from near- to sub threshold supply voltages.

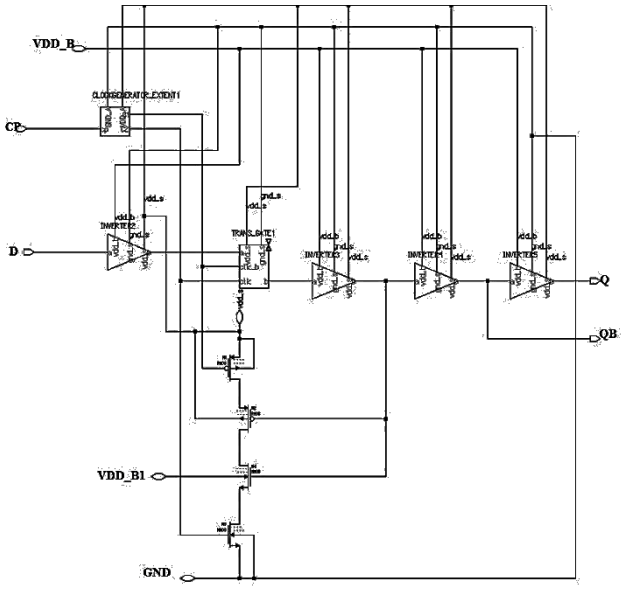

Fig.9 Replica path pulse trigger flip flop

Each inverter in the flip-flop thus incorporates an SVT NMOS and an LVT PMOS. Both cell area and noise margins are improved using this dual-threshold combination. The NAND gate in the pulse generator uses LVT NMOS due to the stacked pull-down network. LVT transistors are assigned to the pulse-controlled paths to boost the circuit speed. A tri-state inverter in the reverse direction of the latch is designed for sub threshold robustness considering process variations. Figure 8 shows the simulation results of proposed structure the data changes at every rising and falling edge of clock.

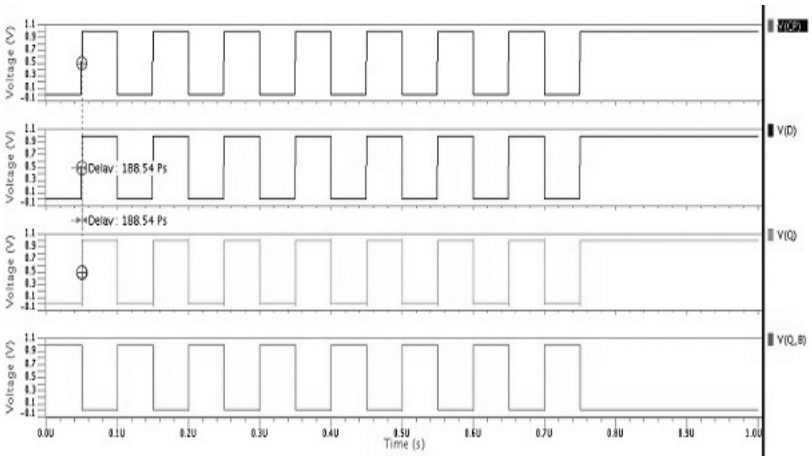

FiG.10 proposed simulation wave forms

TABLE I COMPARISON OF FLIP FLOPS:

Type of Flip Flop	D-Q Delay	CLK-Q Delay	Power Dissipation	No of Transistors
NAND Based FF	182.67 ps	158.6 ps	14.641 nw	-
Three inverter chain	41.21 ns	91.21 ns	53.867 uw	28
Five inverter chain	50.237 ns	237.21 ps	53.740 uw	32
Seven inverter chain	50.238 ns	237.76 ps	53.744 uw	36
Adaptive pulse	50.227 ns	226.65 ps	268.66 nw	32
proposed Dual edge flip flop	186.71 ps	186.71 ps	35.794 nw	28

B. Implementation of mod4 ring counter:

The figure 9 shows implementation of mod4 ring counter by using proposed adaptive dual edge adaptive flip flop. The synchronous Ring Counter is preset so that exactly one data bit in the register is set to logic "1" with all the other bits reset to "0". Pulse is applied to the input of the first flip-flop before the clock pulses are applied. This then places a single logic "1" value into the circuit of the ring counter. So on each successive clock pulse, the counter circulates the same data bit between the four flip-flops over and over again around the "ring" every fourth clock cycle. But in order to cycle the data correctly around the counter we must first "load" the counter with a suitable data pattern as all logic "0's" or all logic "1's" outputted at each clock cycle would make the ring counter invalid.

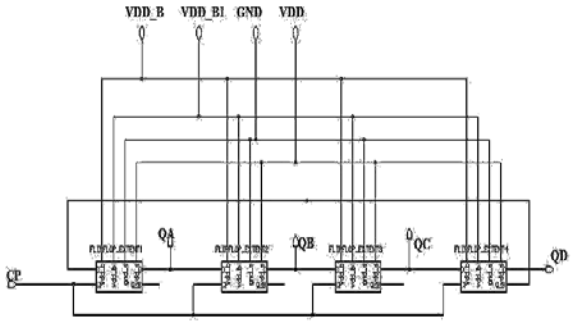

Figure 11 mod4 ring counter

This type of data movement is called "rotation", and like the shift register, the effect of the movement of the data bit from left to right through a ring counter.

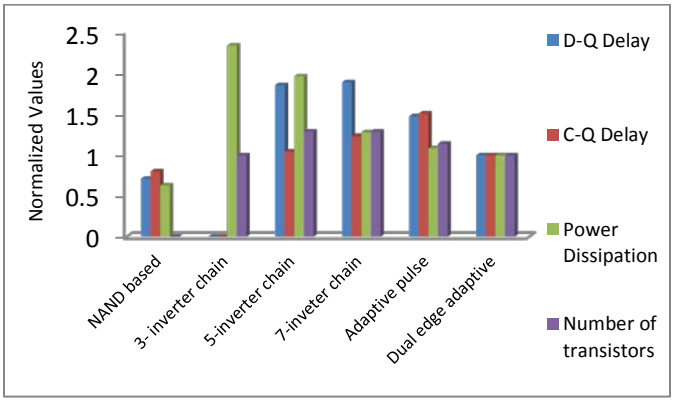

Figure 12 Comparison of different Flip-flop parameters

IV. CONCLUSION

In proposed dual edge triggered flip-flop even though the clock load increased the overall power dissipation is reduced. By reducing the power consumption in sequential elements the overall power consumption in circuits decreased drastically and by using dual edge pulse generator in place of single edge pulse generator the number of transistors reduced. So the complexity of adaptive pulse trigger flip flop reduced.

Dual edge adaptive pulse triggered flip flop mainly used in low power and high speed applications because of its high speed switching activity.

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AUTHORS

First Author – S. Harish, M.Tech (pursuing), MVGR College of Engineering and spharish498@gmail.com.
Second Author – M. Satyanarayana, M.Tech PhD, MVGR College of Engineering and profmsn26@gmail.com.

Correspondence Author – S. Harish, spharish498@gmail.com, 9951537240.