The Design of Low Noise Amplifiers in Nanometer Technology for WiMAX Applications

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Abstract- In this paper the design of two low noise amplifiers proposed for WiMAX applications is presented. The two low noise amplifier topologies implemented are: (1) cascoded common source amplifier, (2) Shunt feedback amplifier. The amplifiers are implemented in a standard 180nm CMOS process, and are operated with a 1-V supply voltage and 5.9GHz frequency, the cascoded LNA achieved the best performance with a simulated gain of 15.7dB and noise figure of 1.85dB. The Low noise amplifier has been simulated using cadence spectre.

Index Terms- CMOS; Low-noise-amplifier (LNA); WiMAX

I. INTRODUCTION

The rapid advancement in CMOS scaling and RF CMOS circuit design techniques in the past few years have made it possible to integrate all the elements of a transceiver on a single chip. Inexpensive CMOS technologies have been used successfully to implement all the necessary RF functionality for existing and emerging wireless area network standards, such as Bluetooth and WiMAX [1] [2].The CMOS system-on-chip (SOC) solution to enable a single chip phone, where the analog and digital basebands, power management, and the RF transceiver are fully integrated on a single monolithic CMOS Integrated circuit.

WiMAX is a telecommunications technology which stands for Worldwide Interoperability for Microwave Access. It belongs to the IEEE 802.16 family of standards, which aim to provide wireless broadband access. It provides data rates of up to 100 Mbps at 20 MHz bandwidth [3]. It has a very large coverage area of around 50 km. for one base station which makes it a viable option for implementation of last-mile connectivity. There are two types of WiMAX systems: Fixed WiMAX and Mobile WiMAX. The fixed WiMAX system does not allow handoff between base stations. Mobile WiMAX on the other hand provides both mobile and fixed services.

II. LOW NOISE AMPLIFIERS

The low noise amplifier (LNA) is the vital component in the receiver chain of the communication system. It is the first gain stage behind the antenna in the receiver chain and its noise figure is directly added to the whole system. The LNAs are used to amplify the very weak signals coming from the antenna.

A. Cascoded Common Source Amplifier

The most frequently used topology for LNA design is the cascoded common source amplifier with inductive source degeneration show in the Fig. 1[4]. The cascoded common source amplifier is also called as telescopic cascode amplifier because the cascode transistor is the same type as the input transistor [5].

The cascode topology gives a higher gain, due to the increase in the output impedance and it also has a better isolation between the input and output ports. The cascode common source amplifier has a higher reverse isolation [6]. The suppression of the parasitic capacitances of the input transistor also improves the higher frequency operation of the amplifier.

B. Shunt Feedback Amplifier

The shunt feedback low noise amplifier is show in the Fig. 4[4]. It has some attractive benefits, like supporting input and output match over a large frequency range and it is able to achieve a very high linearity. The linearity of the amplifier improves the gain, which is largely set feedback, becomes less sensitive to the gain of the amplifier. The feedback elements, which are composed of a resistor in series with a capacitor, linearize the gain and increase the bandwidth of the amplifier. The feedback is also suited for the CMOS low noise amplifiers since the input impedance of MOSFETs is large and mostly capacitive, which means that the input impedance can be controlled and set by the feedback. To improve the high frequency performance, an additional inductor can be positioned in series with the resistor and capacitor [7]. Finally, the high self resonance frequency of inductors, enabled by a post processing technique, has been exploited to achieve a wideband, high impedance drain load.

III. CIRCUIT DESIGNS

The performance requirement for a WiMAX receiver is listed in Table I. These receiver specifications are obtained from the IEEE 802.16 standard released in 2004 [8]. The next part of the design involves the mapping of the specifications from the IEEE standard to relevant system level parameters such as Bit Error Ratio (BER), Signal to noise ratio (SNR), and receiver sensitivity. These system level specifications are then mapped into block level using link budget analysis [9].

Table II. Summarizes the block level specifications for the low noise amplifier. The LNA must be able to achieve high gain and low noise figure to relax the gain requirement of the mixer and at the same time give the whole receiver a low noise figure. The noise figure also determines the minimum input signal that can be resolved by the LNA while the linearity dictates the maximum input signal level that will not cause nonlinear operation. The LNA, having a finite reverse isolation and being connected directly to the antenna, needs a good input and output match to

prevent signals from leaking back to the antenna and getting retransmitted causing unwanted interference.

TABLE I. WiMAX receiver requirements and specifications

Rx max input level on channel reception tolerance	≥ -30 dBm
Rx max input level on channel damage tolerance	≥ 0 dBm
1st adjacent channel rejection	≥ 4 dBm
2st adjacent channel rejection	≥ 23 dBm
Image rejection	≥ 60 dBm
Noise Figure	≤ 7dB

TABLE II. Low Noise Amplifier Specifications

Parameter	**LNA Design**
Technology	180nm
Frequency	5.9GHz
Gain	> 15dB
Power Dissipation	< 4mW
Noise Figure	< 3dB
S12 (dB)	- 45.86
S11 (dB)	-10.3
S22 (dB)	-14.5

A. Cascoded Common Source Amplifier

In schematic of the designed cascoded common source amplifier is shown in Fig. 1. The input impedance of the cascoded common source low noise amplifier circuit shown in Fig. 1 will be capacitive due to the gate source capacitance C_{gs}. To reduce the noise and improve the power gain in the circuit a lossless degenerating inductor L_s is added to the source of the cascode transistor M_1. The input impedance of the LNA can be computed based on (1) [4], with the value of source inductance L_s. The width of the cascode transistor M_2, was set equal to the width of the input transistor to take advantage of the reduced junction capacitance in the layout. The output matching network, composed of the drain inductor, L_d, and the output capacitors, C_1 and C_2, can be designed. Fig. 2 shows the final simulation design of the cascoded common source LNA with device sizes and bias voltages. Fig. 3 shows the layout design of cascoded common source LNA [10].

$$Z_{in} = \left(\frac{g_m}{C_{gs}}\right) * L_s \qquad (1)$$

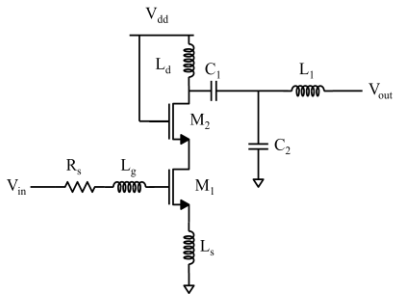

Figure 1. Schematic design of cascoded common source LNA

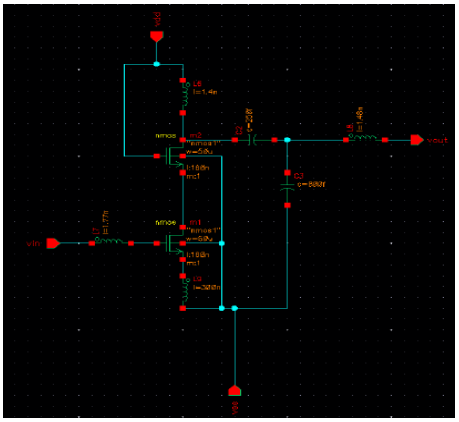

Figure 2. Simulation setup to analyse the design of cascoded common source LNA

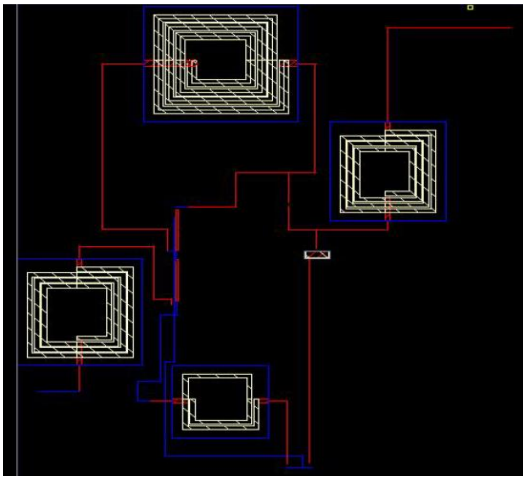

Figure 3. Layout design of cascoded common source LNA

B. Shunt Feedback Amplifier

The design of shunt feedback low noise amplifier is shown in Fig. 4, the value of the feedback resistor which sets the power gain is given in (2) [4], where R_f, Z_o, and S_{21} are the values of the feedback resistor, output impedance, and the transducer gain. A small inductor was placed in the gate of the transistor to aid input matching. A load inductor was placed in the drain of the transistor to tune out the junction capacitances in the drain of the transistor. The value of the feedback capacitor, which is used for biasing purposes, was set large enough to not have a significant effect on feedback. The Fig. 5 and Fig. 6 shows the simulation and the layout design of the shunt feedback LNA.

$$R_f = Z_o\,(1+ |S_{21}|). \qquad (2)$$

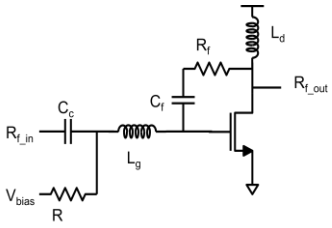

Figure 4. Schematic design of shunt feedback LNA

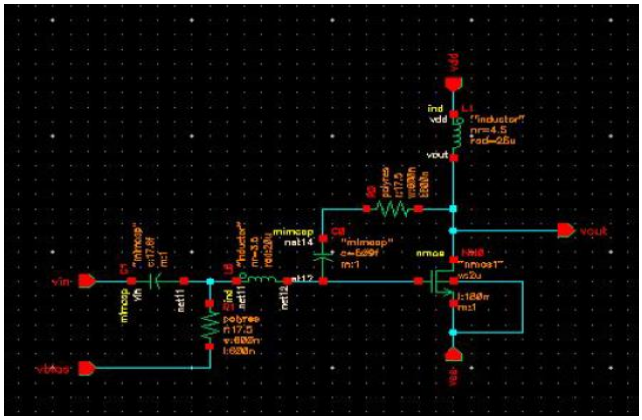

Figure 5. Simulation setup to analyse the design of shunt feedback LNA

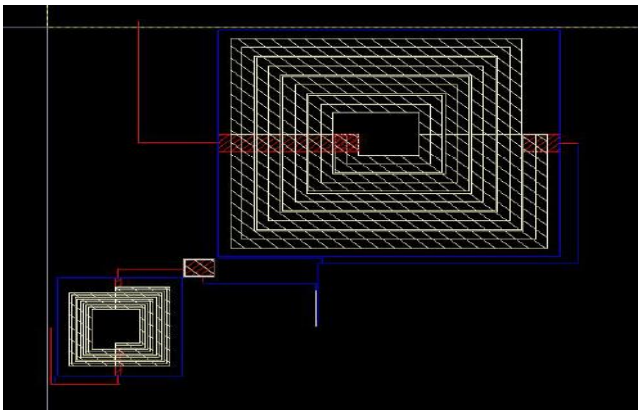

Figure 6. Layout design of shunt feedback LNA

IV. CALCULATION AND ANALYSIS

The LNA topologies were implemented in a standard 180- nm CMOS process. The extraction of all device parameters for use in simulations was done using Virtuoso Schematic Composer and Spectre Simulator from Cadence Design System. The low-noise amplifiers were designed to operate at the frequency band of 5.725 GHz to 5.925 GHz and the measurements in the plots were taken at 5.9 GHz.

A. Inductive Source Degeneration Input Matching

The first constraint on the LNA was to assure that the input impedance matches the source impedance, i.e. the LNA presents a purely resistive load of 50Ω to the antenna, in order to maximize the power transfer.

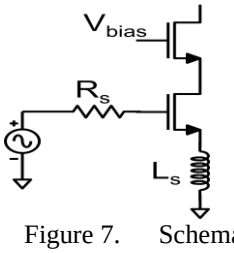

Figure 7. Schematic of a cascode LNA design with source degeneration

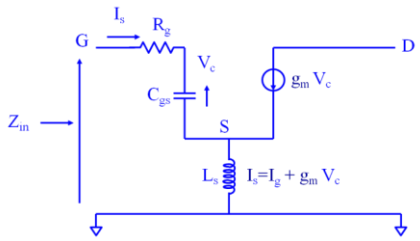

Figure 8. Equivalent model with source degeneration

$$Z_{in} = \frac{V_g}{I_g} = \frac{I_g R_g + V_c + j\omega I_S L_s}{I_g}$$

$$Z_{in} = \frac{L_s \cdot g_m}{C_{gs}}$$ where Z_{in} may be say 50ohms

In most LNA designs the value of Ls is picked and the values of gm and Cgs are calculated to give the required Z_{in}.

B. Degeneration Inductor L_S

The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology.

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{R_S}{L_S} = \frac{50}{1nH} = 50GHz$$

C. Optimal Q of Inductor

Optimal Q is given by:

$$Q_L = \sqrt{1 + \frac{1}{P}}$$

Where $p = \frac{\delta.\alpha^2}{5.\gamma}$

The parameters for p are dependent on the CMOS technology but typically α is assumed to be 0.8 -1 (take to be 0.9)

δ is set to 2 - 3 times the value of (normally 4)

y is set between 2 - 3 (normally 2)

Where $p = \frac{4.(0.9)^2}{5.4} = 0.162$

$$Q_L = \sqrt{1 + \frac{1}{0.162}} = 2.67$$

D. Evaluation of L_G

$$L_g = \frac{Q_L R_S}{\omega_o} - L_S$$

Where ω_O = centre frequency

$2\pi.5.9G = 3.7E^{10}$ rad/sec

$L_g = \frac{2.67x50}{3.7\ E^{10}}$ - 1nH = 2.6nH

E. To Find C_{GS} (Gate-Source Capacitance)

$$C_{gs} = \frac{1}{\omega_o{}^2(L_{gs}+L_s)}$$

$$C_{gs} = \frac{1}{(3.7\ E^{10})^2(2.6nH+1nH)} = 0.205pF$$

F. To Find W

$$W = \frac{3\ Cgs}{2\ Cox\ .Lmin}$$

$$W = \frac{3 \times 0.205pF}{2 \times 3.419E^{-3} \times 0.6E^{-6}} = 158.7um$$

$L_{min} = 0.6E^{-6}$ m; $T_{ox} = 1.01\ E^{-8}$ m

$\varepsilon_{ox} = \varepsilon_{ox} . \varepsilon_o$

Where

ε_s = dielectric constant for silicon = 3.9 and

ε_o = dielectric constant for free space = $8.854E^{-14}$ F/cm

$$C_{ox} = \frac{\varepsilon ox}{Tox} = \frac{3.9 \times 8.854\ E^{-14}}{1.01\ E^{-8}} = 3.419E^{-3}\ pF/um^2$$

G. To Calculate g_m

$g_m = \omega_T . C_{gs}$

g_m = 50GHz x 0.205pF = 0.01025A/V

H. To find V Effective

$$V_{eff} = (V_{gs}-V_T) = \frac{g_m \cdot L_m}{\mu_n . C_{ox} . W}$$

μ_n = device mobility = 433cm/V

$$V_{eff} = \frac{0.01025 \times 0.6E^{-6}}{433 \times 3.419E^{-3}\ pF/um2 \times 158.7um}$$

V_{eff} = 0.25uV

V_T = 0.7v

$V_{eff} = (V_{gs} - V_T)$

$V_{gs} = V_{eff} + V_T$

V_{gs} = 0.25 + 0.7

V_{gs} = 0.95V ~ 1V to the gate

I. Bias Current I_D

$I_D = g_m . V_{eff}$ = 0.01025A/V x 0.25V =2.565mA

J.Estimated Optimum Noise Figure

$$NF_{opt} = 1 + \frac{2\gamma}{\alpha}\left(\frac{\omega_o}{\omega_T}\right)\sqrt{p}(|c| + \sqrt{p} + \sqrt{1+p}\,)$$

Take |c| = 0.4

$$NF_{opt} = 1 + \frac{4}{0.9}\left(\frac{3.7\ E^{10}}{50G}\right)\sqrt{0.16}(0.4 + \sqrt{0.16} + \sqrt{1+0.16}\,)$$

NF_{opt} = 4.2 =10 log (4.2) = 6.3dB

V. SIMULATION RESULTS

A. Power Gain (S21)

To compensate noise contribution of subsequent stages in the receiver chain, it is desirable to have a LNA with power gain (S21) more than 15 dB. So, the shunt feedback amplifier has the highest gain with 19.9 dB and the cascoded common source amplifier has the gain with 15.7 dB is achieved at 5.9 GHz. As can be seen on the plot of the power gain, the shunt feedback amplifier has a relatively wideband characteristic compared to the cascode amplifiers. The linearizing effect of feedback gives the shunt feedback amplifier its wideband characteristic compared to the narrowband characteristic of the cascode amplifiers is illustrated in Fig. 9.

B. Noise Figure (NF)

The plot of the noise figure is shown in Fig. 10. The extracted noise figures of the LNA topologies are as follows: 1.85 dB for the cascoded common-source and 2.63 dB for the shunt feedback amplifier. All the LNA topologies achieved a noise figure below 3 dB. As with the power gain plot, the cascoded common source amplifier achieved the less noise figure compared to the shunt feedback amplifier.

C. Input Matching (S11)

In general, it is difficult to achieve both noise matching and power matching simultaneously in an LNA design, since the source admittance for minimum noise is usually different from the source admittance for maximum power delivery. The input matching of the designed low noise amplifiers should be less than –10 dB while maintaining lowest noise figure. In the designed cascoded common source LNA has -9.5dB and shunt feedback LNA has -11.2dB is achieved at 5.9GHz as presented in Fig. 11.

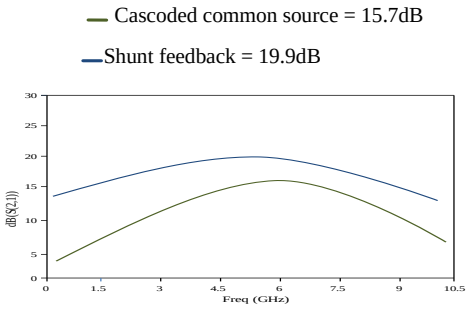

Figure 9. Power Gain

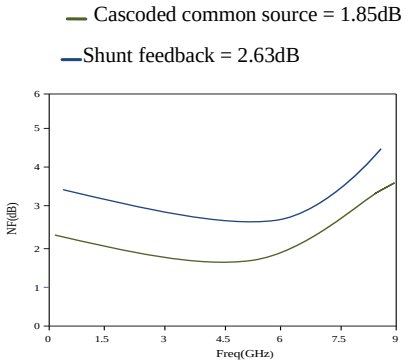

Figure 10. Noise Figure (NF)

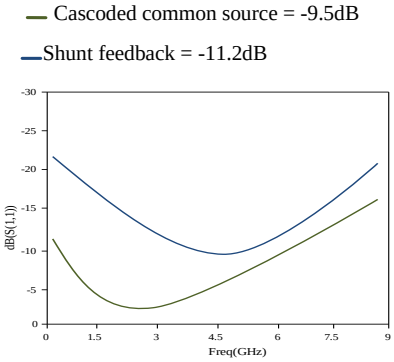

Figure 11. Input Matching (S_{11})

D. Output Matching (S22)

The output matching network does not change the DC bias of the active device. Since the low noise amplifiers are having very low output impedance, it is very easy to achieve the required output matching without any filter network at the output. The shunt feedback LNA has -22.8dB is achieved at 5.9 GHz is as shown in Fig. 12.

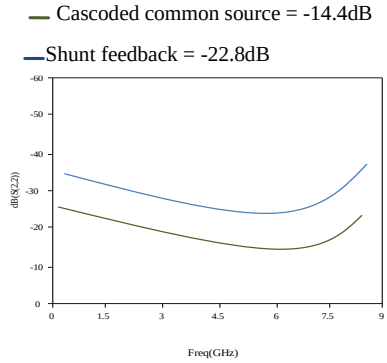

Figure 12. Output Matching (S_{22})

E. Reverse Isolation (S12)

The reverse isolation is very important parameter to ensure better stability. Since the cascode stage eliminates the Miller capacitance, it is chosen to provide better isolation. The shunt feedback LNA achieved the best reverse isolation with -32.5dB at the frequency of 5.9GHz as shown in Fig. 13

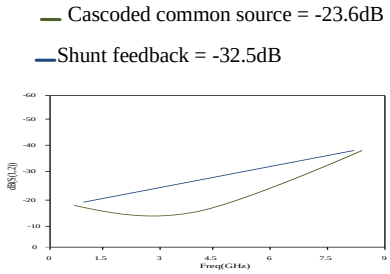

Figure 13. Reverse Isolation (S_{12})

F. Stability Factor (Stab Fact)

The stability of an amplifier is a very important consideration in a design of an LNA and can be determined from the S parameters, the matching networks, and the terminations [16]. The stability factor, `*K'* is calculated over the frequency band 5.725GHz to 5.925 GHz by using the equation (3).

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \qquad (3)$$

The plot of the stability factor is shown in Fig. 14. The two amplifiers are unconditionally stable with stability factor greater than 1 at the frequency of 5.9GHz.

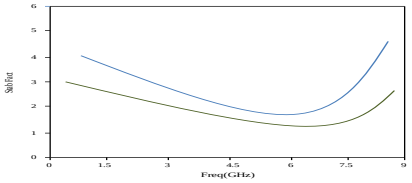

Figure 14. Stability Factor (Stab Fact)

G. Linearity (IIP3)

The amplifier's linearity was measured using the input referred third-order intercept point (IIP3). Fig. 15, Shows the linearity plots for the two amplifiers. The two amplifiers achieved the target IIP3 of -10 dBm. The improved linearity due to feedback gave the shunt feedback amplifier the best linearity among the two amplifiers with an IIP3 of - 5.07 dBm at the frequency of 5.9GHz.

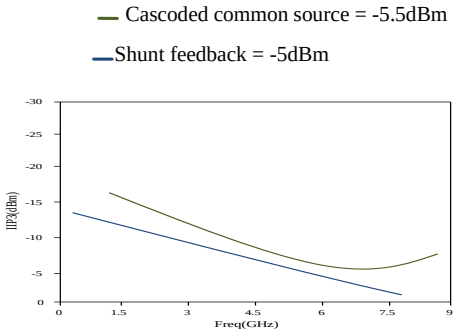

Figure 15. Input referred third-order intercept point (IIP3)

The Table III. Illustrates the summary of the simulation results for the LNA designs. The performance of the designed LNA is compared with the performance of the recently reported Low noise amplifiers.

TABLE III. Comparison of the low noise amplifier designs

Reference	Circuit Designs	V_{DD} [v]	f_c [GHz]	Gain [dB]	NF [dB]	P_{DC} [mW]	S11 [dB]	S22 [dB]	S12 [dB]	IIP3 [dBm]
This Work	Cascoded CS Amplifier	1	5.9	15.7	1.85	19.31	-9.5	-14.4	-23.6	-5.5
	Shunt Feedback Amplifier	1	5.9	19.9	2.63	56.8	-11.2	-22.8	-32.5	-5
[4]	Folded Cascode Amplifier	1	5.9	12.8	1.99	48.28	-12.3	-8.98	-25.9	-6.2
[11]	Current Reuse Amplifier	1.5	5	13	5.7	4.8	-10.3	-14.5	-45.8	-5.6
[12]	Distributive Amplifier	1.8	9	12.5	2.9	21.6	-12	-8	-25	-5.9
[12]	Common Gate Amplifier	1.8	10	15	4.4	12	-9	-12.4	-24	5.1
[12]	Differential Amplifier	1.4	5	12	5.2	22	-10.4	-14.7	-47.5	6.7

VI. CONCLUSION

In this paper, the designs of low-noise amplifiers are implemented for a WiMAX receiver. The amplifiers were implemented in a standard 180-nm CMOS process using 1V as supply voltage. The targeted operation frequency is in the range of 5.725 GHz to 5.925 GHz.

The cascoded common source achieved the lowest noise figure compared to other amplifier due to the noise optimization in the implementation of the input matching using inductive degeneration. The cascoded common-source also achieved the lowest power dissipation since it contains only one current branch. The low voltage operation capability of the cascode was offset by its high power consumption and further optimizations in the design are needed if it will be used in low-power applications. The shunt feedback amplifier achieved the highest gain, which is easily controlled by changing the value of the feedback resistor. The shunt feedback amplifier's highly linear performance makes its choice in the implementation of a wideband receiver. The shunt feedback amplifier has a slightly higher noise figure compared to the cascoded common source amplifier.

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