A Novel Design of an Efficient EMI Reduction Technique for SoC Applications

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Abstract- Electromagnetic interference (EMI), once the exclusive concern of equipment designers working with high-speed signals, is no longer limited to a narrow class of high-end applications. Continued innovation in semiconductor technology has resulted in the ready availability of cost-effective, high-performance system-on-chip (SoC) devices, microcontrollers (MCUs), processors, digital signal processors (DSPs), application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs) and analog/digital converters (ADCs). One of the most effective and efficient approaches to controlling and reducing EMI is to use spread spectrum clock generation (SSCG) technology e.t.c for better implementation of System on Chip , The proposed technique, a novel portable and all-digital spread spectrum clock generator (ADSSCG) suitable for system-on-chip (SoC) applications with low-power consumption is presented in this paper , Provide different EMI attenuation performance for various SoC applications.

Index Terms- All digital spread spectrum clock generator (ADSSCG), digitally controlled oscillator (DOC), low power, portable, triangular modulation.

I. INTRODUCTION

As the operating frequency of electronic systems increases, the electromagnetic interference (EMI) effect becomes a serious problem especially in consumer electronics, microprocessor (µp) based systems, and data transmission circuits [1]. The radiated emissions of system should be kept below an acceptable level to ensure the functionality and performance of system and adjacent devices [1], [2]. Many approaches have been proposed to reduce EMI, such as shielding box, skew rate control, and spread spectrum clock generator (SSCG). However, the SSCG has lower hardware cost as compared with other approaches. As a result, the SSCG becomes the most popular solution among EMI reduction techniques for system-on-chip (SoC) applications [2]–[4].

Recently, different architectural solutions have been developed to implement SSCG. In [4], [5], a triangular modulation scheme which modulates the control voltage of a voltage-controlled oscillator (VCO) is proposed to provide good performance in EMI reduction. However, it requires a large loop filter capacitor to pass modulated signal in the phase-locked loop (PLL), resulting in increasing chip area or requirement for an off-chip capacitor. Modulation on PLL loop divider is another important SSCG type that utilizes a fractional-N PLL with delta-sigma modulator to spread output frequency changing the divider ratio in PLL [6], [7]. However, fractional-N type SSCG not only needs large loop capacitor to filter the quantization noise from the divider, but also induces the stability issue for the wide frequency spreading ratio applications, especially in PC related applications [7].

The proposed ADSSCG employs a novel rescheduling division triangular modulation (RDTM) to enhance the phase tracking capability and provide wide programmable spreading ratio. The proposed low-power DCO with auto-adjust algorithm saves the power consumption while keeping delay monotonic characteristic. This paper is organized as follows. Section 2 describes the proposed architecture and spread spectrum algorithm of ADSSCG. Section 3 focuses on the low-power DCO design and the auto-adjust algorithm for monotonic delay characteristic. In Section 4, the implementation and measurement results of the fabricated ADSSCG chip are presented. Finally, the conclusion is addressed in Section 5.

II. PROPOSED ADSSCG DESIGN

Fig. 1 illustrates the architecture of the proposed ADSSCG. It consists of five major functional blocks: a phase/frequency detector (PFD), an ADSSCG controller, a DCO, and two frequency dividers. The ADSSCG controller consists of a modulation controller, a loop filter, and a DCO code generator (DCG). The ADSSCG can provide the clock signal with or without spread-spectrum function based on the operation mode signal (MODE) setting. In the normal operation mode, the bang-bang PFD detects the phase and frequency difference between FIN_M and DCO_N. When the loop filter receives LEAD from the PFD, the DCG adds a current search step (S_N [15:0]) to the DCO control code, and this decreases the output frequency of the DCO. Oppositely, when the loop filter receives LAG from the PFD, the DCG subtracts the DCO control code to increase the output frequency of the DCO. When PFD output changes from LEAD to LAG or vice versa, the loop filter sends the code-loading signal (LOAD) to DCG to load the baseline code (BASELINE CODE [17:0]) which is averaged DCO control code by the loop filter. Before ADSSCG enters the spread spectrum operation mode, the baseline frequency will be stored as the centre frequency. In the spread spectrum operation mode, the modulation controller uses two spreading control signals (SEC_SEL[2:0] and STEP[2:0]) to generate the add/subtract signal (6_SS) and the spreading step (S_SS[15:0]) for the DCG,

and then it modulates the DCO control code to spread out the DCO output frequency around the centre frequency evenly.

The system clock of ADSSCG controller is FIN_M whose operating frequency is limited by ADSSCG's closed-loop response time which is determined by the response time of the DCO, the delay time of the ADSSCG controller, and the frequency divider. Therefore, the period of FIN_M should not be shorter than the shortest response time to en-sure the ADSSCG functionality and performance. In addition, because the frequency of DCO_N should be the same as FIN_M after system locking, the frequency of FIN_M cannot be higher than the maximum frequency or lower than the minimum frequency of DCO_N. As a result, the frequency range of FIN_M is also limited by the DCO operating range and the divider ratio (N).

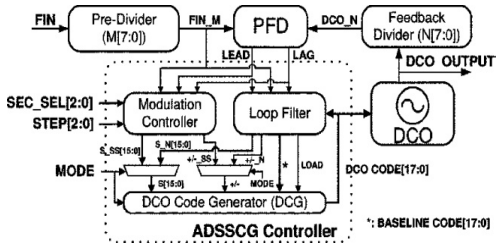

Fig. 1. Architecture of the proposed ADSSCG.

B. Spread Spectrum Algorithm

Since triangular modulation is easy to be implemented and has good performance in reduction of radiated emissions, it becomes the major modulation method for SSCG [2], [4]. In triangular modulation, the EMI attenuation depends on the frequency-spreading ratio and centre frequency, and it can be formulated as Where is the EMI attenuation, SR is the frequency spreading ratio, is the centre frequency, and are modulation parameters [3]. Based on (1), under the same centre frequency, EMI can be reduced further by increasing spreading ratio. In addition, under the same spreading ratio, the higher centre frequency has better EMI attenuation performance.

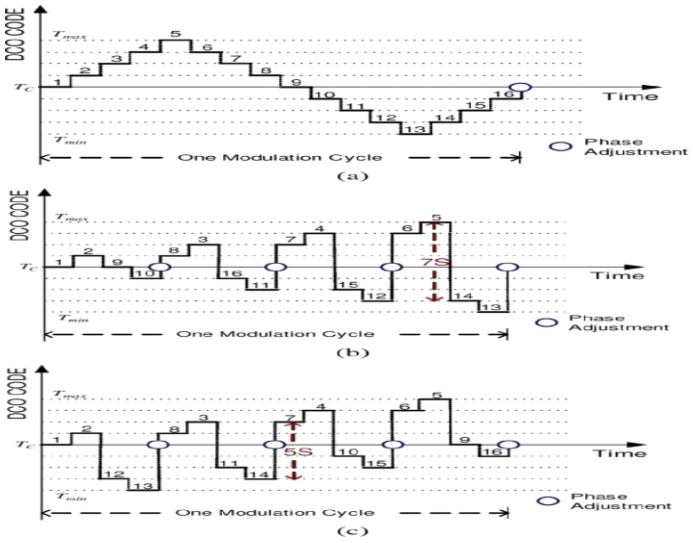

Fig. 2(a) illustrates the conventional triangular modulation with digital approach [9]. Since the output frequency can be changed by the DCO control code, the output clock frequency can be spread by tuning DCO control codes with triangular modulation within one modulation cycle. In the beginning of the conventional spread spectrum, it will start at centre frequency and take one-fourth of the modulation cycle time to reach the minimum frequency , and then takes half of the modulation cycle time to reach the maximum frequency. Finally, it will return to the centre frequency in the last one-fourth modulation cycle time. Because the upper half and lower half in the triangle have the same area, as shown in Fig. 2(a), the mean frequency of the spreading clock is equal to centre frequency and the phase drift will be zero in the end of each modulation cycle. However, in the conventional triangular modulation, the ADSSCG controller can only perform phase and frequency maintenance based on the PFD's output in the end of each modulation cycle. Hence due to the frequency error between reference clock and output clock, reference clock jitter and supply noise, the phase error will be accumulated within one modulation cycle, leading to induce the loss of lock and stability problems.

Thus, in order to enhance phase tracking ability, the division triangular modulation (DTM) is proposed as shown in Fig. 2(b). DTM divides one modulation cycle into many subsections (for example in Fig. 2(b), modulation cycle divides into 16 subsections) and updates DCO control code for phase tracking in every 4 subsections. As a result, the ADSSCG controller can perform four times phase and frequency maintenance in one modulation cycle when modulation cycle divides into 16 subsections. Because DTM can provide the frequency spreading function and keep phase tracking at the same time, it is very suitable for ADSSCG in µp-based system applications. However the disadvantage of DTM is when the frequency changes to different sub-sections; it will induce large DCO control code fluctuations (7 S) as shown in Fig. 2(b), where is the spreading step of DCO control code in spreading modulation.

In order to reduce the peak-to-peak value of DCO control code changing in DTM, the rescheduling DTM (RDTM) is proposed as shown in Fig. 2(c). By reordering the sub-sections in DTM, the peak-to-peak value of DCO control code changing can be reduced to 5 S. As a result, the peak-to-peak value of cycle-to-cycle jitter can be reduced while the period jitter is kept the same. Compared with DTM, the reduction ratio of peak-to-peak jitter by RDTM is related with number of subsection, and it can be formulated as

$$JR = \frac{((COUNT/2)-1)-((COUNT/4)+1)}{(COUNT/2-1)} \times 100$$

Where is the jitter reduction ratio, is the number of subsections. For example, if there are 16 subsections, the jitter reduction ratio is 29% ((7–5)/7), and if the number of subsection is 32, the jitter reduction ratio is 40% ((15–9)/15). Although the order of subsections of DTM is rescheduled by RDTM to reduce the peak cycle-to-cycle jitter, the average cycle-to-cycle jitter still keeps the same as DTM. Besides, because the phase drift of the opposite direction in DTM and RDTM remains the same, the equivalent phase drift is zero. As a result, it will not induce an extra phase drift while the mean frequency remains the same.

III. Digitally Controlled Oscillator

A. The Proposed DCO Architecture

Because DCO occupies over 50% power consumption in all digital clocking circuits, the proposed ADSSCG utilizes a low-power DCO structure to reduce overall power consumption [10]. To achieve the high portability of the proposed ADSSCG, all components in this ADSSCG including DCO are implemented with standard cells. Fig. 3(a) illustrates the architecture of the proposed low-power DCO which employs cascading structure for one coarse-tuning and three fine-tuning stages to achieve a fine frequency resolution and wide operation range. As the number of delay cell in the coarse-tuning stage increases, leading to have a longer propagation delay, the operating frequency of DCO becomes lower.

The shortest delay path that consists of one NAND gate, one path MUX of coarse-tuning stage at the minimum delay determines the highest operation frequency of DCO. There are 2^C different delay paths in the coarse-tuning stage and only one path is selected by the 2^C-to-1 path selector MUX which controlled by C-bit DCO control code. The coarse-tuning delay cell utilizes a two-input AND gate which can be disabled when the DCO operates at high frequency to save power. In order to increase the frequency resolution of DCO, the three fine-tuning stages which are controlled by F-bit DCO control code are added into the the DCO design. The first fine-tuning stage is composed of X hysteresis delay cells (HDC), and each of which contains one inverter and one tri-state inverter as shown in Fig. 3(b). When the tri-state inverter in HDC is enabled, the output signal of enabled tri-state inverter has the hysteresis phenomenon to increase delay [11]. Different digitally controlled varactors (DCVs) are exploited in the second and third fine-tuning stages to further improve the overall resolution of DCO as shown in Fig. 3(b).The operation concept of DCV is to control the gate capacitance of logic gate with enable signal state to adjust the delay time. The second and third fine-tuning stages employ Y long-delay DCV cells and Z short-delay DCV cells, respectively. Since the HDC can replace many DCV cells to obtain wider operation range, the number of delay cells connected with each driving buffer and loading capacitance can be reduced, leading to save power consumption and gate count as well.

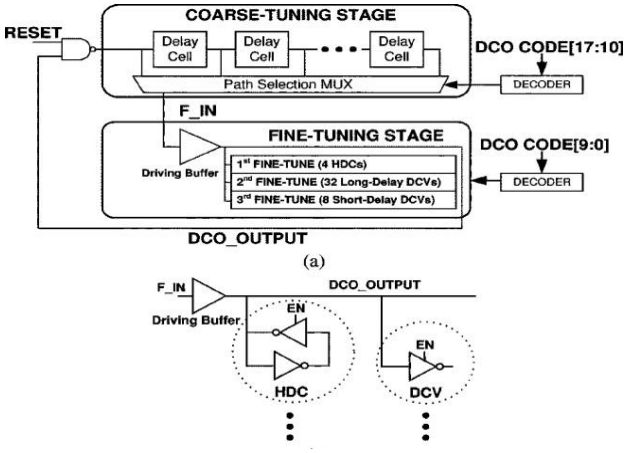

Fig. 3. Architecture of the proposed DCO

Based on an in-house μP-based system for liquid crystal display (LCD) controller applications [12], the requested operating frequency is from 27 to 54MHz. Thus the design parameters of the proposed DCO are determined as follows: *C=8,F=10,X=4,Y=32*, and *Z=8*. Table II shows controllable delay range and the finest delay step of di fferent tuning stages in the proposed DCO under typical case (typical corner, 1.8V,25^0 C). It should be noted that the controllable delay range of each stage is larger than the finest delay step of the previous stage. As a result, the cascading DCO structure does not have any dead zone later than the LSB resolution of DCO.Since the finest delay step of the third fine-tuning stage determines the overall resolution, the proposed DCO can achieve high resolution of 1.1 ps.

IV. Software Results

By using the Xilinx 13.1 and modelsim 6.5b interference estimated and, The following figures shows the result of Interference reduction technique, The following Fig 4 shows the estimating phase error of the applied clock signal and on chip clock signal

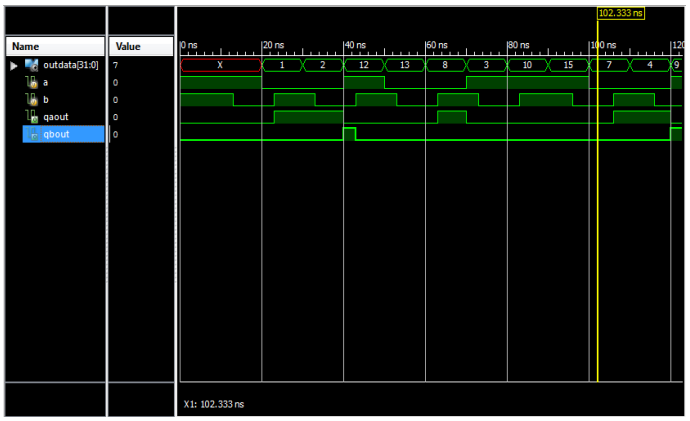

Fig 4. Estimating phase error

The following Fig 5 shows the phase error of the applied clock signal and on chip clock signal and different modes of operation

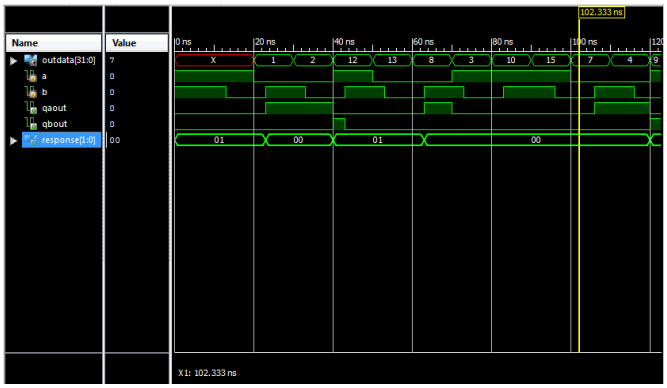

Fig 5. Estimating phase error with different modes

The following Fig 6 shows the phase error correction of the applied clock signal and on chip clock signal and different modes of operation

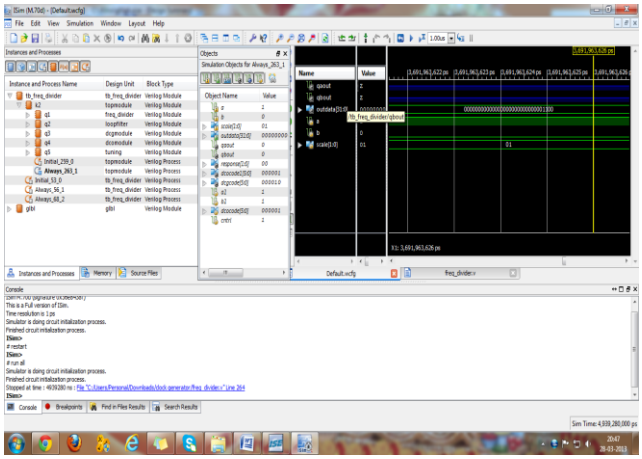

Fig 6. The phase error correction

The following figure Fig 7 shows the power estimation of low power interference technique.

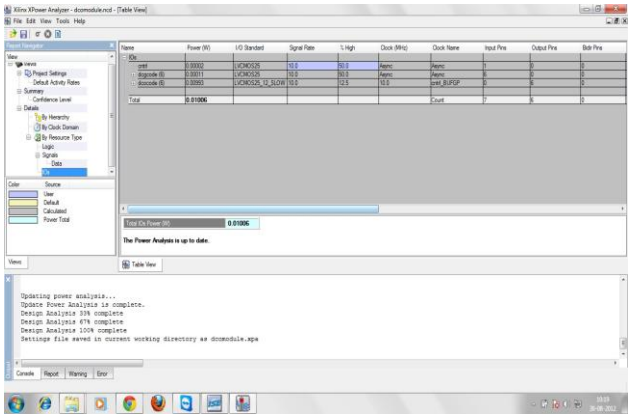

Fig 7. The power estimation of low power interference technique

The following Fig.8 shows the layout of the DCO which is used for the, To minimize the noise coupling from the digital blocks to the DCO core, they have some physical distance as shown in Fig. 10. In addition, putting guard rings and substrate contacts is done carefully.

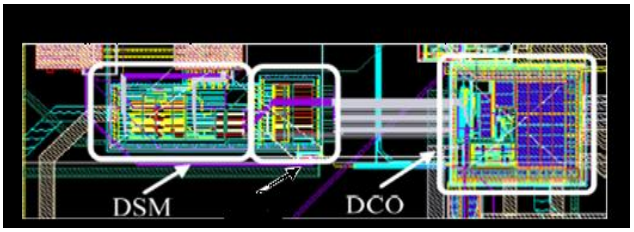

Fig.8 The layout of the DCO

The following Fig.9 shows the various comparison results

Performance Parameter	Proposed	[10]	[2]	[8]	[6]	[9]
Process	0.13μm CMOS	0.13μm CMOS	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS
Operation range (MHz)	98 ~ 599	150	152 ~ 366	18 ~ 214	413 ~ 485	140 ~ 1030
LSB resolution (ps)	0.93	40	10 ~ 150	1.55	2	22
Power consumption	110μW (@200MHz)	1mW (@150MHz)	NA	18mW (@200MHz)	170 ~ 340 μW (Static only)	NA
Portability	Yes	No	Yes	Yes	No	Yes

Fig.9. Comparison of various methods

V. Conclusion

In this paper, we proposed a portable, low power, and area-efficient ADSSCG with programmable spreading ratio for SoC applications. Based on the proposed RDTM, the spreading ratio can be specified flexibly by application demands while keeping the phase tracking capability. With the proposed low-power DCO, the overall power consumption can be saved. The proposed auto-adjust algorithm can maintain the monotonic characteristic of DCO. Measurement results show the proposed ADSSCG can achieve 9.5 dB EMI reductions with 1% frequency-spreading ratio and 1.2 mW frequency of 54 MHz As a result, our proposal achieves less power consumption and area with competitive EMI reduction. Moreover, because the proposed ADSSCG has a good portability as a soft intellectual property (IP), it is very suitable for SoC applications as well as system-level integration.

VI. Future Scope

The proposed ADSSCG employs a novel rescheduling division triangular modulation (RDTM) to enhance the phase tracking capability and provide wide programmable spreading ratio. The proposed low-power DCO with auto-adjust algorithm saves the power consumption while keeping delay monotonic characteristic. So in future all the analog spread spectrum clock generators may be replaced by digital clock generators by using ADSSCG. So in future the EMI reduction is almost achieved thoroughly and this can be further improved by still lowering the power of the digital circuits.

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