An Improved VCO Design with Negative Feedback to Reduce Jitter at High Frequencies

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Abstract - This paper presents an improved design of voltage controlled oscillator (VCO) utilizing the three differential cell CMOS inverters for forming the ring oscillator. The differential cell reduces the power supply fluctuations impact on the oscillator jitter while the negative feedback from frequency to voltage converter reduces the jitter at high frequencies. Finally the proposed model is designed using CMOS 0.18μm foundry technology and simulated using P-Spice software. The result shows that the proposed design improves the jitter attenuation at different offset frequencies up to 40dB.

Index Terms - Phase Locked Loop (PLL), Voltage Controlled Oscillator (VCO), Ring Oscillator, Jitter, Phase Noise.

I. INTRODUCTION

A CMOS ring voltage controlled oscillator was initially used for clock recovery in Ethernet controllers. Since then, the ring oscillator has become a widely used component in communication system. In this role, the ring oscillator is still the most widely produced of all oscillators as compared to alternatives such as LC resonator-based oscillators. Since the ring oscillator is exceptionally compact hence a large number of ring oscillators can be designed with the same chip area as a small spiral inductor also it can oscillate at very high frequencies, (very short periods limited only by gate delays), which is far greater than maximum oscillation frequency of RC phase shift oscillators. Furthermore the ring oscillator provides a large frequency tuning range. One of the major application area of ring oscillators is PLL. The Phase locked loop (PLL) is a critical component in many high speed communication systems because it provides the basis for time functions such as clock control, data recovery, and synchronization. Looking inside of a PLL the Voltage-controlled-oscillator (VCO), is the most important element of the PLL, which can be built by Ring structures, relaxation schemes, or LC resonant circuit. LC design has the best noise and frequency performance with a good quality factor Q of the resonant networks. However, adding high-quality inductors to CMOS design increases the cost and complexity of the chip, it also introduces problems such as eddy currents. Ring oscillators, on the other hand, can be built in any standard CMOS process may require less space die LC drawings. The design is simple, and ring architectures can be used to produce multiple output stages and wide tuning ranges. However, the ring oscillator usually shows poorer phase-noise performance than the LC-tank oscillator because of its low effective quality factor. The time jitter in a normal periodic signal can be considered as fluctuations inphase at the discrete set of zero-crossing instant. The fluctuations are caused by the phase noise of an oscillator, which is defined as continuously evolving stochastic process. The jitter can arise from many reasons such as unwanted injection of signals from other parts of circuits, inherent thermal noise etc.

In this brief, we present an improved design of CMOS ring oscillators design controlled by a frequency to voltage converter through negative feedback and implemented prototypes circles implemented in TSMC CMOS 0.18μm foundry technology which shows the excellent jitter reduction. In rest of the paper the section II presents the functional overview of ring oscillators followed by section III which explains the phase noise and jitter in CMOS ring oscillators. The Section IV presents the proposed design and functionality while Vth section simulation results are presented and finally section VI the conclusion on the basis of simulated results are derived.

II. RING OSCILLATOR

A ring oscillator consisting of a number of delay stages in a loop, which constitutes a negative unstable feedback loop. The period of oscillation is twice the sum of the delay of each delay cell in the ring. Figure 1 shows the linear model of a three-stage ring oscillator. The open loop transfer function of this model is:

\[ H_{jω} = \frac{-g_m R}{1 + RjωC} \]

Where \( g_m \) is the gain of each delay stage of the signal, \( R \) and \( C \) are the load resistance and capacitance at the output of each delay stage. The circuit oscillates only if the frequency dependent phase shift equal to 180 degrees which means, if each phase contributes 60 degrees. The frequency at which this occurs is given by:

\[ \tan^{-1} \frac{180}{ω_{osc} RC} = 60° \]

Hence

\[ ω_{osc} = \frac{\sqrt{3}}{RC} \]

The minimum voltage gain per stage must be such that the magnitude of the loop gain at \( ω_{osc} \) is equal to unity.

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The minimum number of stages of a ring oscillator is 3, because for rings 1 or 2 stages does not provide phase shift sufficient for oscillation. The frequency of oscillation is usually controlled by varying the bias current of the delay cell. However, since ring oscillators do not have high-Q tank for the selection of frequency, have traditionally much more phase noise of oscillators based LC-tank.

2.1 VCOs based on differential ring oscillator
Presently almost all mixed signal ICs use ring oscillators stages of differential delay because of their higher immunity to interference power and the noise substrate. A phase differential delay with the conventional bias circuit replication is shown in Figure 2. The frequency of oscillation of a N-stage differential ring oscillator can be expressed as:

\[ f_0 = \frac{1}{2N \tau_d} \approx \frac{I_{bias}}{NC_V} \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots
\[ t_d = \frac{C_1 V_{op} \ln 2}{I_b} = R_2 C_2 \ln 2 \ldots \ldots \ldots \ldots (11) \]

Figure 3: A typical differential delay stage in ring oscillators.

\[ f_o = \frac{1}{2 M t_d} \ldots \ldots \ldots \ldots (12) \]

The differential pair has an input transition range of:

\[ V_{id} = \pm \sqrt{2V_{eff}} \ldots \ldots \ldots \ldots (13) \]

over which it steers the tail current. \( V_{id} \) is the input differential voltage, and \( V_{eff} \) is the effective gate voltage on the differential pair at balance.

Since the differential inverter already suppresses the phase noise due to power supply fluctuations and flickers the phase noise in such systems is only caused by the jitter at the moment of the zero crossing of the output differential voltage or by the fluctuations in voltage of the zero crossing moment (also called Phase Noise Due to White Noise). The SSB phase noise due to white noise in the differential ring oscillator is defined by:

\[ L(f) = \frac{2kT}{I_b \ln 2} \left[ \gamma \left( \frac{3}{4V_{effd}} + \frac{1}{V_{effb}} \right) + \frac{1}{V_{op}} \left( \frac{r}{f} \right) \right]^2 \ldots \ldots (14) \]

where \( V_{effd} \) is the effective gate voltage of the differential pair at balance, \( g_{mb} \) is the small signal transconductance of the tail transistor.

Now according to equation 14 the following conclusions can be drawn for the phase noise.
1. The phase noise is independent of the number of delay stages, and only depends on the frequency of oscillation \( f_o \). Thus, the phase noise is equal in two rings which oscillate at the same frequency, where one ring comprises a few stages loaded heavily while the other ring comprises more lightly loaded stages.
2. The only technology-dependent parameters are \( V_e \) and \( \gamma \).

IV. PROPOSED WORK

The block diagram of the proposed design is shown in figure 3, as it shows that design consists of a negative feedback block in between the output and input of the VCO. The importance of the circuit can be explained by analyzing the behaviour of ring oscillator for phase noise and jitter. Since the phase noise of the ring oscillator increases with the frequency of oscillation. The phase noise in caused by fluctuations in the instants when the output ramp in a delay element crosses the toggle point.

Figure 4: Block Diagram of Proposed Model

Figure 5: Jitter in a VCO using Differential Ring Oscillators can be modeled as High Pass Filter, and if another High Pass Filter is used with Negative feedback it can convert the VCO jitter transfer function to Low Pass Filter and can reduce the Jitter at higher frequencies.

In the proposed work the High Pass Filter for the feedback loop is designed by voltage to frequency converter (VFO), which generates the output voltage in proportion to the output frequency of VCO.

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V. SIMULATION RESULTS

The Proposed ring-oscillator-based VCO has fabricated in 0.18um CMOS technology. Since the design does not contain any capacitors hence implementation does not require MOS capacitance. A layout of the fabricated VCO is shown in Fig. 7. Which requires the core area of 100umX50um. The active area is approximately equal to 0.19 mm^2. The prototype has been tested for oscillation frequency of 1 GHz. The measured output spectrum of the VCO is shown in Fig. 8, which presents maximum amplitude at the 1 GHz. Figure 8 also shows the phase noise of the prototype. Using the Phase Noise Calculation as mentioned in (9) and converting it for voltage:

\[
L_{\text{total}}(\Delta \omega) = 20 \log \left( \frac{V_{\text{sideband}}(\omega + \Delta \omega, 1\text{Hz})}{V_{\text{carrier}}} \right) \quad \text{(15)}
\]

\[
L(f) = \left( \frac{V_{\text{sideband}}(f + \Delta f, 1\text{Hz})}{V_{\text{carrier}}} \right)^2 \quad \text{(16)}
\]

\[
\text{RMS Phase Noise} = s(f) = \frac{180}{\pi} \sqrt{2 \int L(f) \, df} \quad \text{(17)}
\]

\[
\text{RMS Jitter} = J_{\text{RMS}} = \frac{s(f)}{2\pi f} \quad \text{(18)}
\]

\[
L_{\text{RMS}}(1 \text{MHz}) = 20 \log \left( \frac{10^{-9}}{1} \right) = -180 \text{dBc/Hz}
\]

\[
s(1 \text{MHz}) = \frac{180}{\pi} \left( 10^{-6} \sqrt{2} \right) = 8.103 \times 10^{-5}
\]

\[
J_{\text{RMS}} = \frac{8.103 \times 10^{-5}}{2 \pi \times 10^{9}} = 0.0139 \text{ps}
\]

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the phase noise is –180 dBc/Hz at 1MHz offset from the 1.0 GHz carrier and the jitter performance of the VCO for same offset is 0.0139 ps RMS.

![FFT of output waveform from Proposed VCO](image)

**Figure 8:** the FFT of the output waveform from Proposed VCO.

The power consumption of the proposed design is 1.3mW which is also considerably low.

![Generated output waveform (1 GHz)](image)

**Figure 9:** the Generated output waveform (1 GHz)

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VI. CONCLUSION

This paper presents a negative feedback controller VCO architecture aimed to reduce jitter noise, especially for a VCO working at higher frequencies. Firstly, Phase noise due to power supply fluctuations is inherently improved by differential ring oscillator secondly the use of VFC at feedback loop enhance noise rejection. A wide operating frequency range over all PVT is obtained by using a dual-delay path scheme and digital calibration techniques in the VCO. Experimental results demonstrate that the proposed PLL is a good solution to improve noise rejection.

REFERENCES


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