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Crosstalk Analysis between the bitlines of dualport SRAM

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Abstract- Crosstalk in VLSI interconnects is a major constraint in DSM and UDSM technology. Among various strategies followed for its minimization, shield insertion between aggressor and victim lines is one of the most prominent options. Placing shields around a victim signal line is a common way to enhance signal integrity while minimizing delay uncertainty. This paper analyzes the extent of crosstalk in capacitive coupled interconnects and minimizes the same through shield insertion. Also design guidelines for shielding in the presence of power/ground (P/G) noise are illustrated in this paper. The effects of P/G noise on crosstalk is analyzed for different line lengths, line widths, and interconnect driver resistances. Considering the P/G noise, a shield line can degrade the signal integrity due to increased P/G noise coupling on the victim line. A *RC* interconnect model is used to investigate the effects of coupling capacitance on the crosstalk noise. Physical spacing and shield insertion are compared in terms of the delay on the victim line for several technology parameters.

Dual port SRAM cells contain a second set of access transistors designed to allow a second read from the cell. As device sizes shrink, the spacing between conductors is reduced to the point where crosstalk between second pair of access runners within the same cell area of a dual port device becomes a significant design issue. Techniques for reducing capacitive coupling between these access lines are considered here. Additionally, the effects of technology scaling on P/G noise and shielding efficiency between bit lines are discussed, and related design tradeoffs are addressed. Design tools used to build circuit schematic is Cadence Virtuoso Design Platform, HSpice Simulator for simulation of schematics and CosmosScope (CScope) for observing the waveforms.

Index Terms- Capacitive coupling, Crosstalk, Interconnects, Power/Ground noise, SRAM.

I. INTRODUCTION

In deep sub micrometer integrated circuits, crosstalk between adjacent interconnect lines has become a primary design issue. With aggressive technology scaling, the local interconnect has become more resistive and capacitive. Capacitive coupling has therefore become a significant design issue in local interconnect.

As VLSI technologies scale down, interconnect performance is greatly affected by crosstalk noise due to the decreasing wire separation and increased wire aspect ratio, and P/G noise on crosstalk has become a major bottleneck for design closure. Although P/G noise has received significant attention in the design of robust power distribution networks, the deleterious effects of P/G noise on shielding methodologies is usually neglected. Here, the effects of P/G noise on crosstalk is analyzed for different line lengths, line widths and interconnect driver resistance, to provide practical and more effective shielding methodologies. Comparisons between physical spacing and shield insertion techniques are provided. Boundary conditions are also identified to determine the efficacy regions of spacing and shield insertion.

II. SRAM

SRAM is used in cache memory because it is fast to access and can be accessed in a dual ported manner. There are certain factors that have to be considered before selecting a RAM for system design. These design tradeoffs are density, speed, volatility, cost, and features.

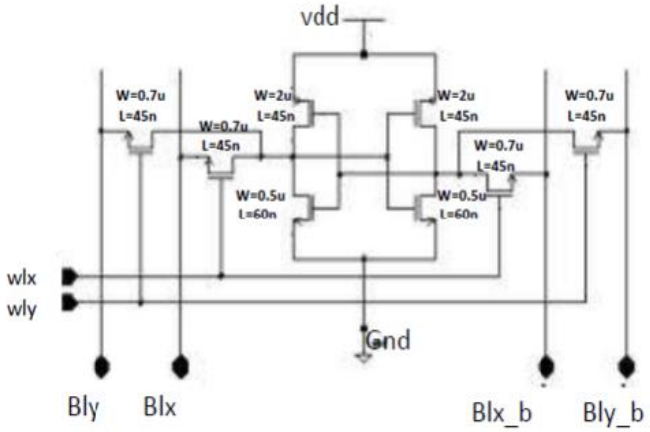
The conventional six-transistor (6T) SRAM is built up of two cross-coupled inverters and two access transistors, connecting the cell to the bit lines. The inverters makeup the storage element and the access transistors are used to communicate with the outside. The cell is symmetrical and has a relatively large area. No special process steps are needed and it is fully compatible with standard CMOS processes.

A. Dualport SRAM

Dual port SRAM cells are fundamentally different from conventional SRAM devices in that they contain a second set of access devices designed to allow a second read or write (or both) path into the cell. The cells are typically planar with all active devices located on the same level of the silicon substrate. This requires that at least a portion of all interconnections for each cell to occupy a common interconnection level. As device sizes shrink, the spacing between conductors is reduced to the point where crosstalk between runners becomes a significant design issue.

In the usual dual port SRAM, the second pair access lines are bit lines. The interconnection layout for this cell is asymmetric with essentially four bit lines per cell and two read lines. To maintain minimum cell size with a given design rule, the four bit lines will generally be the most closely spaced. The word lines are more widely spaced, usually sufficient to avoid undue capacitive interaction. However, from an electrical standpoint, this spacing is the opposite of that desired, since the word line voltage swings are both large, while the read bit lines voltages are relatively small. Thus the lines most susceptible to unwanted capacitive

coupling are read bit lines closely spaced to another line, usually a write bit line.



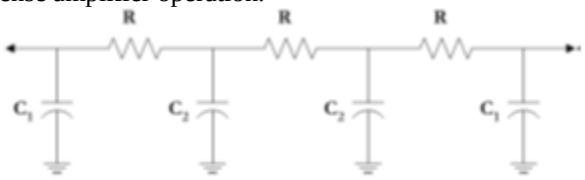
B. Coupling noise in SRAM

Crosstalk is any phenomenon by which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel.

The increased integration density raises the noise level due to inter-signal coupling (capacitive crosstalk) and it can be of two types.

- Bit line-to-bit line coupling
- P/G noise to bit line coupling

This problem is aggravated in dual port devices which have at least one second pair of access runners within the same cell area. The bit lines of dual port SRAM are modeled as a capacitive – resistive (RC) model. Bit line capacitive coupling causes small coupling voltages on adjacent bit lines, which influences proper sense amplifier operation.



C. Crosstalk noise reduction techniques

Several techniques can be used to mitigate the effects of crosstalk noise in high complexity integrated circuits. Increasing the physical distance between the aggressor and victim lines can reduce the coupling capacitance and resistance between adjacent lines. The reduction in crosstalk capacitance is approximately inversely proportional with the increase in spacing. The resistance, however, is not significantly reduced with increasing distance since the resistance is not a long range phenomenon. To reduce the resistance, additional return paths should be provided for the current to flow.

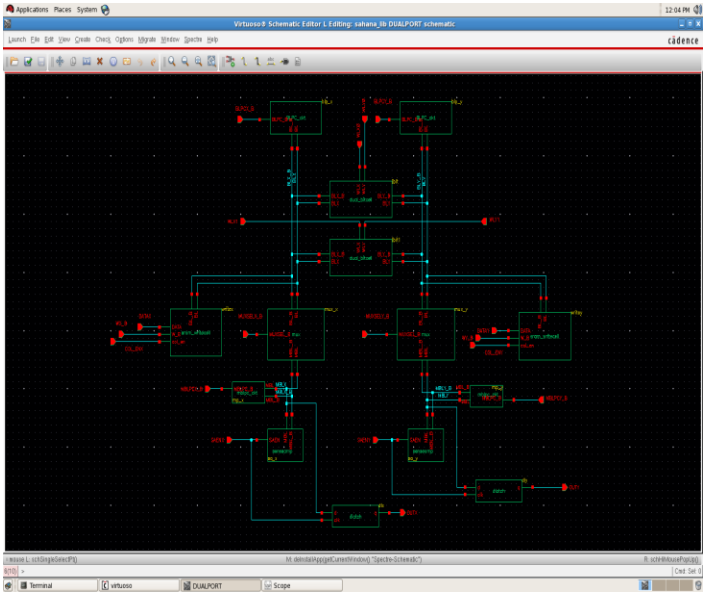
Inserting shield lines between the aggressor and victim lines reduces the capacitive and resistive coupling between adjacent blocks. Shield insertion significantly reduces capacitive coupling between the aggressor and victim lines because capacitive coupling is a short range phenomenon and is significantly reduced in non-adjacent lines. Shield insertion moderately reduces the resistance due to the current return path formed by the inserted shield line for both the aggressor and victim lines. The difficulty in forcing the current return path complicates the inductive shielding process.

Active shielding is another shielding technique in which the shield line switches depending upon the switching pattern of the adjacent bus lines. Capacitive (inductive) coupling is reduced with active shielding when the shield line is switched in the same (opposite) direction as the signal line. The switching activity of the shield lines should therefore be tuned to the switching pattern which is different for non-dominated and dominated interconnects lines. The primary drawback of active shielding is increased power consumption and additional area of the logic circuitry controlling the active shield lines. Furthermore, process and environmental variations may unexpectedly affect the signal arrival times, degrading the efficiency of active shielding.

Sizing the buffer driving the aggressor and victim lines is another technique to reduce crosstalk noise. The effective conductance of the driver increases with larger drivers. For the victim line, a larger driver can be used to maintain the victim line at a constant voltage by increasing the driver conductance. For the aggressor line, using a smaller driver decreases the crosstalk noise since the signal transition is slower due to the increased time constant, decreasing the induced noise on the victim line. Proper sizing of the driver on the aggressor and victim lines can therefore produce lower crosstalk noise. This technique is however subject to delay constraints since a smaller driver increases the gate delay. Wire sizing can also be used to modify the line resistance, coupling capacitance, line-to-substrate capacitance, and self-inductance.

III. IMPLEMENTATION

The implementation was done for a dual-port 128X4 SRAM array. Each SRAM cell is a combination of precharge circuit, 8T-SRAM bitcell and a sense amplifier. This array is accessed with the help of a multiplexer. The bit lines and the shield lines are modeled using RC-model considering the resistance of each line and the capacitance between the lines. Since the mutual inductance is almost nil for very small separation, RC model is considered instead of RLC. The measurements were taken for different widths, sizes and lengths of bitlines and shieldlines.



IV. ANALYSIS

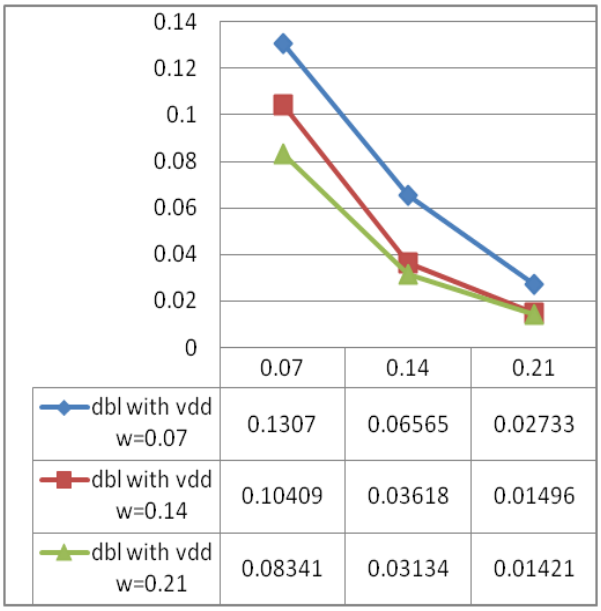
The resistance and capacitance (i.e. ground capacitance and bit line coupling capacitance) – RC parameters change for different

spacing between the bitlines and different widths of the bitlines is listed in the below table.

Space (µm)	Width (µm)	Resistance (Ω)	c gnd (fF)	c bit (fF)
	0.07	387.58	8.42	15.16
0.07	0.14	166.1	12.66	14.42
	0.21	154.93	17.04	14.58
	0.07	237.27	12.06	9.2
0.14	0.14	157.95	15.67	6.46
	0.21	100.78	20	6.44
	0.07	210.29	14.70	4.97
0.21	0.14	154.93	17.68	3.33
	0.21	100.78	22	3.31

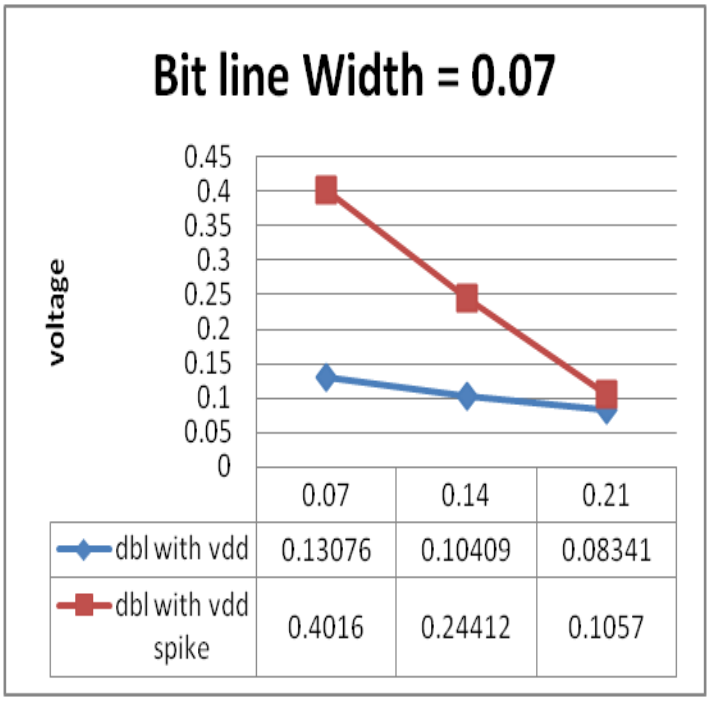
A. Crosstalk noise comparison with and without shielding

Shield insertion and physical spacing between adjacent interconnect are evaluated for several bit line widths and separation between the aggressor and victim. A comparison of shield insertion and physical spacing for different widths is illustrated in the figures below for a constant line length of 100um. Note that the distance between the aggressor and victim lines remains the same for both the physical spacing and shield insertion methods.



B. Crosstalk noise comparison with and without p/g noise in V_{DD} line

For the 45nm technology that we are using, P/G noise becomes a significant design issue. The P/G network has become more resistive, increasing the noise within the P/G distribution network, with technology scaling. Additionally, with supply voltage scaling, the noise of the P/G network is more significant. P/G noise is the dominant source of crosstalk noise when the noise is greater than 10% of the supply voltage. Coupling from the aggressor to the victim is the dominant noise source when the P/G noise is less than 2%of the supply voltage. The P/G noise on the shield line reduces the efficiency of shielding because this noise also couples to the victim lines.



V. CONCLUSION

In this paper on *Crosstalk Analysis between the Bitlines of Dualport Sram*, we have given a comprehensive analysis of crosstalk noise with and without shielding and also the effect of shielding line noise have been studied. It can be inferred from the analysis that shielding is preferable for smaller driver resistance and physical spacing is preferable for higher driver resistance of the bit lines. Also shielding is more efficient when the coupling capacitance of the bit lines is higher and wider. We can also see that coupling from the aggressor to victim is dominant source of noise when the P/G noise is absent. The P/G noise is dominant source of crosstalk noise when the noise is greater than 10% of supply voltage. The analysis gives the comparisons for making a optimal trade-off between lower power and noise immunity by using a combination of spacing/shielding depending on the extent of coupling.

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