Low-Power and High Speed Carry Select Adder

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Abstract- Adders are the basic building blocks of any processor or data path application. In adder design carry generation is the critical path. To reduce the power consumption of data path we need to reduce number of transistors of the adder. Carry Select Adder is one of the fast adder used in many data path applications. There is a chance to reduce the area, power and delay in the CSLA structure. The proposed design is implemented by using D-latch instead of using RCA cascade structure for Cin=0 or Cin=1. In this proposed design power and delay is reduced to 10.8% and 4.6% for 8bit, 17.73% and 49.3% for 16bit, 20% and 44.5% for 32bit, 21.9% and 59.8% for 64bit when compared to the Regular Carry Select Adder (CSLA). Power and delay is reduced to 4.43% and 37.23% for 8bit, 12.37% and 37.8% for 16bit, 14.06% and 45.68% for 32bit, 14.43% and 50.57% for 64bit when compared to the modified CSL adders (BEC). The delay is reduced 37.24% for 8bit, 60.4% for 16bit, 61.6% for 32bit, 14.43% and 56.74% for 64bit when compared to the modified CSL adder (WITHOUT USING MULTIPLEXER).

Index Terms- CSLA, D-Latch, BEC, LOW POWER AND HIGH SPEED.

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use D-Latch instead of RCA with Cin = 0 or cin = 1 anyone in the regular CSLA to achieve High speed, lower area and power consumption [2]–[4]. The main advantage of this D-Latch logic comes from High Speed than the n-bit Full Adder (FA) structure. The details of the D-Latch logic are discussed in Section VI. This brief is structured as follows. The SQRT CSLA has been developed by using D-latch and compared with regular SQRT CSLA and ref[4-5].

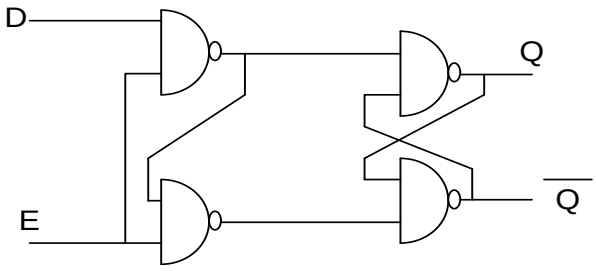


Fig.1D-Latch

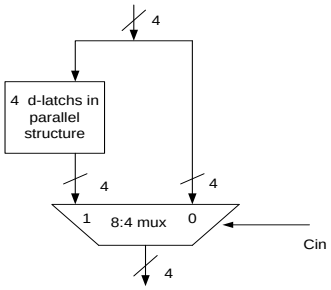


Fig.2 4-bit D-Latch with multiplexer.

Fig.1 shows the internal structure of D-Latch when D-Latch en=1 the input to the d-latch pass transistor should be D and when en=0 the input to the pass transistor should be value of D just before the transition of clock from 1 to 0.To obtain the value of D just before transition a buffer is needed.

Fig.2 shows the internal structure of 4-bit D-Latch circuit. When en=1 then the RCA structure will calculate the output for cin=1 and that will be stored in D-Latch. When en=0 then the RCA structure will calculate the output for cin=0 and the D-Latch out will not change that will stores previous value of RCA when en=1. And that D-latch, RCA structure outputs are given to the multiplexer by using selection line(cin) it will gives the proper output.

II. LITERATURE REVIEW

Bedriji 1962 proposes that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums.

AkhilashTyagi 1993 introduces a scheme to generate carry bits with block carryin 1 from the carries of a block with block carryin 0.

Chang and Hsiao 1998 propose that instead of using dual carry ripple adder a carry select adder scheme using an add one circuit to replace one carry ripple adder.

Youngwood Kim and Lee Sup Kim 2001 introduces a multiplexer based add one circuit is proposed to reduce the area with negligible speed penalty.

Yajuan He et al 2005 proposed an area efficient square root carry select adder scheme based on a new first zero detection logic.

Ramkumar and Harish 2012 propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

Sajesh Kumar U, Mohamed Salih K. and Sajith K 2012 propose carry select adder without using multiplexer which reduce area and power consumption.

III. REGULAR 16-B SQRT CSLA

CSLA compromise between ripple carry adder and carry look ahead adder. When compared to RCA CSLA is high speed and when compared to carry look ahead adder hardware complexity less. The main disadvantage of regular CSLA is the large area due to the multiple pairs of ripple carry adder. The Fig.5 shows the regular 16-bit carry select adder. It is divided into five groups with different bit size RCA. From the structure of CSLA, it is evident that there is scope for reducing area, power and delay in CSLA.

The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer. Internal structure of the group 2 to 5 of regular 16-bit CSLA is shown Fig.3. One input to the multiplexer goes from the RCA with Cin=0 and other input from the RCA with Cin=1.

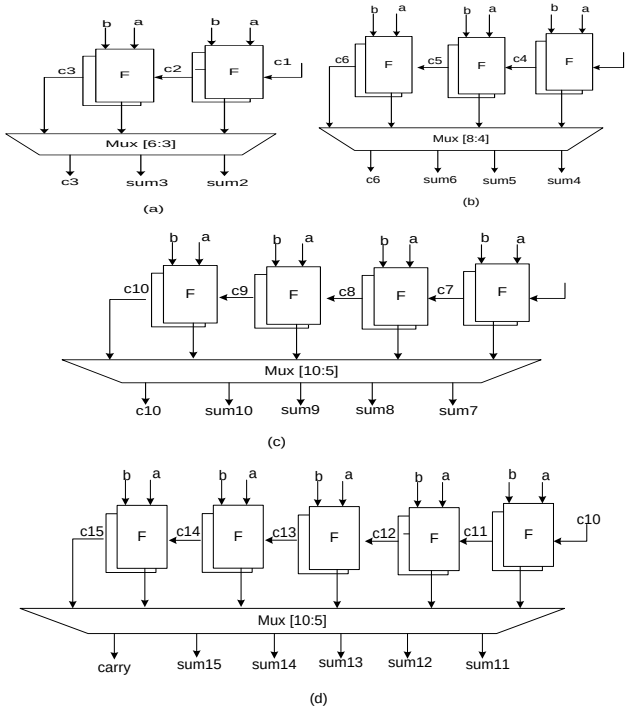


Fig .3 internal structure of Regular CSLA group A to D

There is a chance to reduce the area, power and delay in the CSLA structure.

IV. MODIFIED 16-B SQRT CSLA (BEC)

The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The modified16-bit CSLA using BEC is shown in Fig.6 [4]. The structure is again divided into five groups with different bit size RCA and BEC. The group 2 to 5 of the modified 16-bit CSLA is shown Fig. 4.

One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 to 5 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power.

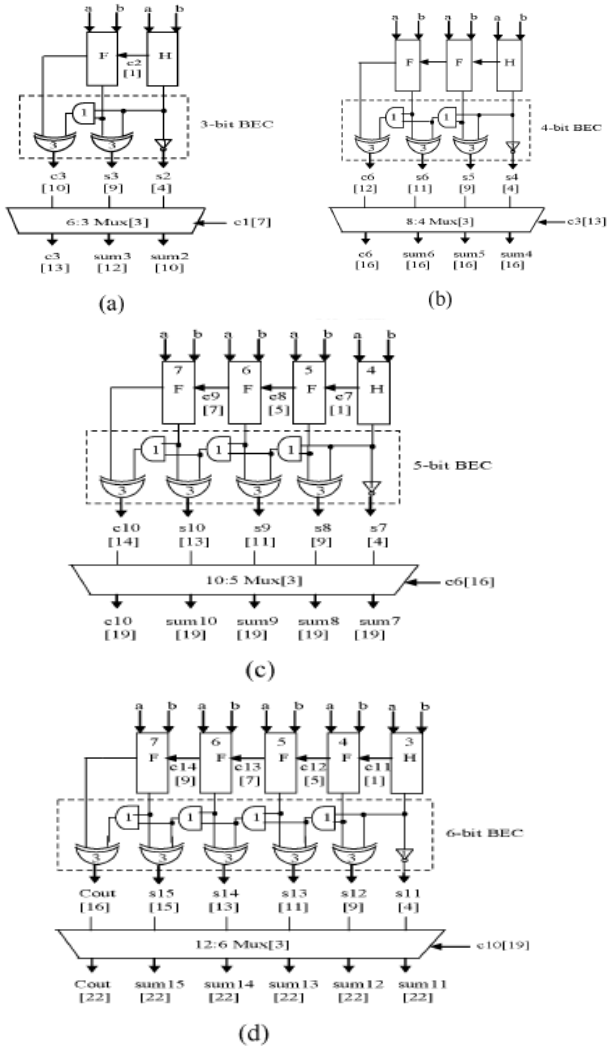


Fig.4 internal structure of Modified CSLA(BEC) group A to D

But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.

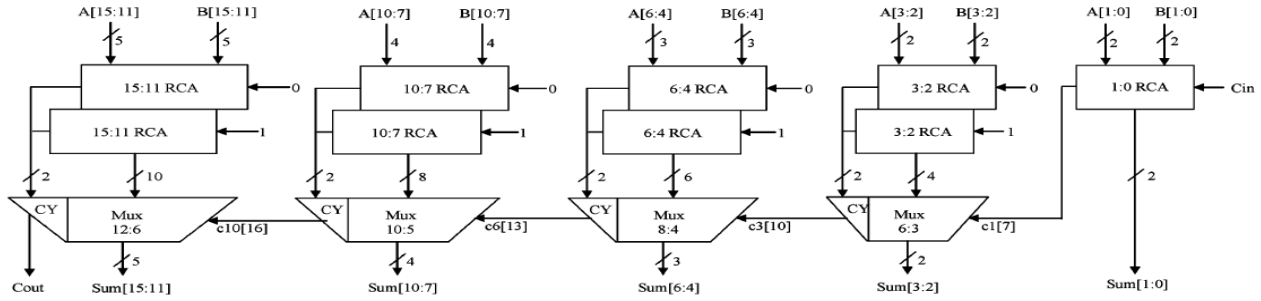


Fig .5 16bit regular CSA

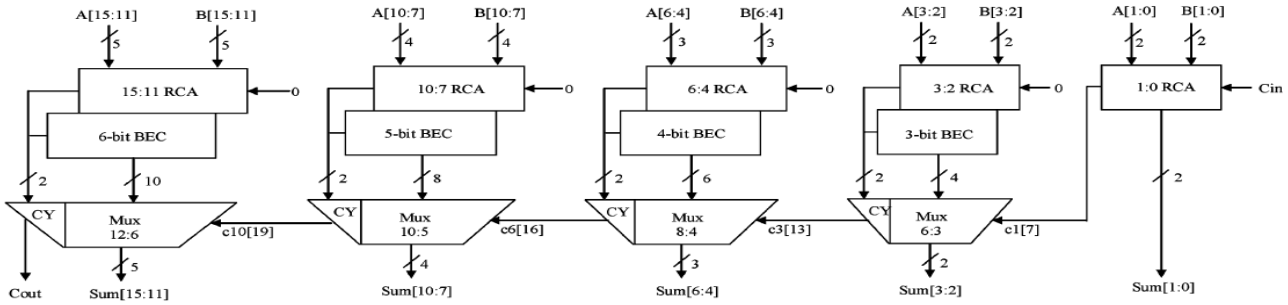


Fig.6 CSLA by using BEC [4]

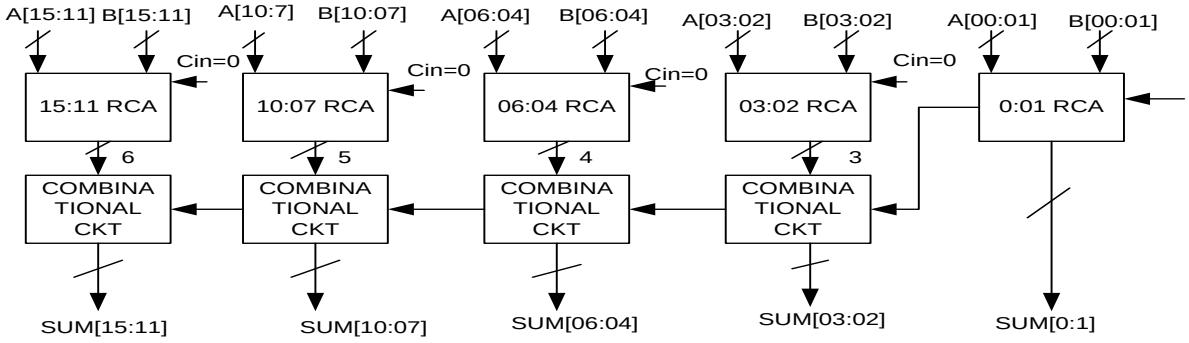
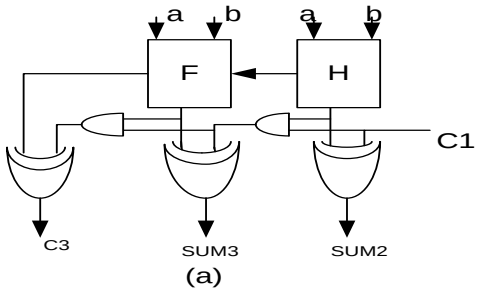


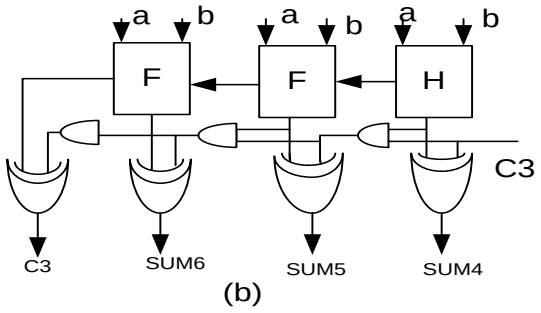
Fig .7 CSLA without using multiplexer [5]

V. MODIFIED 16-B SQRT CSLA (WITHOUT USING MUX)

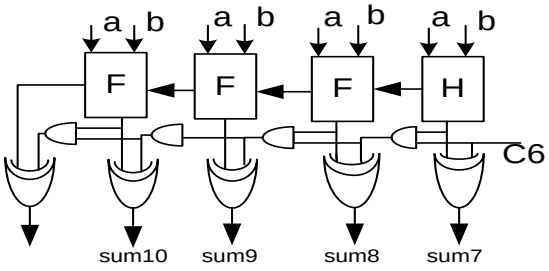
In this method CSLA with cin=1 and multiplexer is replaced by the simple combinational circuit which consists of XOR and AND gates. By using this method area and power is reduced when compared to regular CSLA and modified CSAL(BEC). The modified 16-bit CSLA without using mux is shown in fig.7 REF[5]. The structure is again divided into five groups with different bit size RCA and Combinational.

Initially RCA structure is calculate for cin =0 the output of full adder is given to the combinational circuit and one of the input of that combinational circuit is previous stage carry then it will provide the proper output by using Xor and And gates structure. The group 2to 5 of the modified 16-bit CSLA is shown Fig. 8.Comparing the group 2 to 5 of regular, modified BEC and WITHOUT MUX CSLA, it is clear that in this structure area and power is reduced.





(b)



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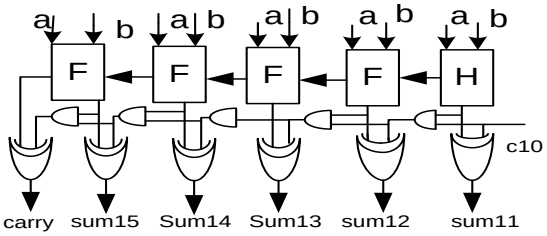


(d)

Fig .8 internal structure of Modified CSLA (Without using Multiplexer) group A to D

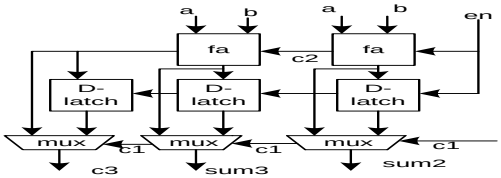
But the disadvantage of WITHOUT MUX method is that the delay is increasing than the regular CSLA and modified BEC.

VI. PROPOSED CSLA USING D-LATCH

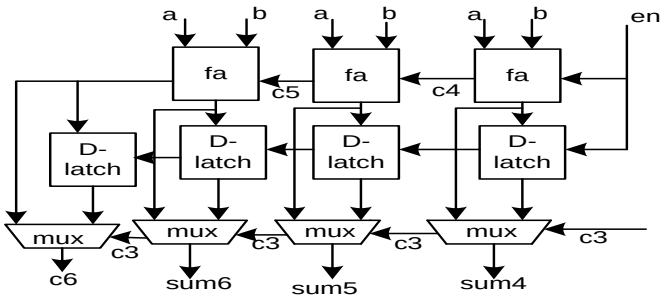
In this method replace any one of the RCA structure (i.e. cin =1 or cin =0) by parallel structure of D-latches. For n bit RCA structure it required n D-latches with enable pin as a clk. Latches are used to store one bit information. The RCA structure cin is replace by enable pin , where enable signal is clk signal. When enable pin en =1 then the RCA structure is calculate for cin=1 that result is stored in D-latch. When en =0 then it will calculate for cin =0 and the D-latch output and full adder output is given to the mux. By using selection line it will gives the proper output.

Where the enable time period for '1' is very less when compared to the enable pin '0'. Initially RCA stracture will calculate for en=1 and then en =0. The architecture of proposed 16-b CSLA is shown in Fig. 10. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e., most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. 9, it can understand that latch is used to store the sum and carry for Cin=1.

Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry. The Fig.9 shows the internal structure of group 2 to 5 of the proposed 16-bit CSLA.

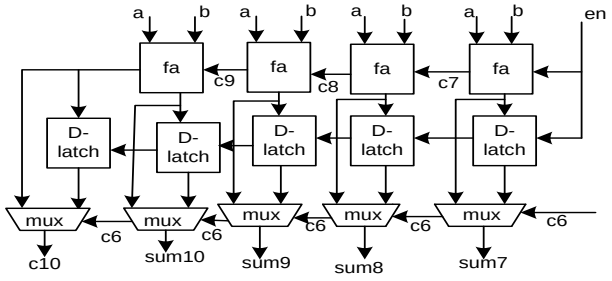


(a) Internal structure of 3 D-latchs in parallel block of Fig.10



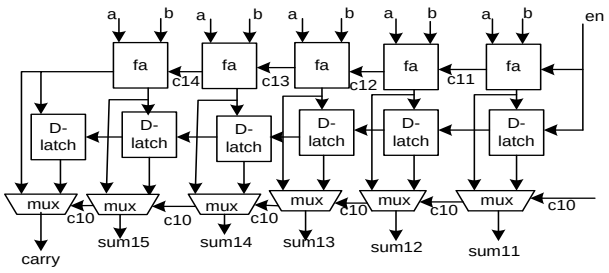
(b)

Internal structure of 4 D-latchs in parallel block of Fig.10



(c)

Internal structure of 5 D-latchs in parallel block of Fig.10



(d)

Internal structure of 6 D-latchs in parallel block of Fig.10

Fig.9 internal structures of Proposed CSLA by using D-Latch

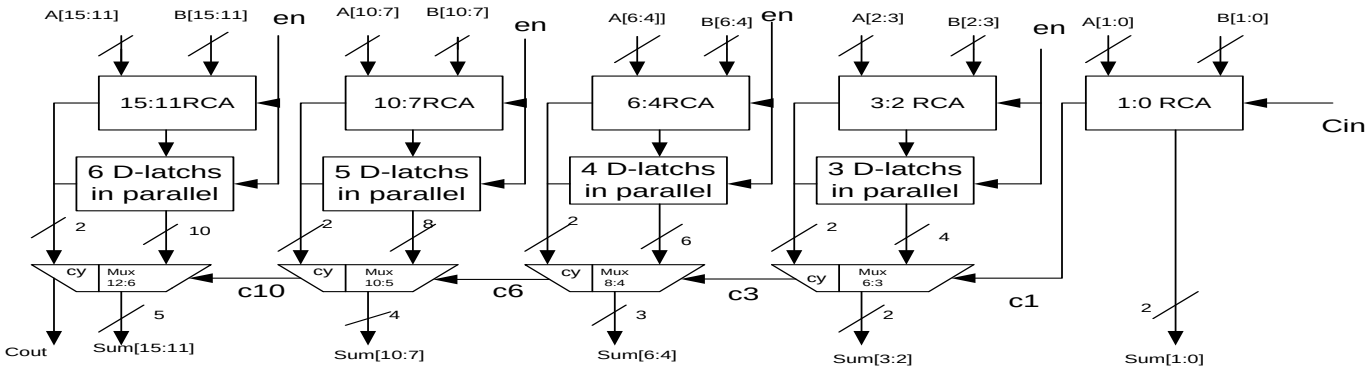


Fig.10 Proposed Paper by using D-Latch

VII. SIMMULATION RESULTS

The design proposed in this paper has been developed using Verilog-HDL and synthesized in Synopsys RTL design compiler. The similar design followed for all regular, modified and Proposed SQRT CSLAs. Table 1 to 4 exhibits the simulation results of all the CSLA structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power. The percentage reduction in the cell area, total power, total delay, power-delay product and the area–delay product as function of the bit size are shown in below Table. Also plotted is the percentage delay and power reduced in Fig. 11 It is clear that the delay of the 8-, 16-, 32-, and 64-b proposed SQRT CSLA is reduced by 4.6%, 49.3%, 44.5%, and 59.08%, respectively when compared to regular SQRT CSLA. Power reduction of the proposed paper when compared to regular SQRT CSLA 8, 16, 32 and 64-b is 10.8%, 17.73%, 20.01% and 21.9%, respectively.

COMPARISON OF REGULAR AND MODIFIED SQRT CSLA WITH PROPOSED PAPER:

Table 1: 8-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)
8 bit	Regular CSLA	2.195	955.937	15.241	33.45
	BEC CSLA	3.336	628.906	14.229	47.46
	Without Using MUX	3.337	434.843	7.956	26.55
	Using D-latch	2.094	952.343	13.598	28.47

When compared to regular and modified circuit delay is reduced but power and area is increased negligibly when compared to modified CSLA without using mux only.

Table 2: 16-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)
16 bit	Regular CSLA	4.848	2016.093	35.631	172.73
	BEC CSLA	3.941	1362.031	33.458	131.793
	Without Using MUX	6.201	952.343	18.413	114.14
	Using D-latch	2.450	1901.093	29.311	71.80

When compared to regular and modified circuit delay is reduced but power is increased when compared to modified CSLA without using mux. But here the power delay product and area delay product is reduced when compared to regular and modified circuit.

Table 3: 32-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)
32bit	Regular CSLA	6.587	4161.562	77.499	510.48
	BEC CSLA	6.729	2813.906	71.450	480.78
	Without Using MUX	9.539	1958.593	39.0177	372.18
	Using D-latch	3.655	3856.093	61.409	224.41

When compared to regular and modified circuit delay is reduced but power is increased when compared to modified CSLA without using mux. But here the power delay product and area delay product is reduced when compared to regular and modified circuit.

Table 4: 64-bit results comparison

Bit size	Type of adder	Delay(ns)	Area(nm)	Power(mw)	Power delay product(10^ -12)
64 bit	Regular CSLA	11.169	8377.031	161.870	1807.92
	BEC CSLA	11.181	5760.7812	147.69	1651.17
	Without Using MUX	15.542	4057.3437	81.304	1263.40
	Using D-latch	4.566	7593.593	126.371	577.0

When compared to regular and modified circuit delay is reduced but power is increased when compared to modified CSLA without using mux. But here the power delay product and area delay product is reduced when compared to regular and modified circuit.

The design proposed in this paper has been developed using Verilog-HDL and synthesized in Synopsys RTL compiler.The similar design followed for all regular, modified and Proposed SQRT CSLAs. Table exhibits the simulation results of all the CSLA structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power. The percentage reduction in the cell area, total power, total delay and power-delay product as function of the bit size are shown in above Table[1-4]. Also plotted the percentage reduction in delay and power is shown in Fig. 11(a),Fig.11(b) respectively. It is clear that the delay of the 8-, 16-, 32-, and 64-b proposed SQRT CSLA is reduced by 4.6%, 49.3%, 44.5%, and 59.08%, respectively when compared to regular SQRT CSLA. Power reduction of the proposed paper when compared to regular SQRT CSLA 8, 16, 32 and 64-b is 10.8%, 17.73%, 20.01% and 21.9%, respectively.

Fig.12 shows the Simulation results of 64-bit CSLA using D-Latch. And Fig13 shows the power and delay calculation results by using synopsys of 64-bit CSLA using D-Latch.

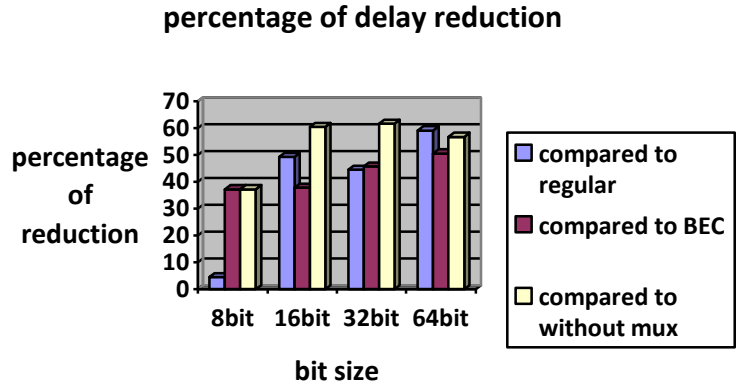


Fig .11(a) percentage in delay reduction

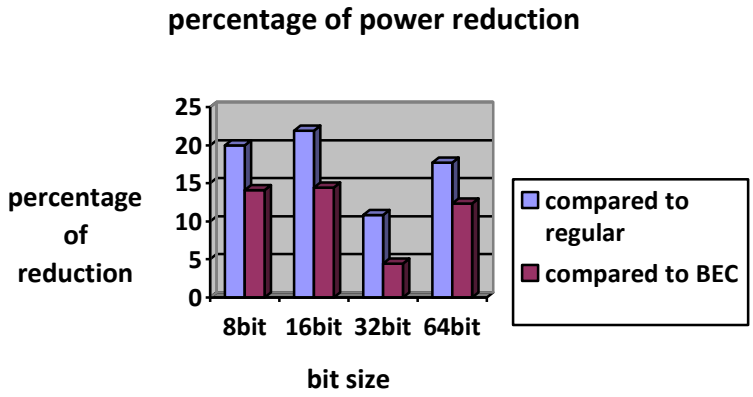


Fig.11 (b) percentage in power reduction

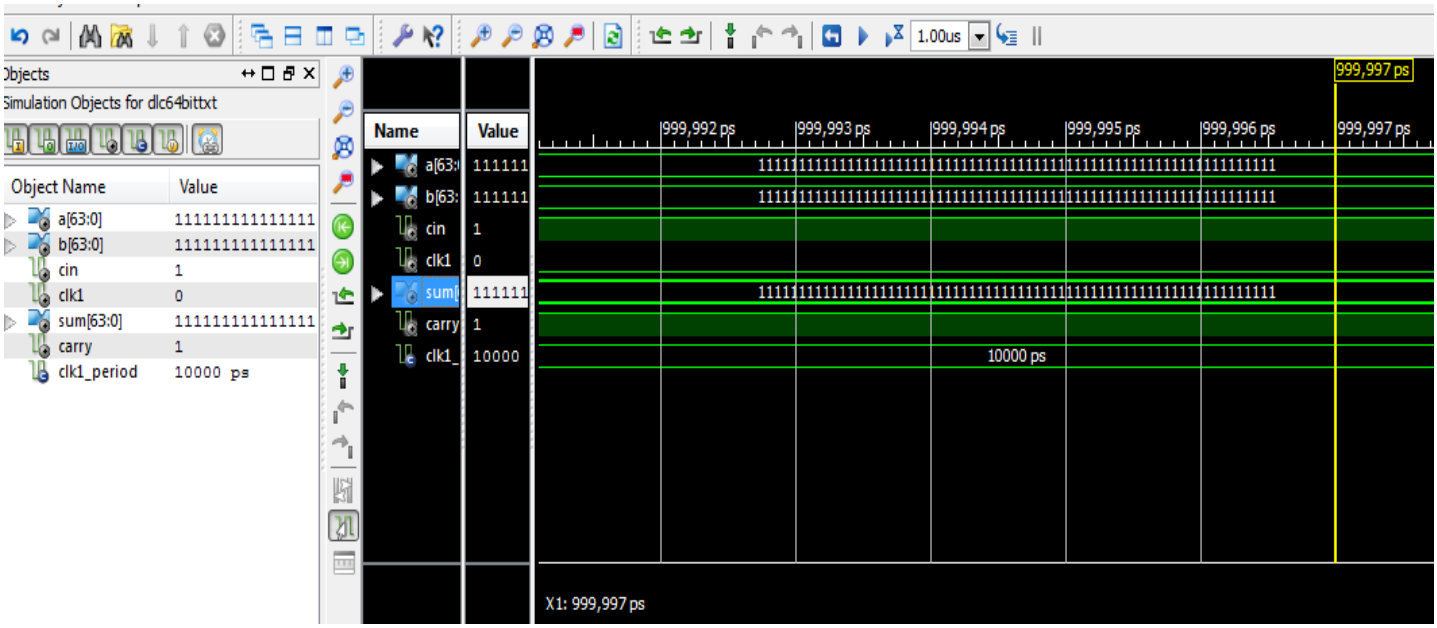


Fig.12 Simulation result of CSA using D-Latch

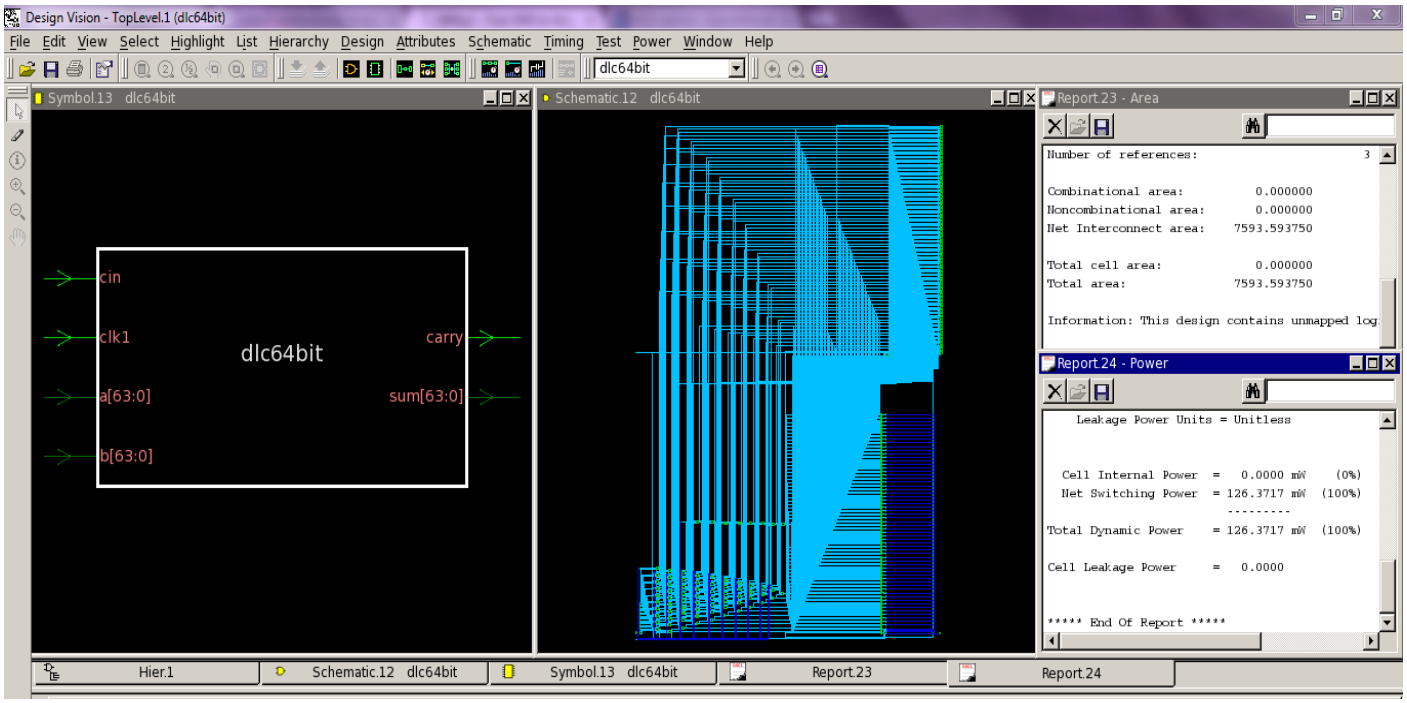


Fig.13 Power and Delay calculation of proposed circuit by using synopsys tool

VIII. CONCLUSION

A uique approach is proposed in this paper to reduce the area, power and delay of SQRT CSLA architecture. This paper shows the design of carry select adder implemented by using D-Latch and compared with regular CSA and modified CSA(BEC and Without using Multiplexer). All these adders are implemented on Spartan XC3S500E FPGA device and the performance is compared. Power and Area is calculated by using synopsys RTL tool. This paper having better results when compared to CSA and modified techniques.

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