Design of an Efficient Automatic Repairing System

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Abstract- Self-repairing digital systems have recently emerged as the most promising alternative for fault-tolerant systems. The proposed system is developed for automatically detect the fault and correcting it in digital system with high efficiency using self-repairing technique. It composed of structural layer and gene control layer. The structural layer consists of working modules, spare modules and their interconnections. In these system, each module of our system connecting with four spare modules for replacing faulty working modules at four times. Gene control layer controls the operation of modules. The module is the encoded data, called the genome, contains information about the function and the connection. Therefore, a faulty module can be replaced and the whole system's functions and connections are maintained by simply assigning the same encoded data to a spare (stem) module. The gene control layer determines the neighboring spare module in the structural layer to replace the faulty module without collision. We verified the self repairing digital system mechanism by simulating the system in Xilinx software.

Index Terms- Dynamic routing, redundancy, self-repair, stem cell.

I. INTRODUCTION

Reliability has always been an issue with electronic systems ever since the first electronic systems were designed. Electronic systems are so fragile that affect the whole system when a single problem is occur. Devising fault-tolerant system that can deal with such problem has been a considerable challenge. The project "Design of an efficient self-repairing digital system" has the interesting field namely Testing of VLSI circuits which are in the field of Engineering. Testing is the process of exercising a product and analyzing its resulting response to check whether faults are introduced during the manufacturing or operation phase. Testing is needed for circuit manufacturers must thoroughly test their products before delivering them to customers. The causes of circuit can be divided into two main categories design errors and manufacturing defects.

The self-repairing circuit can recover from a fault by isolating the faulty block. And differentiating the spare block which contains the same genetic code previously held in the faulty block. In this system a small part (faulty cell) of the system only need to be change. Moreover this system can recover a working cell several times.During the early stages, if fault occur in digital system whole system get affected. It can be corrected by replacing faulty blocks and the rerouting is made for normal operation using triple modular redundancy [1], self healing approach [2]. It takes long time and also large part of the circuit must be replaced even if a small part in the module is malfunctioning. Essential procedures of self-repair, cell replacement and rerouting process are highly complex. So implementation is very difficult in this situation.

The proposed system simplifies the self-repairing mechanism and also it gives enough efficiency when number of hardware increases. While adding spare modules it ensuring good fault-coverage. Self-repairing system composed of structural layer and gene control layer. Structural layer consist of both working cell (WC), spare cell (SC) and their interconnection. Gene control layer consist of Index Changing Unit (ICU), Differentiation Unit (DU). It determines the proper spare module in the structural layer to replace the faulty module without collision. This self-repairing mechanism is operated in parallel. So, even several faults occur in different modules at same time, the system can recover them.

We consider a Full adder is a working cell.This paper is organized as follows. Section II presents the overall mechanisms between components in the proposed system. Section III and IV describes the functional layer and gene control layer of new self repairing architecture. . In Section V the comparison with existing approaches are explained Section VI, the proposed system is implemented in XILINX and the experimental result is illustrated. Section VI summarizes the proposed system and describes future studies.

II. OVERVIEW OF THE PROPOSED SELF-REPAIRABLE DIGITAL SYSTEM

Self repairing mechanism consists of two layers, Structural layer and Gene-control layer which are shown in fig. 1. The structural layer consists of working modules, spare modules and their interconnections. The module has a basic structure, encoded data and fault detection unit. Each cell has identical structure, and modules are classified as working cell, spare (stem) cell or isolated cell. Each and every WC has four neighboring SC's. Similarly every SC's connected with four sides of WC's. The gene control layer determines the neighboring spare module in the structural layer to replace the faulty module without collision. The gene control layer is positioned in parallel with structural layer. It composed of index changing unit and differentiation unit. Gene control layer controls the operation of cells in the structural layer.

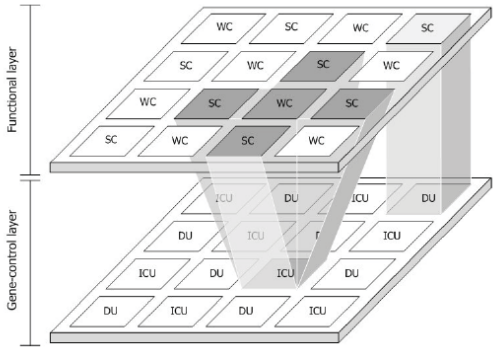

Fig. 1. Proposed self-repairing digital system. Overall architecture and related cells between the functional layer and the control layer.

III. NEW SELF-REPAIRING ARCHITECTURE: FUNCTIONAL LAYER

Structural layer is also called a functional layer. This structural layer composed of several working modules, spare modules and the routing architecture between cells. The module has a basic structure, encoded data and fault detection unit. Each cell has identical structure, and modules are classified as working cell, spare (stem) cell or isolated cell. Each and every WC has four neighboring SC's. Similarly every SC's connected with four sides of WC's.

In the event of fault occurrence WC can be replaced by any of the available SC from four neighboring SC's. Consider SC1, SC2, SC3 and SC4 are placed left, down, right and top side of WC respectively. When WC gets fault it replaced by SC1 (left SC). If SC1 is busy with some other WC's, then the faulty WC is replaced by SC2 (down SC). It is an anticlockwise operation.

The WC has some encoded data, which is available in all four neighboring SC's. Because of this reason WC can be replaced by any available neighboring SC for normal fault free operation. A WC can be replaced up to four times even though the number of SC's is similar to the number of WC's

A. Routing architecture

Fig. 2. shows how the WC's and SC's are arranged for this self-repairing mechanism. While two WC's can be replaced by neighboring SC's WC2gets input from the output of WC1. WC1 connects its output with four neighboring SC's in the same way WC2 receives its input from output of WC1. This connection between WC1 (SC's of WC1) and WC2 (SC's of WC2) is made dynamically by input selection MUX. This connection is controlled by encoded data of each cell. Each WC has four MUX. In case of WC1 is connected with WC2 through the first MUX, the remaining inputs and outputs of cells connected to the wire are disconnected. After replacing the WC1 and WC2 with spare cells SC1 of WC2 receives input from SC of WC1 output. Hence the routing architecture has an efficient in a complex circuit also.

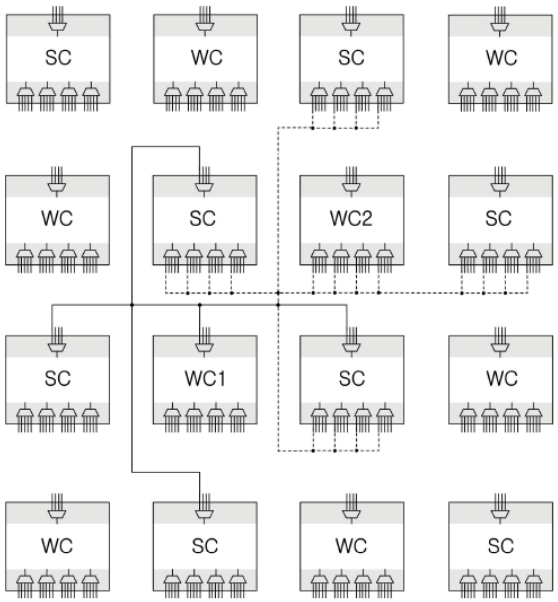

Fig.2. Artificial routing architecture, the proposed connection from WC1 to WC2 by a connecting solid line and dotted line.

Many systems are affected by soft memory errors than the hardware failure. Fault detection unit is mainly for detecting the fault and correcting it. Flow chart of fault detection and correction operation is shown in fig. 3. There are three types of physical faults. Permanent fault: A hardware malfunction that always occur when a particular set of conditions exists, and that can be made to occur deliberately, in contrast to a sporadic fault.Intermittent fault:It is a malfunctioning of a device or system that occurs at intervals, usually irregular. An intermittent fault is caused by several contributing factors. Transient fault: It is a fault that is no longer present if power is disconnected for short time and then restored.

Fig.3 Flow chart of fault detection and correction.

IV. IV. NEW SELF-REPAIRING ARCHITECTURE: GENE-CONTROL LAYER

The gene control layer is positioned in parallel with structural layer. It composed of ICU and DU. Gene control layer controls the operation of cells in the structural layer. Every ICU is the responsible for every WC and its four neighboring SC's. DU is assigned proper SC for fault recovery by replacing SC from WC. When the fault occurred, it propagates to the ICU. ICU changes the SC's index bits and isolates the WC. Then DU in the SC differentiates the SC from the faulty WC.

Every SC has index bit, which is in the gene control layer. Index bit shows the state of each cell in structural layer. There are three types of index bits changing during runtime. The index bits for each SC in gene control layer are shown in table. I.
State bit: It shows the spare cell is available are not.

Direction bit: It shows the direction of spare cell
Differentiation bit: It differentiate spare cell from WC.

State bit	Stem cell		0
	Working or Isolated cell		1
Direction bits	The direction of the WC for which stem cell is differentiated	Left	00
		Down	01
		Right	10
		Up	11
Differentiation bit	No change		0
	Differentiate the stem cell		1

Table 1 Index bits for each stem cell in gene-control layer

A. Index changing unit

The ICU operation is explained in table.4.2. Here W is the functional cell and LS, DS,RS and TS are left spare cell, down spare cell, right spare cell and top spare cell of W respectively. After receiving fault signal from the structural layer all the possible changes of index bits is shown in table. II

The condition for the change					state before fault					state after fault occurrence									
Fault signal					state bit					differentiation bit					direction bit				
W	LS	DS	RS	TS	W	LS	DS	RS	TS	W	LS	DS	RS	TS	W	LS	DS	RS	TS
1						0					1								
1						1	0					1					01		
	1					1	0					1					01		
1						1	1	0					1					10	
	1					1	1	0					1					10	
		1				1	1	0					1					10	
1						1	1	1	0					1					11

Table 2 Index changing unit

In table.4.2 the first line delivers the condition for the change (W=1) fault will be present, the state bit before the fault occurrence (LS=0) left spare cell is free, the direction bit after the fault occurrence (LS=1) W is replaced by LS, and direction bit is changed to 01 for next time fault occurrence.

B. Differentiation unit

The state before the differentiation			The state after the differentiation	
Differentiation bit	direction bit	state bit	state bit	direction of WC for SC substitute
1	00	0	1	right
	01			top
	10			left
	11			down

Table 3 Differentiation unit

Every SC has a DU, which differentiates SC with WC and differentiation bit. If the differentiation bit of the spare cell is changed to "1" while having the direction bits of "10," the spare cell is differentiated into a cell like the WC, which is located on the right side.

V. COMPARISION WITH EXSISTING APPROACHES

A. Triple modular redundancy

In computing, triple modular redundancy, sometimes called triple-mode redundancy, (TMR) is a fault-tolerant form of N-modular redundancy, in which three systems perform a process and that result is processed by a majority-voting system to produce a single output. If any one of the three systems fails, the other two systems can correct and mask the fault.The TMR concept [1] can be applied to many forms of redundancy, such as software redundancy in the form of N-version programming.

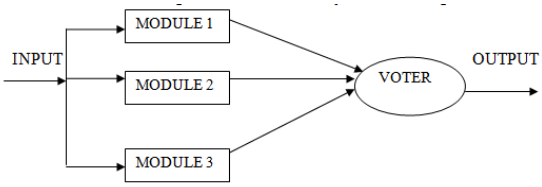

Fig. 4. Triple Modular Redundancy

In TMR, three identical logic circuits (logic modules) are used to compute the same set of specified Boolean function. If there are no circuit failures, the outputs of the three circuits are identical. But due to circuit failures, the outputs of the three circuits may be different. A voter circuit is used to decide which of the circuit's outputthe correct output is. The majority voter output is 1 if two or more of the inputs of the majority voter are 1; output is 0 if two or more of the majority voter inputs are 0. The disadvantage of this system is to cover the fault once. If all the three modules are faulty, then this system does not produce the correct output.

B. Muxtree method

A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. In this method, a digital circuit is converted into an array of

MUXTREE cells and the initial connection information among the MUXTREEs is encoded as a gene in each MUXTREE cell.

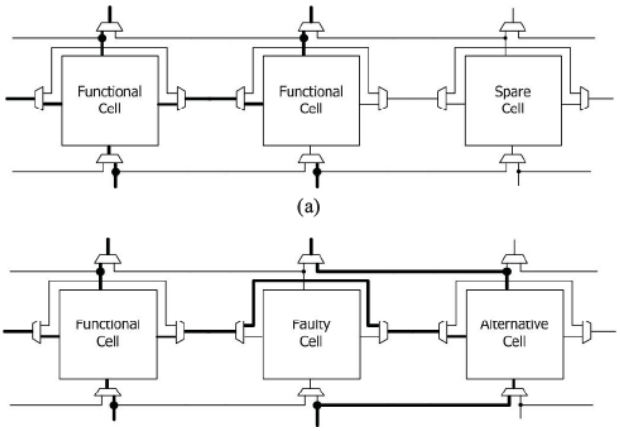

Fig. 5. Rerouting in the MUXTREE approach.

This system consists of molecular level, cellular level and organ level. In the MUXTREE system, if a fault cannot be recovered at the molecular level, it can then be recovered at the cellular level by replacing the faulty cell with an SC[3]. Although this allows the MUXTREE system to recover multiple faults, it requires many SCs. The disadvantage of this system is it consumes long time to recover faults and it has less fault coverage.

C. Self-healing system

Self-healing system is one of the fault tolerance techniques [2].Router cells do not exist in the original circuit, which has no self-repairing property, and hence the router cell as well as the spare cell is considered as overhead in the analysis. The self-healing approach has a router cell that helps the system bypass a faulty cell after replacement of a cell. If a functional cell [F2 in Fig. 6(a)] is substituted by a spare cell [S1 in Fig. 6(a)], the router cell connects the output of the functional cell [F1 in Fig. 6(b)] to the new functional cell [F2 in Fig. 6(b)] [7].

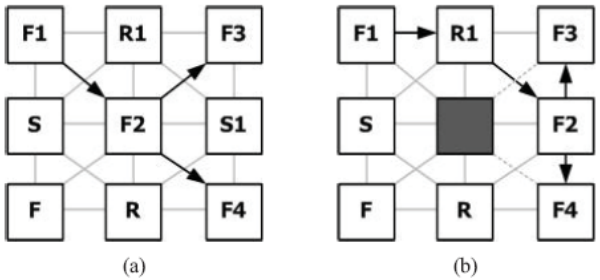

Fig. 6. Rerouting in the self-healing approach. (a) State before the fault occurrence. (b) State after the fault occurrence

The disadvantage of this system is if the router cell fails, it stops its operation and the efficiency cannot be achieved.

VI. EXPERIMENTAL RESULT

Fig. 7 shows the basic structure of every working cell. That working cell may be any kind of combinational circuit. Here the basic structure of working cell is full adder. The full adder consists of three inputs a, b and cin and two outputs sum and carry. A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Cin. A and B are the operands, and Cin is a bit carried in from the next less significant stage. A full adder can be constructed from two half adders by connecting A and B to the input of one half adder, connecting the sum from that to an input to the second adder, connecting Ci to the other input and OR the two carry outputs. A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates.

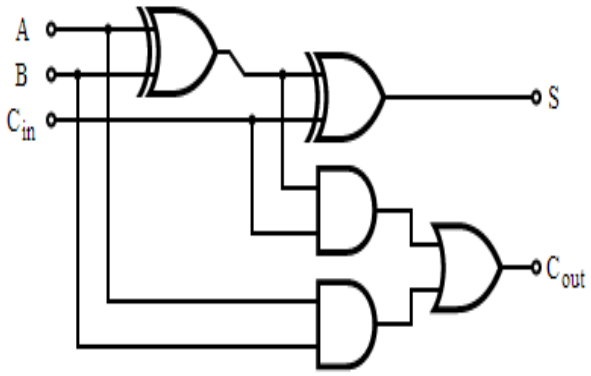

Fig. 7. Structure of full adder.

If that full adder working cell is faulty, then it can be replaced by the stem cell. That stem cell contains the same circuit as that of the working cell. An SC can be replaced by any of its four neighboring WCs for fault recovery. For example, the working cell full adder goes faulty; the WC is replaced by the left side stem cell SC00.Fig. 8show the faulty WC is replaced by SC00.

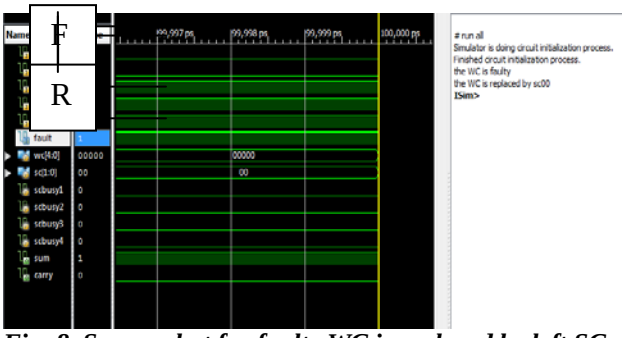

Fig. 8. Screen shot for faulty WC is replaced by left SC

VII. CONCLUSION

In this project a new self repairing digital circuits provides good fault coverage. This system detects any type of faults and corrects it. It uses four stem cells for every WC. Fault in the WC can be detected by fault detection unit and it propagates to the index changing unit. It has three index bits for changing the

direction and state of the fault. The differentiation unit differentiates SC from the faulty WC. If any SC is busy the faulty WC is replaced by some other SC. So the faulty WC is replaced by SC without collision. In this system there is no need of dynamic routing, reconfiguration and rerouting.

While adding additional stem cells for more number of fault recoveries efficiency is achieved. Our future goal is to develop self repairing digital circuits using six stem cells.

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