

AREA AND POWER EFFICIENT CMOS ADDER DESIGN BY HYBRIDIZING PTL AND GDI TECHNIQUE

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Abstract- In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling factors. Leakage power accounts for an increasingly larger portion of total power consumption in deep submicron technologies. Recently, in technology the power density has increased due to combination of higher clock speed, smaller process geometries and scaling factors, layout structure and greater functional integration. As results static power consumption is becoming more dominant state. This is a challenge for the CMOS integrated circuit designers. However the integrated CMOS designers do have a few methods which they can use to reduce this static power consumption. Since, these methods have some drawbacks. To attain lowest static power consumption one has to sacrifice design area and circuit performance. In this paper we proposed a new method to reduce static power in the CMOS VLSI circuit using dual stack approach without being penalized in area requirement and circuit performance.

Index Terms- dual stack approach, static power saving technique, stack effect, static power reduction.

1. INTRODUCTION

A large proportion of digital functional blocks are only active for a small fraction of time. When the functional block is not operated leakage still occurs. In submicron technology such a phenomenon is aggravated due to the reduced threshold voltage from scaling. Leakage power occurs 40% of total power consumption in today's high performance microprocessors. Leakage power reduction becomes the key to a low power design. CMOS technology features size, scaling factors and threshold voltage have been scaling down for decades for achieving high density and high performance. Because of this technology trending transistors leakage power has increased exponentially. As the features size becomes smaller, shorter channel lengthened result increased Sub-threshold leakage current through a transistor when it is off.

Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons the static power consumption that is leakage power dissipation has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provided an efficient way to reduce leakage power but disadvantages of each technique limit the application of each technique. We propose a new approach providing a new choice to low-leakage power VLSI designers. The previous techniques were summarized and compared with our new approach presented in this paper.

II. FULL ADDER CIRCUITS

Static logic style gives robustness against noise effect automatically provides reliable operation immediately. The Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. It also suffers from static power dissipation. Implementation of enlarged multiplexers and XOR based circuits are advantageous in pass transistor logic.

The dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general all the mentioned styles cannot compete with CMOS style in robustness and stability. The conventional CMOS 28 transistors adder circuit design shown in Figure 1. Figure 1 it is considered as base case throughout this paper. The comparison with base case. Transistor sizes are specified as a ratio of Width/Length (W/L).

It is observed that the conventional adder circuit that the transistors ratio of PMOS to NMOS is 2 for an inverter. Further power gating technique is used to reduce the leakage power where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. The sizing of each block is based on the following basis. The sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the Width/Length ratio of transistor. The reduced sizes reduce the area occupied by the circuit. This will reduce the silicon chip area and in term reduction in the cost.

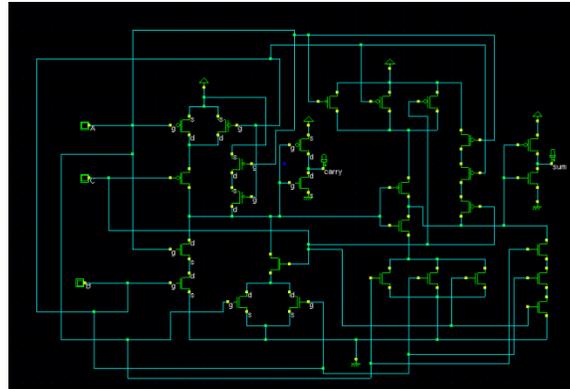


Figure 1. Conventional CMOS full adder (Base case).

Modified adder circuit of Design 2 is shown in Figure 3 of 90nm technology. The W/L (width/length) ratio of PMOS is 1.5 times than of W/L (width/length) ratio of NMOS. Each block has been treated as an equivalent inverter. The aim of this design is to reduce the standby leakage power. Further compare to the Base case with both (90nm technology) Design 1 and (70nm technology) Design 2. The ground bounce noise produced when a circuit is connected to sleep transistor is reduced.

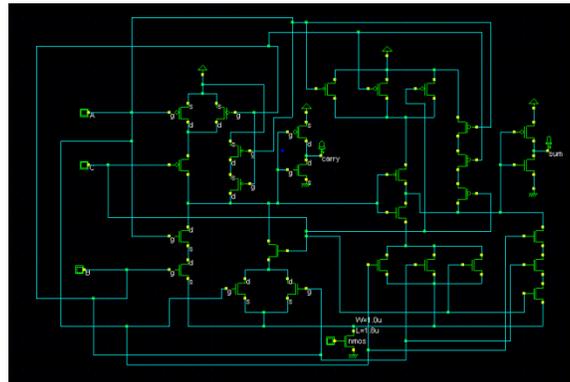


Figure 2. (Design 1) Full adder circuit with sleep transistor (90nm technology).

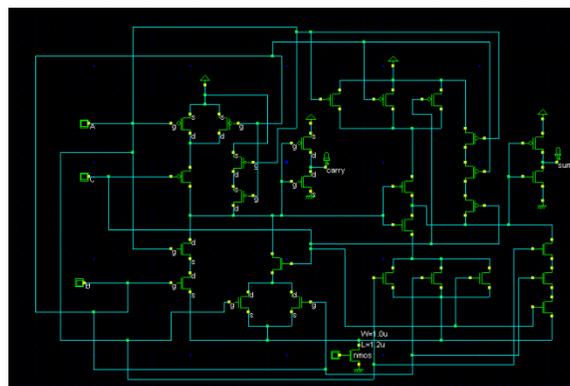


Figure 3. (Design 2) Full adder circuit with sleep transistor (70nm technology).

III. PERFORMANCE ANALYSIS

A. Active Power.

Power dissipated by the circuit when the circuit is in active state is termed as Active power. Input vectors are fed into the circuit and the average power dissipation is measured. All of the input combinations are considered for simulation. The same input vectors combination have been given to the all three designs- Base case, Design 1 and Design 2 a comparison has been made for the same in both 90nm and 70nm technologies.

B. Standby leakage power.

Standby leakage power is measured when the circuit is in standby mode. Sleep transistors are connected to the pull down network of 1-bit full adder circuit. Sleep transistor is off by asserting an input 0v. Size of a sleep transistor is equal to the size of largest transistor in the network (pull up or pull down) connected to the sleep transistor. The sleep transistor size in (90nm technology) Design 1 and Design 2 (70nm technology) is reduced due to the resizing of the adder cells in proposed circuit. Standby leakage power is measured by giving different input combinations to the circuit. Standby leakage is greatly reduced in both Design 1 and Design 2 for both 90nm and 70nm technologies.

C. Four bit adder active and standby power.

Full adder cells shown in figure 1, figure 2 and figure 3 are used to design 4-bit ripple carry adder. Four-bit adders are in all three designs Conventional, Design 1 and Design 2. For both 90nm and 65nm technologies are constructed. The active power and standby power are calculated. An active power is calculated by setting the select terminal of the adder to logic high and standby power is calculated by setting the Select terminal to 0V. Compare of active and standby power of all the designs in both 90nm and 70nm technologies as shown in figure 4 and figure 5.

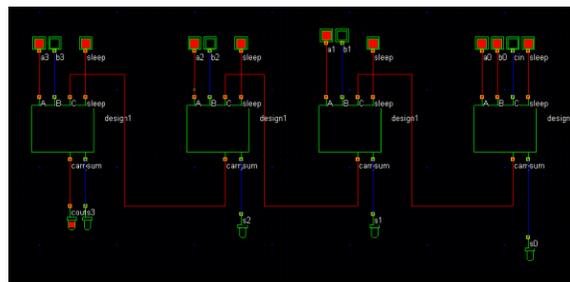


Figure 4. Four-bit full adder (Design 1) 90nm technology.

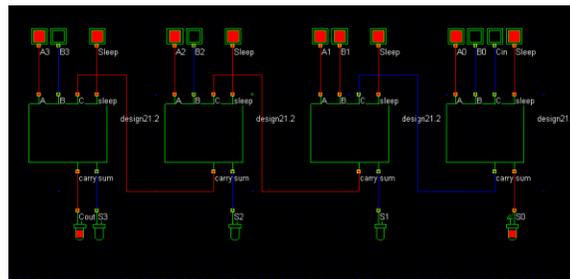


Figure 5. Four-bit full adder (Design 2) 70nm technology.

IV. PROPOSED DESIGN

We review proposed circuit level approaches for sub-threshold leakage power reduction.

Dual Sleep Approach

Dual sleep approach use the advantage of using two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. The dual sleep portion can be made common to all logic circuitry less number of transistors is needed to apply a certain logic circuit.

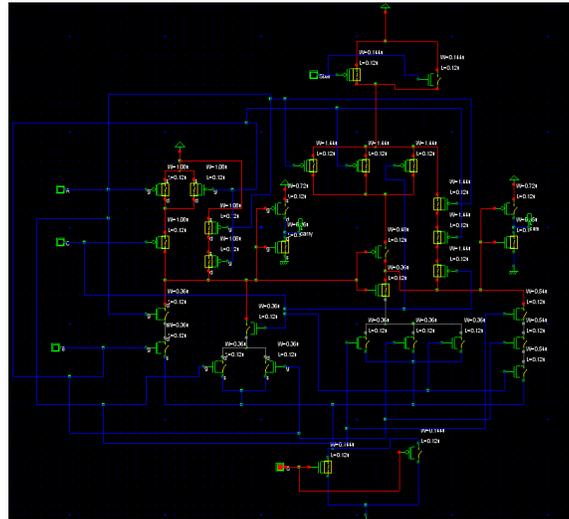


Figure 6: One-bit full adder using dual sleep approach.

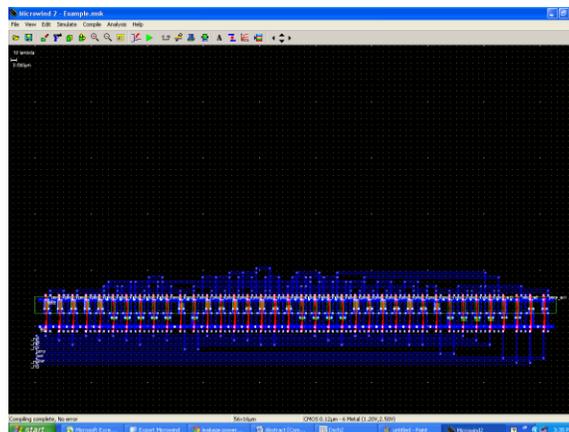


Figure 7: Layout for one-bit full adder using dual sleep approach.

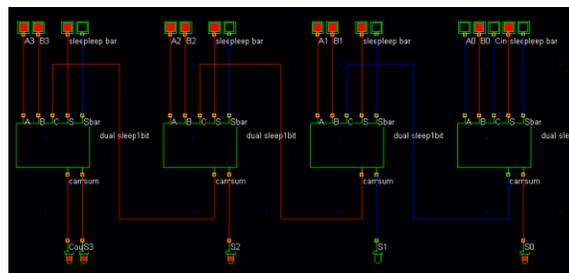


Figure 8: Four-bit full adder design using dual sleep approach.

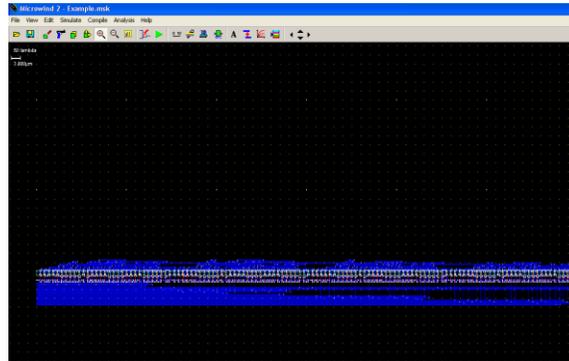


Figure 9: Layout for four-bit full adder design using dual sleep approach.

V. SIMULATION METHODOLOGY

We compare the dual sleep techniques with previous approaches explained earlier namely: conventional CMOS with sleep transistor and ripple carry adder. We compare these designs approaches in terms of dynamic and static power consumption and analysis of delay as well as area.

VI. CONCLUSION

Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. In this paper we present an efficient methodology for reducing leakage power in VLSI design. The Variable Body Biasing approach shows improved results in terms of static and dynamic power and delay power analysis product. It gives the CMOS circuit designers another option in designing integrated circuits more efficiently.

REFERENCES

- [1] S.Mutohetal., "1-V Power Supply High-speed Digital Circuit Technology with Multi-threshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.
- [2] M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T.N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep submicron Cache Memories," International Symposium on Low Power Electronics and Design, pp. 90-95, July 2000.
- [3] J.C.Park, V.J.Mooney and P.P Feiffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation, pp.148-158, September 2004.
- [4] Pren R. Zimmermann, W.Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid- State Circuits, vol. 32, pp. 1079- 1090, July 1997.
- [5] S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verilog, 2006.
- [6] K.Bernstein, "Design and CAD challenges in sub-90nm CMOS technologies," in Proc. int. conf. comput. Aided Des., 2003, pp. 129- 136.
- [7] N.West. K. Eshragian, Principles of CMOS V LSI Design: A systems Perspective, Addison- wesley, 1993.
- [8] Ku He, Rong-Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction during Mode Transition," in ICCD07, pp. 388-394, 2007.