Hard ware implementation of area and power efficient Carry Select Adder using reconfigurable adder structures

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Abstract- In data processing processors, adder is a basic digital circuit. To perform any arithmetic operation, addition is the basic operation to perform. To compute fast arithmetic operations adder must be fastest. CSLA is the fastest adder when compare to RCA and CLA. From the structure of CSLA it is observed that there is a scope to reduce area further so that power can be lowered [3-4]. This paper proposes a new architecture of CSLA using reconfigurable adder structures (RAS) and is compared with regular SQRT CSLA, CSLA using BEC [7]. The experimental analysis shows that the proposed CSLA using RAS is having advantages regarding area and power**.**

Index Terms- area efficient, low power, CSLA, BEC, SQRT CSLA and RAS

I.INTRODUCTION

In VLSI designing, most important areas of research is to design area and power efficient data processors. In digital adders, speed of addition operation depends on the propagation of carry bit through the adder. In a conventional RCA sum of each bit is generated only after the previous bit has been summed and carry propagated into the next position. Next position bits has to wait until it found the previous carry bit takes longer computation time to perform addition. For fast addition operation CLA is designed which occupies more area and consumes more power. CSLA is designed to compromise between small delay and large area of CLA and longer delay and small area of RCA [5-6].

This paper provides comparison of existed designs and proposed design of CSLA using RAS. This paper structured as follows. Section II deals with literature survey. Section III deals with CSLA using dual RCA. Section IV explains about CSLA using BEC. Section V deals with CSLA using RAS. Section VI deals with the delay and area evaluation of all groups of CSLA using RAS. Simulation results are mentioned in section VII. Results are compared and analyzed in section VIII and section IX concludes the work. Section X indicates the future scope of this work

II.LITERATURE SURVEY

By generating multiple sums by considering Cin=0 and Cin=1 and then select a carry to generate sum so that the carry propagation delay has been overcome which is proposed by o.j.Bedrij.1962 [1].

Maximum carry propagation delay in last stage of carry save adder is to be reduced through BEC method which is proposed by Ram Kumar.2010 [2]. Instead of using dual RCA in SQRT CSLA, BEC method is proposed which replaces one set of RCAs thus the total area and power will be reduced to great extent which is proposed by B. Ram Kumar and Harish.M.kittur.2011 [7].

III.CSLA USING DUAL RCA

Structure of 16 bit SQRT CSLA using dual RCA is shown in fig.1. It consists of five groups with different sizes of RCAs. The delay and area evaluation of basic blocks used in regular CSLA is shown in table I[7]. The numerals with in square braces of fig.1. specifies the delay.

The structure of group2 is shown in fig.2. Consists of two sets of 2 bit RCA. Selection input c1 arrival time is t=7 which is later than s2[t=6] but earlier than s3[t=8]. Therefore sum2[t=10] is the summation of delay of mux[t=3]. Similar evaluation can be done for remaining other groups[7]. Area and delay evaluation of all groups listed in table II.

TABLE I

Delay and area of basic blocks of CSLA using dual RCA

Basic blocks	Delay(number of gates in critical path)	Area (total number of gates)
XOR	3	5
2:1 MUX	3	4
Half adder	3	6
Full adder	6	13

TABLE II

Delay and area count of groups in 16bit CSLA using dual RCA

Group	Delay (number of gates present in critical path)	Area (number of gates)
Group 1	7	26
Group 2	13	57
Group 3	16	87
Group 4	19	117
Group 5	22	147

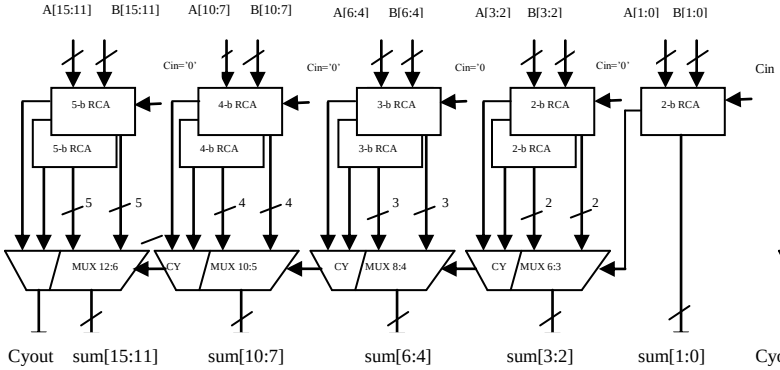

Fig.1. 16bit SQRT CSLA using dual RCA

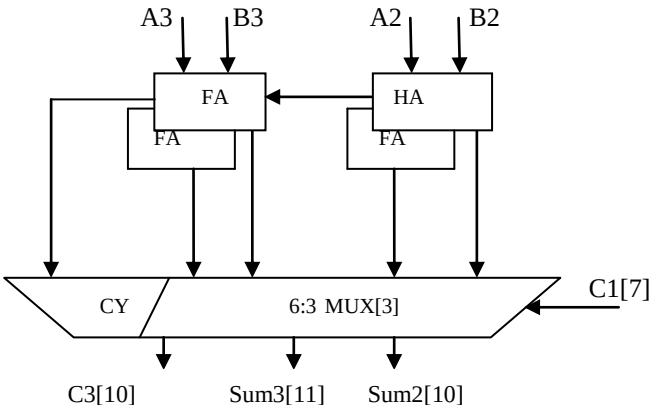

Fig.2. Delay and Area evaluation of Group2 of CSLA using dual RCA

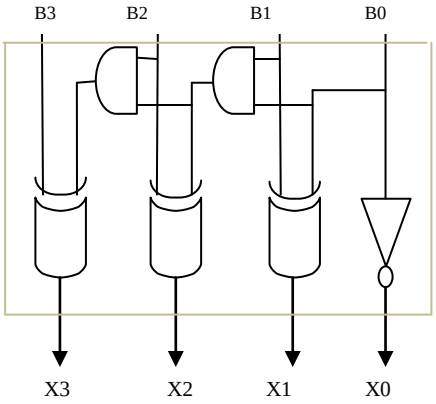

Fig.4. BEC logic

IV.SQRT CSLA USING BEC

Structure of 16bit SQRT CSLA using BEC logic is shown in fig.3. It also consists of 5 groups with different sizes of RCAs. Structure of BEC logic is shown in fig.4. In regular CSLA second set of RCA with Cin=1 can be replaced with BEC logic to reduce the area and power of conventional CSLA[]. Group2 of

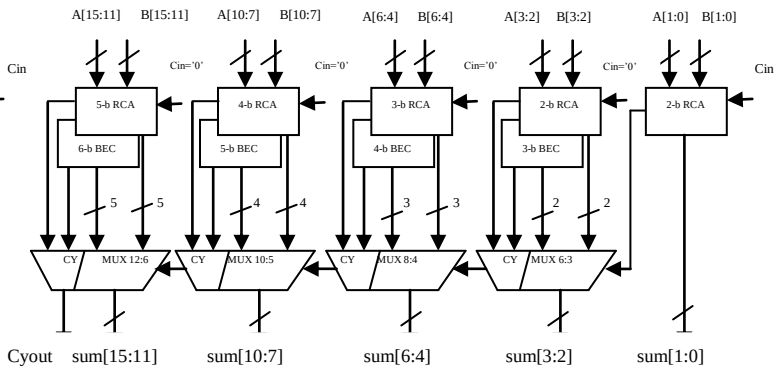

Fig.3. 16bit SQRT CSLA using BEC

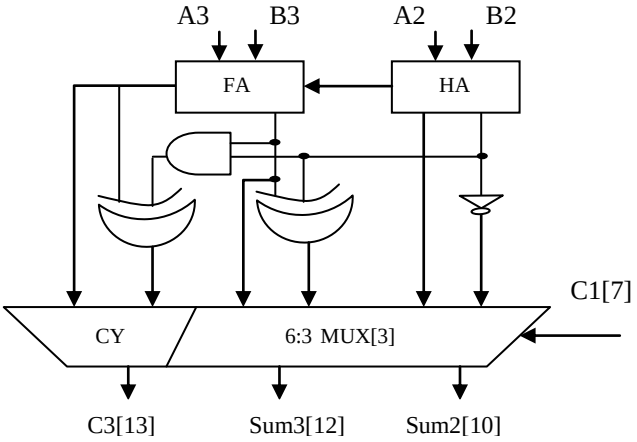

Fig 5. Delay and Area evaluation of Group2 of CSLA using BEC

H is a Half Adder
F is a Full Adder

the 16 bit SQRT CSLA using BEC is shown in fig.5. Area and delay evaluation of each group is done manually by referring table1 and listed in table III.

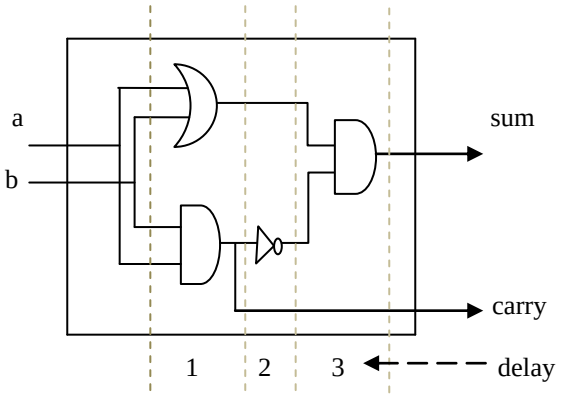

Fig.6. Reconfigured Half Adder

Group2 of 16bit SQRT CSLA using RAS is shown in fig.9. Total gate area and delay for each group is mentioned in table V.

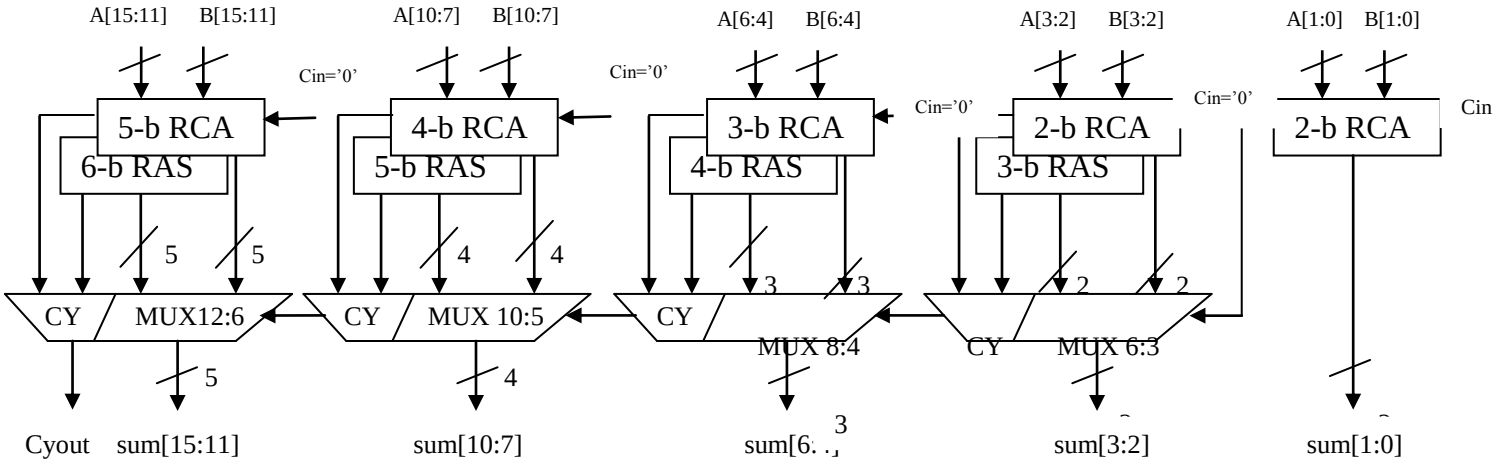

Fig.7. 16bit SQRT CSLA using RAS

TABLE III

Delay and area count of groups in 16bit CSLA using BEC

Group	Delay (number of gates present in critical path)	Area (number of gates)
Group 1	7	26
Group 2	13	43
Group 3	16	66
Group 4	19	89
Group 5	22	112

V.SQRT CSLA USING RAS

Simple gate level modification of half adder, full adder blocks can reduces total gate area without affecting the delay. Reconfigurable half adder and full adder structures are shown in fig.6.and fig.8.

The structure of SQRT CSLA using RAS is shown in fig.7. First set of RCAs consists of all full adders can be replaced with reconfigurable adder structures hence the area reduced further. The second set of RCA of regular CSLA, BEC logic of CSLA using BEC is replaced with RAS logic consists of only half adders and not gate. Hence the area reduced furthermore. The delay and area evaluation of reconfigurable adder structures is shown in table IV. Calculation procedure of delay and area is similar to the methods followed for SQRT CSLA using BEC[7].

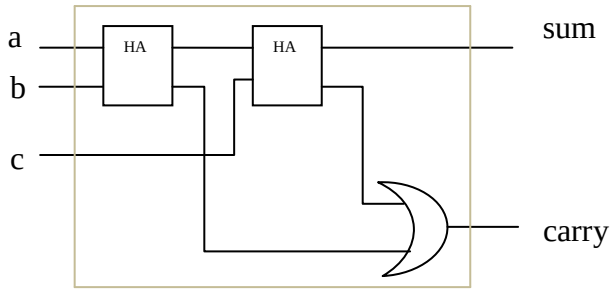

Fig.8. Reconfigured Full Adder

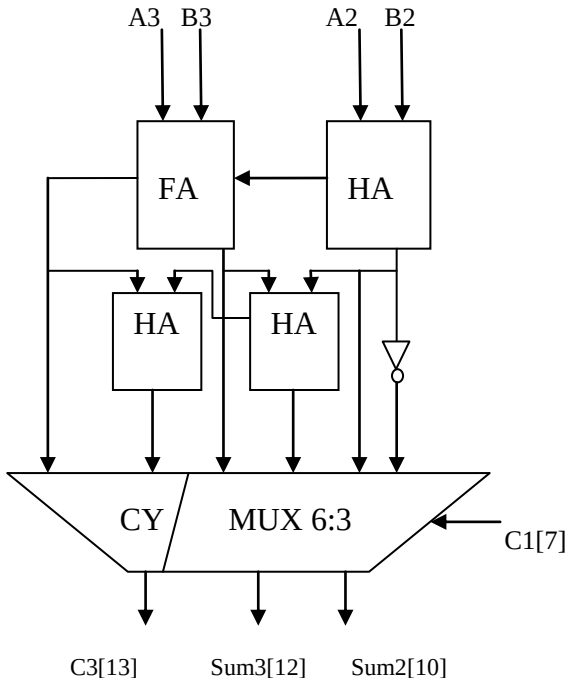

Fig.9.group 2 of CSLA using RAS

TABLE IV

Delay and area of reconfigurable structures of CSLA using RAS

Basic blocks	Delay(number of gates in critical path)	Area (total number of gates)
2:1 mux	3	4
Half adder	3	4
Full adder	6	9

VI.DELAY AND AREA EVALUATION METHODOLOGY OF 16-BIT CSLA USING RAS

Evaluation of delay and area of each group of the proposed structure is similar to the evaluation of SQRT CSLA using BEC. SQRT CSLA using RAS uses reconfigurable structures of half adder and full adder having less number of gates, hence area reduced to great extent.

Estimation of maximum delay of 16 bit CSLA using RAS is similar to the delay estimation of 16 bit CSLA using BEC[7]. By referring Tables III and V, it is clear that, the gate count in CSLA using RAS is reduced without affecting the delay.

Area evaluation has been determined as follows

Group1:-

Gate count=FA*2 =9*2=**18**

Group2:-

Gate count=FA+(HA*3)+NOT+(MUX*3)

=9+(4*3)+1+(4*3)=**34**

Group3:-

Gate count=(FA*2)+(HA*4)+NOT+(MUX*4)

=(9*2)+(4*4)+1+(4*4)=**51**

Group4:-

Gate count=(FA*3)+(HA*5)+NOT+(MUX*5)

=(9*3)+(4*5)+1+(4*5)=**68**

Group5:-

Gate count=(FA*4)+(HA*6)+NOT+(MUX*6)

=(9*4)+(4*6)+1+(4*6)=**85**

(ref table IV for individual gate areas of RAS blocks)

TABLE V

Delay and area count of groups in 16bit CSLA using RAS

Group	Delay (number of gates present in critical path)	Area (number of gates)
Group 1	7	18
Group 2	13	34
Group 3	16	51
Group 4	19	68
Group 5	22	85

VII. SIMULATION RESULTS

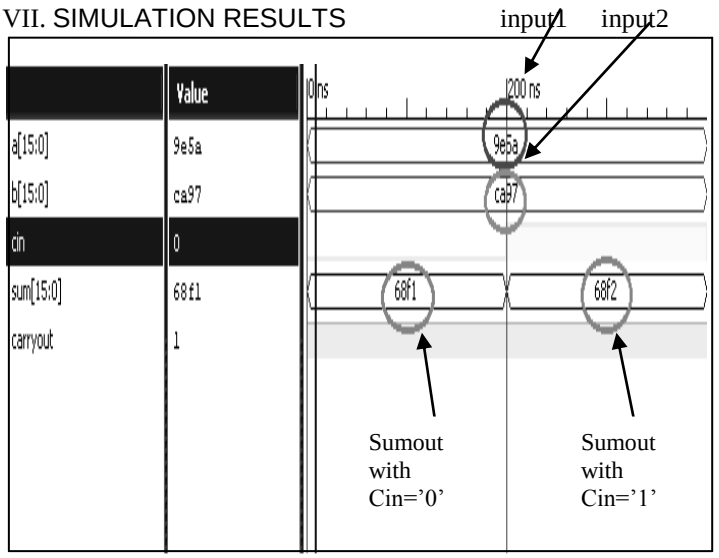

TABLE VI

Comparison of CSLA using RAS with CSLA using BEC and CSLA using dual RCA

Group	16 bit SQRT CSLA using dual RCA	16 bit SQRT CSLA using BEC	16 bit SQRT CSLA using RAS
Group 1	26	26	18
Group 2	57	43	34
Group 3	87	66	51
Group 4	117	89	68
Group 5	147	112	85
total	434	336	256

VIII.RESULT ANALYSIS

Efficiency of the SQRT CSLA can be evaluated using the comparison of number of gates utilized in the existing adders and the proposed SQRT CSLA using RAS which is shown in table VI. From the comparison table it is clear that, the proposed SQRT CSLA using RAS saves 178 gate areas than regular CSLA, 80 gate areas than SQRT CSLA using BEC without affecting gate delays. So the proposed design has given better results as compared to existing designs.

IX.CONCLUSION

A simple gate level reconfigurable approach of full adder and half adder is proposed in this paper to reduce the area and power of SQRT CSLA. The proposed CSLA with RAS is simple, low power, area efficient for VLSI implementation.

X.FUTURE SCOPE

This proposed design is implemented for 16bit word size and parameters like area, delay, power are evaluated. This work can be further extended for 32 bit, 64 bit, 128 bit and so on.

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