Area and Power Efficient Router Design for Network on Chip

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Abstract-As network on chip (NoC) systems become more prevalent in today's industry. Routers and interconnection networks are the main components of NoC. Therefore, there is a need to obtain low area and power models for these components so that we can better understand the area and power tradeoffs. In this paper a low- area and power efficient NoC architecture is proposed by eliminating the virtual channels. Buffers are replaced by elastic buffer. In order to get the advantage of both buffered and buffer less the cross bar is split in to two parts. Implementation is done in Micro wind 3.5 the proposed router area is reduced by 47.89% and power is reduced by 11.2% compared to base line router accordingly.

Index Terms- Virtual channel, NoC, Elastic buffer

I. INTRODUCTION

To solve the problem of the traditional bus in the area interconnect scaling and power consumption, etc., a new on-chip communication structure Network-on-Chip has been proposed[1].NoC provides high performance communication is at the cost of an increase in the structure complexity. An interconnection network dissipates a significant fraction of power and complexity increases the area. So power consumption and area has become important parameters in the NoC design. Routers are the most important communication components in NoC, whose power and area model is the focus of the relevant research [2]. The input buffers of router increase the power budget and chip area. Eliminating input buffers is a natural approach to design low-power NoCs or reducing the number of input buffers overhead degrades the network performance

II. PREVIOUS WORK

Different techniques have been proposed to reduce or eliminate the size of input buffers. Initially iDEAL, a low-power area-efficient NoC is achieved by reducing the number of buffers within the router [3]. To overcome the performance degradation caused by the reduced buffer size, adaptive dual-function links is used which is capable of data transmission as well as data storage when required. Other designs targeting power saving with router design have different approaches. A dynamic buffering resources allocation design named ViChaR (Virtual Channel Regulator) focuses on efficiently allocating buffers to all virtual channels, by deploying a unified buffering unit instead of a series of separated buffers, and minimizing the required size [4]. Another approach utilizing channel buffering is the Elastic Channel Buffers (ECB), which replaces the repeaters with flip-flops, and eliminates the router buffers altogether [5]. Other bufferless networks such as FlitBLESS [6, 7] and SCARAB [11] adopt either deflecting or dropping conflicting packets, thereby reducing the latency and power, while sustaining throughput at low network loads while at higher network loads, these networks suffer deflection/dropping leading to an increase in power consumption. In NoC, a router sends packets from a source to a destination router through several intermediate nodes. If the head of packet is blocked during data transmission, the router cannot transfer the packet any more. In order to remove the blocking problem, wormhole routing method is proposed in [8]. The wormhole router splits the packet into several flits which can be transferred in a single transmission. Buffer allocation and flit control are performed at a flit level in wormhole routing since wormhole routing does not allocate available buffer to whole packet [9]. Therefore, the wormhole routing is a method which can minimize overall latency and may decrease buffer size compared to others. In addition, VCs are used to avoid deadlock problem and thus increase throughput. The main purpose of VCs is to decouple the allocation of buffer space to allow a flit to use a single physical channel and competing with other flits.

III. NOC BASELINE ROUTER ARCHITECTURE

A NoC router is implemented using wormhole technique it consists of buffers, switches, and control units which are required to store and forward flits from the input ports to the desired output ports. The architecture is actually similar to that of modern routers, but with smaller area and buffer size .Figure:1 shows a NoC 16 buffer slots per input port. The buffer slots are divided into four queues, and each queue is called a virtual channel (VC) [10]. There are four cardinal input ports and output ports connected from and to +x, -x, +y and- y directions. The last pair of input/output ports is connected from and to the processing element (PE). The four VCs are sandwiched between the de-multiplexer connected to the input port, and the multiplexer connected to the crossbar. Each input unit can communicate with router, virtual-channel allocator, and switch allocator, which are responsible for Routing Computation (RC), Virtual-Channel Allocation (VA), and Switch Allocation (SA), respectively. The crossbar is controlled by the switch allocator for correctly connecting input ports to output ports .

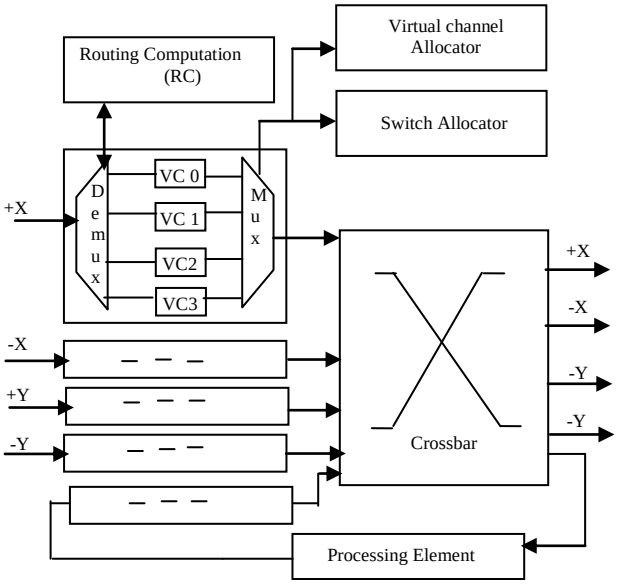

Figure: 1 NoC Router

The virtual channel allocator is to provide a common channel to the requestors for that VA receives neighboring router's virtual channel status and previous router's request signals and then generate virtual channel request signals with an available virtual channel of the next router. Once the virtual channel is allotted then switch allocator will grant the following flits when they arrive at flit buffers. If there are multiple requests, a SA will select the winner in a round-robin fashion for each priority level. Then the winning flit has permission to access crossbar. Crossbar is responsible for physical connection between input ports to its destined output ports, based on the grant.

IV. PROPOSED ROUTER

In proposed router shown in Figure: 2 the advantage of both buffered as well buffer less router are achieved. In order to get the both the advantage dual cross bar is used. At low traffic condition the flit traverse from the first crossbar and at high load condition flit traverse from second crossbar using elastic buffer. There are two crossbars with the primary crossbar having four input ports, the secondary crossbar having five input ports and both of them having five output ports. The four input links are connected to both crossbars via de-multiplexers, and the injection port of the PE is connected to the last input port of the secondary crossbar. . The function of processing element is to give feedback from output to input to show whether the flit is valid or not.The elastic buffer slots are connected serially, thus eliminating VCs and the corresponding virtual-channel allocator. Switch allocator is modified to control the de-multiplexers, the crossbars, and the multiplexers to maintain the correct packet flow in both crossbars. Elastic buffers (EBs) are an efficient flow-control scheme that uses the storage already present in pipelined channels instead of input virtual-channel buffers (VCBs). Removing VCBs reduces the area and power consumed by routers, but prevents the use of virtual-channel.

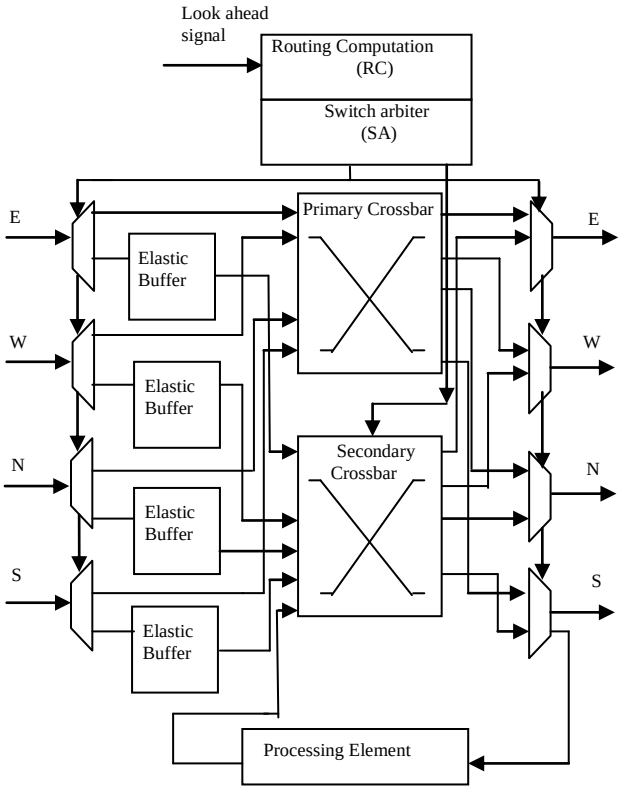

Figure: 2 Proposed Router

Elastic buffer shown in Figure: 3uses a ready-valid handshake to advance a flit (flow-control digit). An upstream *ready* (R) signal indicates that the downstream EB has at least one empty storage location and can store an additional flit. A downstream *valid* (V) signal indicates that the flit currently being driven is valid. A flit advances when both the ready and valid signals between two Elastic Buffers are asserted at the rising clock edge.

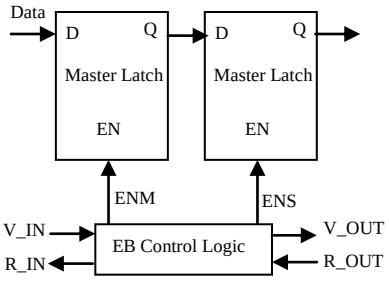

Figure: 3 Elastic Buffer

V. SIMULATION AND RESULT

Implementation is done on DSCH 3.5 and simulation is done on MICROWIND 3.5 at 180 nm. The designing parameters are selected at the time of designing.NoC baseline router and proposed routers are design using the same platform for validation.

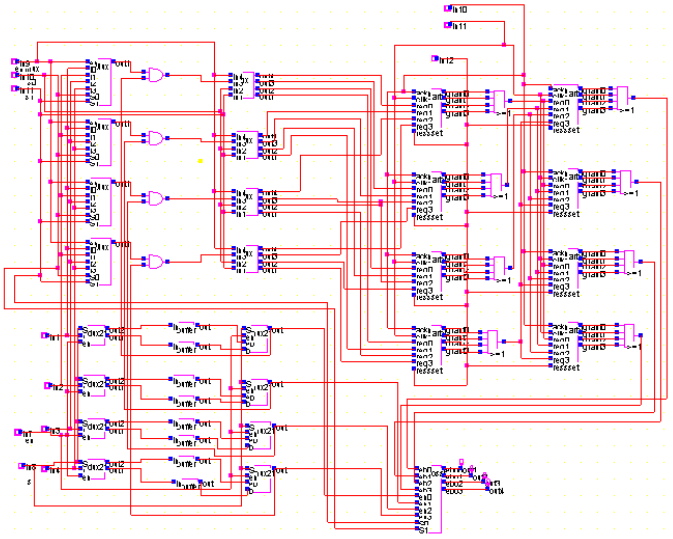

Figure: 4 Base line router on DSCH

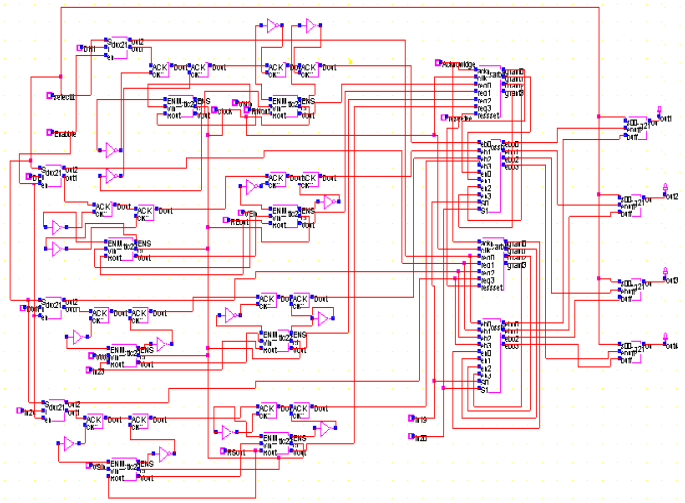

Figure: 5 Proposed router on DSCH

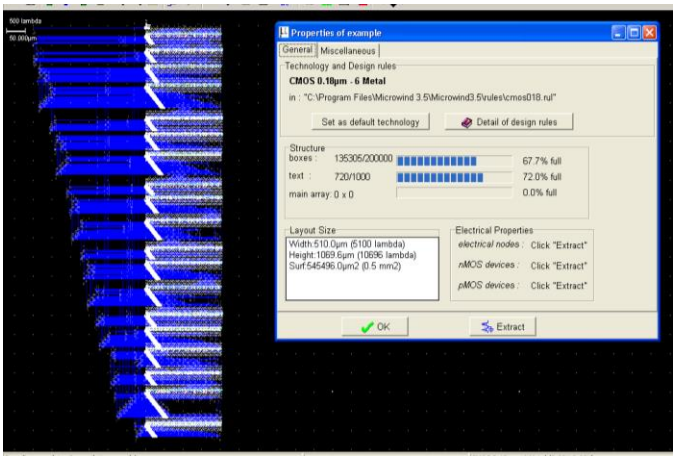

Figure: 6 Base line router area on Micro wind 3.5

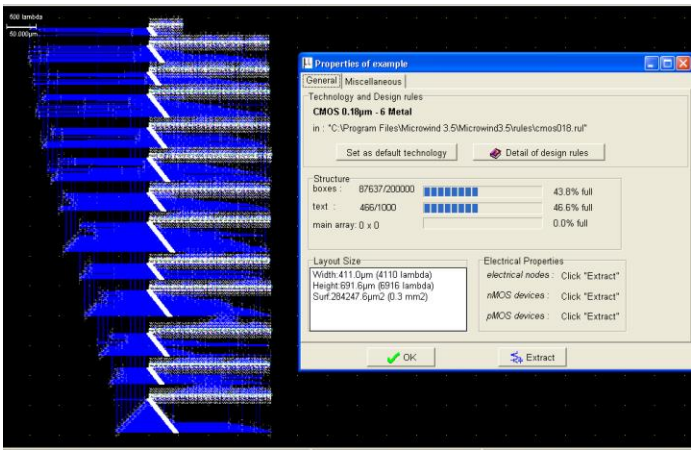

Figure: 7 Proposed router area on Micro wind 3.5

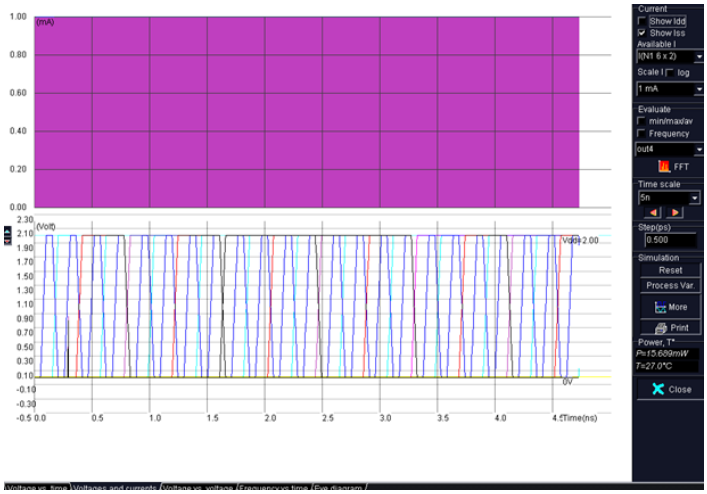

Figure: 8 Analog simulation of Base line router

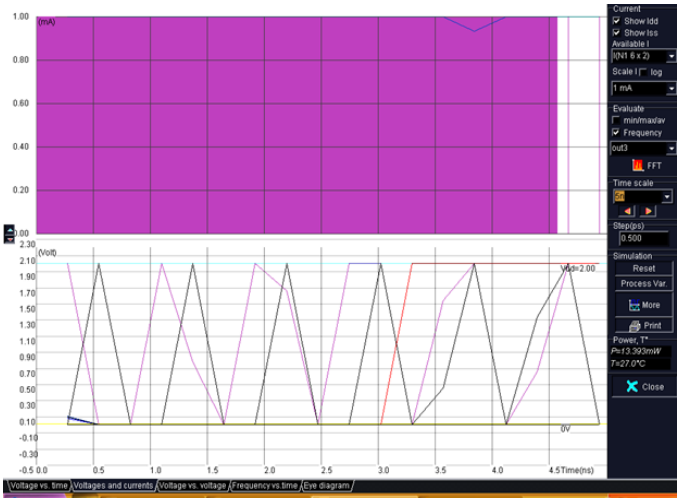

Figure: 9Analog simulation of Proposed router

Table 1 Comparison based on average power and area

Design	Total average power(mW)	Area (mm2)
Baseline router	15.689	545496.0
Proposed router	13.93	284247.6

The power of proposed router reduced to 11.2% and the area of the proposed router reduces by 47.89% compared to the base line router. Figure: 4&5 shows the circuit diagram of both routers. Area is calculated shown in Figure: 6&7 of both routers. Analog simulation of two routers is done as shown in Figure: 8 & 9 respectively. Table 1 shows the comparative analysis of both router in terms of power and area.

VI. CONCLUSION

In this paper we evaluate the performance of dual cross bar router design using elastic buffer with an objective of reducing power and area. The proposed design shows power reduction of 11.2% and area reduction 47.89% compare to baseline router result in increase in performance. With the proposed design we conclude that the advantage of both buffered and buffer less is achieved and single elastic buffer is enough to store a number of flit on each port with saving power when compared to the same number of VC router buffer based NoC architecture.

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