Assessment among Single and Three Phase 14 – Echelon Cascaded Multilevel Inverter

C.Gnanavel[*], N.Kamalamoorthy[**], V. Prabhu[***]

[*] Assistant Professor in EEE, Vivekananda College of Technology for Women
[**] Assistant Professor in EEE, Vivekananda College of Technology for Women
[***] Maharaja Engineering College, Avinashi

Abstract- Multilevel inverters have an attracted a great deal of attenuation in medium voltage and high power application. Due to their lower switching losses, EMI, high efficiency. Among the several multilevel inverters topology it is more attractive due to the simplicity of control. This paper proposes to CHMLI output voltage level is increase to reduced total harmonic Distortion. Hence the paper mainly focused on 14 level multilevel inverter using 12 switches (3H-bridge inverters). The result shows that the proposed method evaluate single and three phase cascaded multilevel inverter effectively minimizes a large number of specific harmonics and reduced switching loss , the output voltage in addition of very low total harmonic distortion. This paper proposed on HCMLI that uses only one power source for each phase. It can produce desired multilevel voltage wave from the multilevel inverter topology can overcome some of its limitations the conventional method. Echelon.

Index Terms- Cascaded Multi level inverter (CHMLI), Total Harmonic Distortion (THD), Pulse Width Modulation (PWM).

I. INTRODUCTION

Modern power semiconductor devices have made the cascaded H-bridge multilevel converter, patented in 1975, practical for use as medium/high-voltage inverters, the output voltage and reduce the undesired harmonics; different sinusoidal pulse width modulation (PWM) and space-vector PWM schemes are suggested for multilevel inverters however, PWM techniques are not able to eliminate low-order harmonics completely. This paper discusses about the cascaded multilevel inverter and how to reduce the Total Harmonic Distortion using the control of switching angle i.e. Conduction angle control method. Conventional 14- echelon pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, lower EMI, lower total harmonic distortion (THD), and others. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters, including the following: multilevel sinusoidal (PWM), multilevel selective harmonic elimination, and space vector modulation.

A typical single-phase echelon inverter adopts full-bridge configuration by using approximate sinusoidal modulation technique as the power circuits. The output voltage then has the following three values: zero, positive (+Vdc), and negative (−Vdc) supply dc voltage (assuming that Vdc is the supply voltage). The harmonic components of the output voltage are determined by the carrier frequency and switching functions. Simulation and experimental results are presented to validate the proposed inverter configuration.

This paper presents a single& three-phase 14-echelon inverter topology for dc systems with a novel Pulse width-modulated (PWM) control scheme. In our project HBMLI is used. It is main reason to simplicity of control and a cascade multilevel inverter is built to synthesize a desired AC voltage from several levels of DC voltages. Though the cascaded has the disadvantage to need separate dc sources the problem of the dc link voltage unbalancing does not occur, thus easily expanded to multilevel. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors.

The result shows that the proposed method effectively minimizes a large number of specific harmonics, and the output voltage result in very low total harmonic distortion and switching frequency. In our project HBMLI is used

II. EXISTING TECHNOLOGY

In conventional method they are used 11- level Inverter with 5 H-Bridge circuits. By using this method inverter offers high total harmonic distortion.

III. PROPOSED TECHNOLOGY & BLOCK DIAGRAM

In proposed method we implied a 14- echelon Inverter with 3 H-Bridge circuits. By using this proposed idea it minimizes the high total harmonic distortion through the appending of echelons. In this paper both single and three phase total harmonic distortion has minimized.

A cascaded multilevel inverter consists of a series of H-bridge (single phase, full bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or solar cells. Figure shows the basic structure of a single phase cascaded inverter with SDCSs. Each SDCS connected to an H bridge inverter. The ac terminal voltages of different level inverters are connected in series. Unlike the diode clamped or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors.

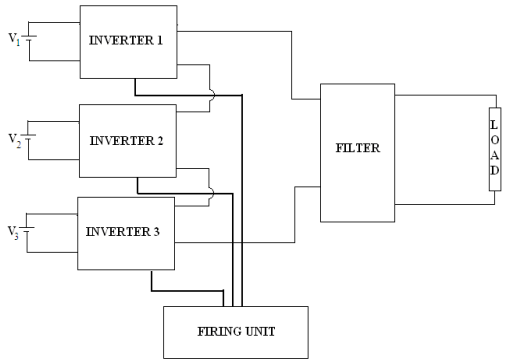

Fig 3.1 Block Diagram

One multilevel inverter topology incorporates cascaded single-phase H-bridges with separate dc sources (SDCSs) from the transformer secondary. This requirement makes renewable energy sources such as fuel cells or photovoltaic a natural choice for the isolated dc voltage sources needed for the cascade inverter. Fig shows a single-phase structure of an m-level cascade inverter. Each SDCS is connected to a single phase full-bridge, or H-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$, by connecting the dc source to the ac output by different combinations of the four switches one of the main advantages of the cascaded inverter is that the series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and inexpensively. Also, redundant voltage levels can be included in an application design so that the inverter can still operate even with the loss of one level. This enables the multilevel inverter to continue to function even when there is a problem with one of the dc sources or with one of the power electronics devices that make up the H-bridge.
This paper discusses about the cascaded multilevel inverter and how to reduce the Total Harmonic Distortion using the control of switching angle i.e. Conduction angle control method.

Multilevel inverter is constructed depends on the number of echelons. Totally it requires (m-1) capacitors and 2 (m-1) switches for the construction of m level inverters. And also it needs 2 (m-1) (m-2) diodes to clamp the voltage at various level of voltage. Gate signal is generated using the comparator. The ramp signal is compared with DC voltage. By adjusting the DC magnitude the pulse width is controlled. Here the lower switch conducts for long time than the upper switch.

IV. Proposed Maneuver

This paper presents a new control method for the cascaded H-bridge multi-level inverter. Although the proposed method results in a slight reduction in voltage levels, only one isolated dc source per phase is required. This reduces the inverter cost and complexity. This new method is first applied to the traditional cascaded H-bridge inverter for two and three cells per phase. The control is then applied to an inverter with multi-level cells. A joint-phase redundancy technique is also explored for extending the power quality of the proposed technique

A cascaded multilevel inverter consists of a series of H-bridge (single phase, full bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs) from transformer secondary, which may be obtained from batteries, fuel cells, or solar cells. Figure4.2 shows the basic structure of a single phase cascaded inverter with SDCSs. Each SDCS connected to an H bridge inverter. The ac terminal voltages of different level inverters are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors.

Among three types of topologies, the proposed paper topology is cascaded multi level inverter method. In this method, the diode clamps the voltage across the switch to one level. And all diodes are selected as same type. i.e. same voltage withstanding capacity. The diode provides the forward path and feedback path to the current.

V. Modes of Operation

The operation of echelon inverter is explained in different modes. During each mode what are devices are in on and off condition. There are totally 14 modes for full cycle operation. But for half cycle there are seven modes. i.e. To produce the positive half cycle of output voltage leg A operation of single phase inverter is explained. The remaining negative half cycle operation is for leg B.

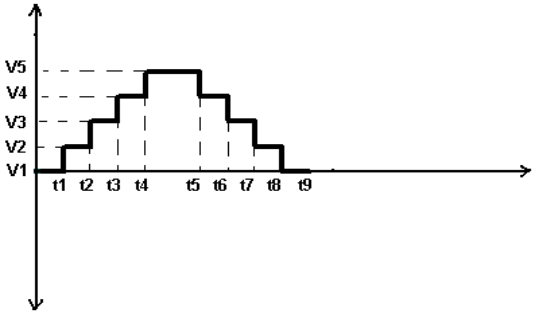

Figure5.1 output voltage waveform to explain the modes of operation

Mode 1 (0 < t < t1)

In this mode the output voltage is zero. No devices of upper arm of leg A are turned on. But lower arm switches are in on condition. So the output voltage across the load is zero and equal to V_1. And all switches of lower arm of leg B are in on condition.

The circuit diagram shows the five level diode clamped inverter with separate DC sources instead of capacitors.

Mode 2 (t1 < t < t2)

In this mode the switch in upper arm Ma1 is switched on and M_{A1} in lower arm is switched off. So the output voltage is equal to V_2. The current flows from the lower diodes D_5, D_9 and D_{11} and through switch M_{a1} to load. And all switches of lower arm of leg B are in on condition.

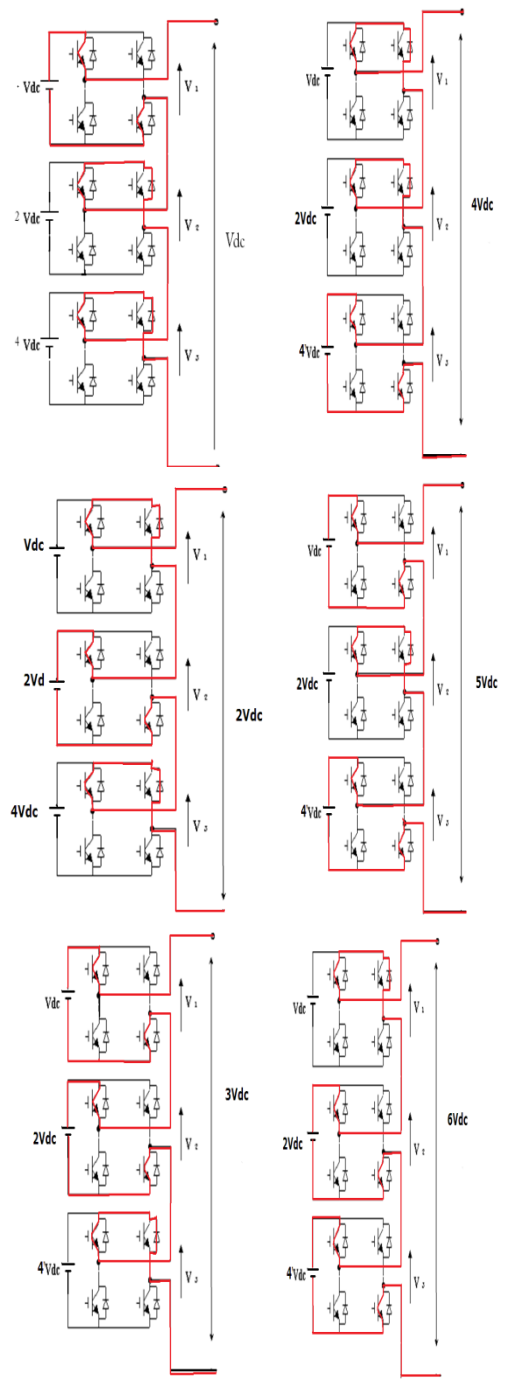

Figure 5.2 Positive and Negative Mode of Operation mode 1 operation **(0 < t < t1)**, Mode 2 operation, **(t1 < t < t2),** Mode 3 operation **(t2 < t < t3)**, Mode 4 operation **(t3 < t < t4)**, Mode 5 operation **(t4 < t < t5)**, Mode 6 operation **(t5 < t < t6)**, **Mode 6(t5 < t < t6)**

In this mode the switches in upper arm $Ma_1$and Ma_2 are switched on and MA1 & M_{A2} in lower arm are switched off. So the output voltage is equal to V_3. The current flows from the diodes D_8, D_7 and through switch Ma1&Ma2 to load. And all switches of lower arm of leg B are in on condition.

Mode 4 (t3 < t < t4)

In this mode the switches in upper arm M_{a1}, M_{a2} and M_{a3} are switched on and $_{MA1,}$ M_{A2} & M_{A3} in lower arm are switched off. So the output voltage is equal to V_4. The current flows from diode D_1 through switches M_{a1}, M_{a2} & M_{a3} to load. And all switches of lower arm of leg B are in on condition.

Mode 5 (t4 < t < t5)

In this mode the all switches in upper arm M_{a1}, M_{a2}, M_{a3} and M_{a4} are switched on and M_{A1}, M_{A2}, M_{A3} & M_{A4} in lower arm are switched off. So the output voltage is equal to V_5. The current flows from the through switches M_{a1}, M_{a2}, and M_{a3} & M_{a4} to load. And all switches of lower arm of leg B are in on condition.

Mode 6 (t5 < t < t6)

In this mode the switches in upper arm M_{a1}, M_{a2} and M_{a3} are switched on and M_{A1}, M_{A2} & M_{A3} in lower arm are switched off. So the output voltage is equal to V_4. The current flows from diode D_1 through switches M_{a1}, M_{a2} & M_{a3} to load. And all switches of lower arm of leg B are in on condition.

Mode 7 (t6 < t < t7)

In this mode the switches in upper arm $M_{a1}$and M_{a2} are switched on and M_{A1} & M_{A2} in lower arm are switched off. So the output voltage is equal to V_3. The current flows from the diodes D_8, D_7 and through switch M_{a1}&M_{a2} to load. And all switches of lower arm of leg B are in on condition.

Mode 8 (t7 < t < t8)

In this mode the switch in upper arm M_{a1} is switched on and M_{A1} in lower arm is switched off. So the output voltage is equal to V_2. The current flows from the lower diodes D_5, D_9 and D_{11} and through switch M_{a1} to load. And all switches of lower arm of leg B are in on condition

Mode 9 (t8 < t < t9)

In this mode the output voltage is zero. Because all devices of upper arm of leg A are turned off. But lower arm switches are in on condition. So the output voltage across the load is zero and equal to V_1. And all switches of lower arm of leg B are in on condition.

5.1Principle of Operation

A cascaded multilevel inverter consists of a series of H-bridge (single phase, full bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from batteries, fuel cells, or solar cells. Figure 4.3 shows the basic structure of a single phase cascaded inverter with SDCSs. Each SDCS connected to an H bridge inverter. The ac terminal voltages of different level inverters are connected in series. Unlike the diode clamp or flying capacitors inverter, the cascaded inverter does not require any voltage clamping diodes or voltage balancing capacitors.

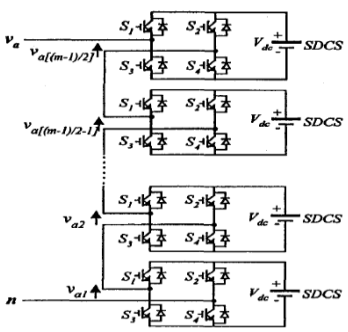

Fig 5.1 Single-phase structure of a multilevel cascaded H-bridges inverter

One multilevel inverter topology incorporates cascaded single-phase H-bridges with separate dc sources (SDCSs) from the transformer secondary. This requirement makes renewable energy sources such as fuel cells or photovoltaic a natural choice for the isolated dc voltage sources needed for the cascade inverter. Fig 5.1 shows a single-phase structure of an m-level cascade inverter. Each SDCS is connected to a single phase full-bridge, or H-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$, by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3,and S_4,.

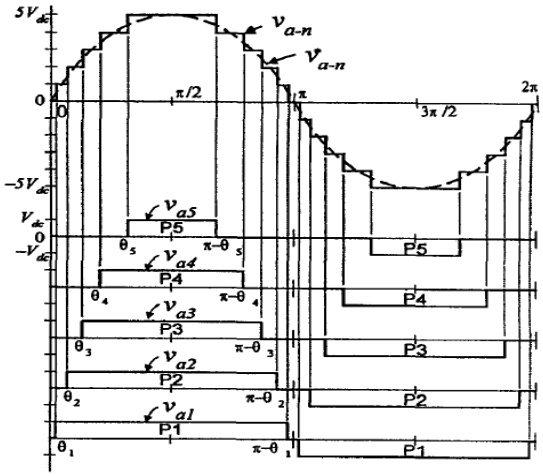

Fig 5.2 Waveforms and switching method of the 14-level cascade inverter.

To obtain $+V_{dc}$, switches S_1 and S_4 are turned on. Turning on switches S_2 and S_3 yields $-V_{dc}$. By turning on S_1 and S_2, or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels *m* in a cascade inverter is defined by m = 2s+l, where s is the number of separate dc sources (photovoltaic modules or fuel cells). An example phase voltage waveform for an 14- level cascaded H-bridge inverter with *5* SDCSs and *3* full bridges is shown in Fig 4.3.1phase voltage $V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5}$. The output voltage of the inverter is almost sinusoidal, and it has less than 5% total harmonic distribution (THD) with each of H Bridge switching only at fundamental frequency.

The conducting angles, θ_1, θ_2,….. θs. can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics.

For the 14-level case in Fig. the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics can be eliminated with the appropriate choice of the conducting angles. From Fig.5.2, note that the duty cycle for each of the voltage levels is different. If this same pattern of duty cycles was used continuously, then the level of voltage source would be required to generate much more power than the level-5 voltage source.

VI. Harmonic Analysis

The proposed system analyses the frequency spectrum and voltage control. In conduction angle control the lower order harmonics are reduced. By adjusting the turn on angle to various levels, it is possible to reduce the lower order harmonics and the efficiency, power factor is improved. The Fourier expression is also obtained for the output voltage of five-level inverter.
For 14-echelon inverter

$$V_o(wt) = \sum_{n=1,3,5\cdots}^{\alpha} (4Vdc/n\Pi)(\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_3 + \cos n\alpha_4) \sin n\theta \quad \ldots\ldots\ldots 5.3$$

Where V_{dc} is the supply dc voltage.

In the above expression there are four angles related to output voltage. So it is possible to reduce four odd harmonics. Because even harmonics are not present in output voltage. But our aim is to control the output voltage and reduction of harmonics. From the above expression four equations are formed and the four angles are found.

If the no of levels are increased it is not easy to find the switching angles to remove particular order of harmonics. For that elimination theory is used. The modulation index is chosen as 0.8 for low THD. In 14- level inverter, to reduce the LOH from the output voltage, the turn-on angles are calculated from the output voltage equation. To reduce the lower order harmonics 5^{th}, 7^{th} and 11^{th} in the proposed system, the conduction angle is found by solving the following equation.

VII. Proposed Harmonic Reduction Technique

There are four equations to find the angles to reduce LOH especially 5^{th}, 7^{th} and 11^{th} in the output voltage. At the same time we can control the required output RMS voltage using the equation 5.4The other equations5.5, 5.6and 5.7are used to reduce the fifth, seventh and eleventh order harmonics. Totally the THD is reduced.

The four equations are

$$\cos\alpha_1+\cos\alpha_2+\cos\alpha_3+\cos\alpha_4 = m \quad \ldots\ldots\ldots 7.1$$
$$\cos 5\alpha_1+\cos 5\alpha_2+\cos 5\alpha_3+\cos 5\alpha_4 = 0 \quad \ldots\ldots\ldots 7.2$$
$$\cos 7\alpha_1+\cos 7\alpha_2+\cos 7\alpha_3+\cos 7\alpha_4 = 0 \quad \ldots 7.3$$
$$\cos 11\alpha_1+\cos 11\alpha_2+\cos 11\alpha_3+\cos 11\alpha_4 = 0 \quad .7.4$$

Using MathCAD program, the conduction angles were found to satisfy the above equations and they are
$\alpha_1 = 12.834^o$; $\alpha_2 = 29.908^o$; $\alpha_3 = 50.993^o$; $\alpha_4 = 64.229^o$;
The total harmonic distortion is defined as

$$THD = \frac{\sqrt{(V_3^2 + V_5^2 + V_7^2 + \ldots\ldots V_{31}^2)}}{V1} \quad 7.5$$

VIII. Simulation Results

The simulation result shows that the developed 14-echelon PWM inverter has many merits such as reduces number of switches, lower EMI, less harmonic distortion and the THD of

the proposed inverter is consider by alleviated and the dynamic response are also improved significantly.

The simulation result proposed to minimize the THD. With using of reduced low number switches. The voltage of DC link for each H-bridge units is considered to be $V_1 < V_2 < V_3$, and simulation is done The simulation result shown in single & three phase and compare THD .the simulation result shows that FFT Analysis to find the THD. The first simulation result was minimizing single phase 14 – level HCMLI the THD level was 15.16%. The Second Simulation result was minimizing three phase 14 – level HCMLI the THD level was 13.74%. So three phase total harmonics distortion is very less 1.42%. Main advantages of project thus proposed inverter involves many advantages over the convention inverter.

The study can further be investigated by employing control schemes to have higher dynamic response and by using high level inverters.

8.1 Simulation Model (1Φ)

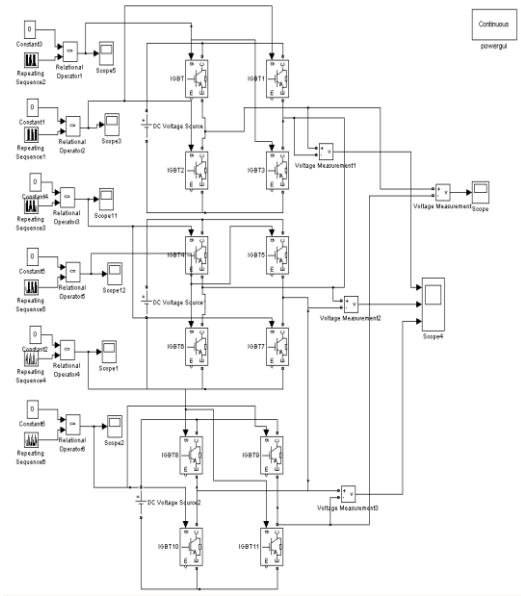

Fig 8.1 Single Phase 14 –echelon Cascaded Multilevel Inverter

8.2 Simulation Output Diagram

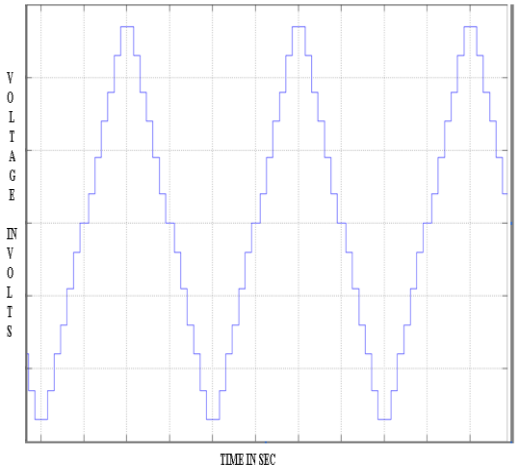

Fig8.2Simulation Output

8.3 TOTAL HARMONIC DISTORTION (1Φ)

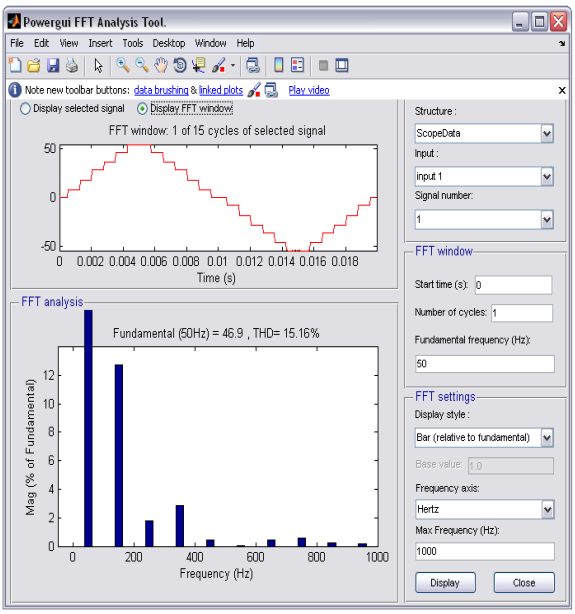

Fig 8.3 Total Harmonic Distortion (THD)

8.4 Simulation Model (3 Φ)

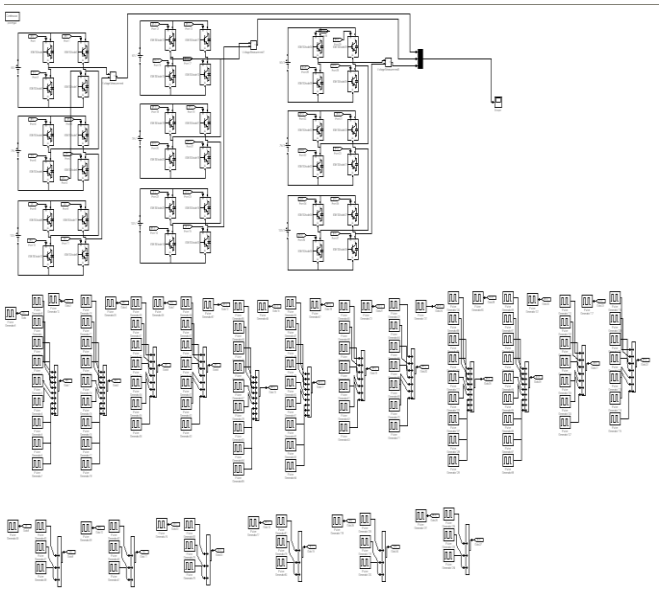

Fig 8.4 Three Phase 14 –level CMLI

8.5 Simulation Output Diagram (3ϕ)

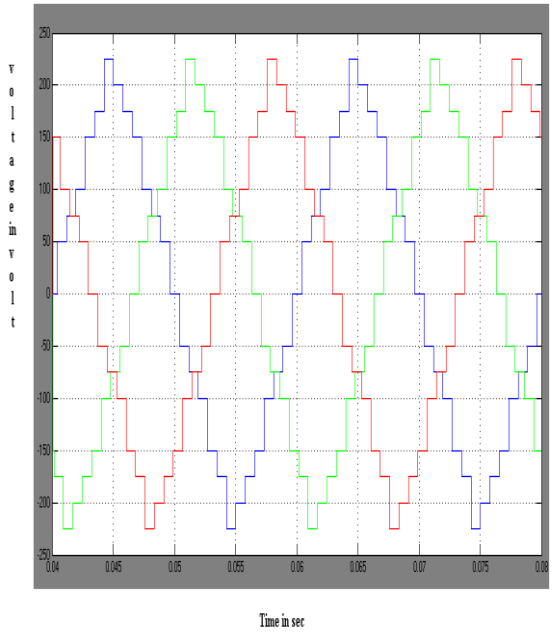

Fig 8.5Simulation Output Diagram (3Φ)

8.6 Total Harmonic Distortion (3 Φ)

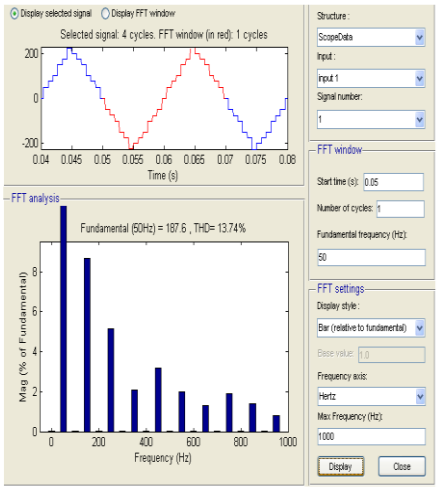

Fig 8.6Total Harmonic Distortion (3Φ)

s.no	Order of Harmonics	Frequency in HZ	Harmonics in%
1.	3rd	150	12.07%
2.	5th	250	1.95%
3.	7th	350	2.84%
4.	9th	450	0.41%
5.	11th	550	0.06%
6.	13th	650	0.41%
7.	15th	750	0.55%
8.	17th	850	0-22%
9.	19th	950	0.17%
		TOTAL	15.16%

Table:1 Single phase 14 echelon CMLI

Three Phase 14-Echelon CMLI

s. no	Order of Harmonics	Frequency in HZ	Harmonics in%
1.	3rd	150	11.70%
2.	5th	250	1.73%
3.	7th	350	0.44%
4.	9th	450	0.21%

5.	**11th**	**550**	**0.06%**
6.	**13th**	**650**	**0.41%**
7.	**15th**	**750**	**0.10%**
8.	**17th**	**850**	**0.22%**
9.	**19th**	**950**	**0.02%**
		TOTAL	**13.74%**

Table: 2Three phase 14 echelon CMLI

IX. Conclusion

This paper is mainly focused on, to reduce Total Harmonic Distortion (THD*)* and number of switch& improve output voltage level. In conventional method, used 11- echelon Inverter with 5 H-Bridge circuits. In proposed method we implied a 14-echelon Inverter with 3 H-Bridge circuits. By using this proposed idea it minimizes the high total harmonic distortion through the appending of echelons. In this paper both single and three phase total harmonic distortion has minimized. Simulation result is providing for a 14-level cascade H-bridge inverter to validate the accuracy of computational result. Single and Three phase simulation result was minimizing 14 – level HCMLI the THD level was 15.16%&13.74%. Comparison of result with active harmonics elimination techniques shows that the total harmonics distortion and switching frequency of output voltage decreased dramatically

References

[1] Mehdi Abolhassani, Senior Member, IEEE, "Modular Multipulse Rectifier Transformersin Symmetrical Cascaded H-Bridge Medium Voltage Drives"IEEE transactions on power electronics, vol. 27, no. 2, February 2012

[2] Ayoub Kavousi, Behrooz Vahidi, Senior Member, IEEE, Reza Salehi, Mohammad Kazem Bakhshizadeh,Naeem Farokhnia, Student Member, IEEE, and S. Hamid Fathi, Member, IEEE ,"Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters. IEEE transactions on power electronics, vol. 27, no. 4, April 2012 "

[3] Zhengming Zhao, Senior Member, IEEE, Yulin Zhong, Hongwei Gao, Senior Member, IEEE, Liqiang Yuan, Member, IEEE, and Ting Lu, Member, IEEE, "Hybrid Selective Harmonic Elimination PWM for Common-Mode Voltage Reduction in Three-Level Neutral-Point-Clamped Inverters for Variable Speed Induction Drives" IEEE transactions on power electronics.

[4] Nima Yousefpoor, Seyyed Hamid Fathi, Member, IEEE, Naeem Farokhnia, Student Member, IEEE, and Hossein Askarian Abyaneh, Senior Member, IEE"THD Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters".IEEE transactions on industrial electronics, vol. 59, no. 1, January 2012 373

[5] Youssef Ounejjar, Member, IEEE, Kamal Al-Haddad, Fellow, IEEE, and Louis A. Dessaint, Senior Member, IEEE"A Novel Six-Band Hysteresis Control for the Packed UCells Seven-Level Converter:Experimental Validation", IEEE transactions on industrial electronics, vol. 59, no. 10, October 2012

[6] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," IEEE Trans. Ind. Appl., vol. 32, no. 3, pp. 509–517, May/Jun.1996.

[7] J. Rodr´ıguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," IEEE Trans. Ind. Electron., vol. 49,no. 4, pp. 724–738, Aug. 2002.

[8] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converter for large electric drives," IEEE Trans. Ind. Appl., vol. 35, no. 1, pp. 36–44,Jan./Feb. 1999.

[9] J. Wang and F. Z. Peng, "Unified power flow controller using the cascade Multilevel inverter," IEEE Trans.Power Electron., vol. 19, no. 4, pp. 1077–1084, Jul. 2004.

[10] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," IEEE Trans. Ind. Appl., vol. 35, no. 5, pp. 1098–1107,Sep./Oct. 1999.

[11] M. Calais, L. J. Borle, and V. G. Agelidis, "Analysis of multi carrier PWM methods for a single-phase five-level inverter," in Proc. 32nd Annu. IEEE PESC, Jun. 17–21, 2001, vol. 3, pp. 1173–1178.

[12] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in Proc. 22nd Annu. IEEE PESC, Jun. 24–27, 1991,pp. 96–103.

[13] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," IEEE Trans. Power Electron., vol. 7, no. 3, pp. 497–505, Jul. 1992.

[14] A. Nabae and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[15] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in fourlevel Diode-clamped converters with passive front end," IEEE Trans. Ind.Electron., vol. 52, no. 1, pp. 190–196, Feb. 2005.

[16] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," IEEE Trans. Ind. Electron., vol. 53, no. 5,pp. 1504–1511, Oct. 2006.

[17] A. Nabae and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

Authors

First Author – Gnanavel .C was born in Erode in May 23rd, 1986. He graduated in 2007 from Anna University, Chennai and post graduated in 2010 from Anna University of technology, Coimbatore. He has 3 national conference papers to his credit and He has published two journals. Journal of Global Research in Computer Science and International journal of advanced information sciences and technology. His currently working as Assistant Professor in the department of EEE at Vivekanandha College of Technology, Namakkal., Email Id: gnana2007@gmail.com

Second Author – **N.KamalaMoorthy** received his Bachelors Degree in Electrical and Electronics Engineering from Anna University, Chennai, India in the year 2008.and Masters Degree in Control and Instrumentation Engineering from Anna University of Technology, Coimbatore, India in the year 2011. He is currently pursuing his Ph.D. at Anna University, Chennai. His research interest includes optimization of power system operation, dispersed generation and energy storage. At present, he is affiliated with the Center for Advanced Research, of Vivekanandha College of Technology for women, Tiruchengode. He has authored over 10 research papers in various International/National conferences, Journals and symposiums. His areas of interest include Transmission and Distribution,

Renewable energy resources, Power electronics. Email Id: erkamaleee@gmail.com

Third Author –

V.Prabhu was born in Erode in March 10th, 1983. He received his Bachelors Degree in Electrical and Electronics Engineering from Anna University, Chennai, India in the year 2006 and Masters Degree in Power Electronics Drives from Anna University of Technology, Coimbatore, India in the year 2010. He has authored over 7 research papers in various International/National conferences, Journals and symposiums. His areas of interest include Electrical Machines, Power electronics, Electronic Devices & Circuits . He currently working as Assistant Professor in the department of EEE at Maharaja Engineering College, Aviashi, Tamilnadu. Email Id: prabhuveeramani@gmail.com