VLSI Using CMOS Fabrication

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Abstract- "VLSI stands for "Very Large Scale Integration, which is the capability of semiconductor to fabricate many MOS family transistor into single silicon chip. CMOS is referred as "Complementary Metal Oxide Semiconductor" which is the technology of fabricating the n-type and p-type MOSFETs side by side on the same silicon substrate to construct a VLSI circuit. It has capability of developing both digital as well as analogue based applications. There are three types of materials used to design CMOS VLSI circuits. They are insulator, conductors and semiconductors. The paper also enlightens the fabrication process sequence which involves following steps silicon manufacture, wafer processing, lithography, oxidation, diffusion, ion implantation,deposition, metallization, testing and packing. The main advantages of this technology are CMOS possess very high input impedance and the outputs are significantly high. The VLSI Technology is currently a booming technology which has changed the electronic world."

I. INTRODUCTION

VLSI stands for *"**V**ery **L**arge **S**cale **I**ntegration"* which reflects the capability of semiconductor to fabricate more than 1000 MOS family transistor into a single silicon chip. The growth of VLSI technology is best described by *"Moore's Law"*. As per the Moore's law the number of transistor doubles every 18 months. The technology has decrease the device size with increasein number of gates or MOSFET in single IC.

Fabrication is the process of creating integrated circuits (ICs) which realize electronic circuits. It involves multiple steps of photolithographic along with chemical process to gradually create circuits on a wafer made of pure semiconductor. The MOS fabrication processes are

- ***N-type MOS (nMOS)***

In this process IC is built with n-type source and drain and a p-type substrate in which electrons are carrier. On a high voltage at gate, IC will conduct and on a low voltage at gate, IC does not conduct. The IC built by N-type MOS fabrication are faster than P-type fabrication, since the carriers are electrons that travels twice as fast as holes.

- ***P-type MOS (pMOS)***

In this process IC is built with p-type source and drain and a n-type substrate in which holes are carrier. On a high voltage at gate, IC does not conduct and on a low voltage at gate, IC will conduct. The IC built by P-type MOS fabrication are more immune than N-type fabrication.

- ***Complementary MOS (CMOS)***

CMOS uses complementary and symmetrical pairs of p-type and n-type MOSFETs.

The paper is organised as follows: Section I deals with CMOS Technology. Section II deals with Fabrication Materials, Section III illustrates CMOS fabrication technique and Section IV deals with Fabrication sequence. The Section V describes the advantage of VLSI and Section VI draws a brief summary of the paper.

II. CMOS TECHNOLOGY

CMOS is referred as *"**C**omplementary **M**etal **O**xide **S**emiconductor"*which is the technology of fabricating the n-type and p-type MOSFETs side by side on the same silicon substrate. CMOS ICs composed up to billions of transistor of both n-type and p-type on a piece of rectangular silicon substrate of 10 to 40 mm^2.

The characteristics of CMOS are high noise immunity, low propagation delay and low static power consumption.

Firstly, propagation delay is short as delay is in order of 20 to 50 ns depending upon the supply voltage. Secondly, CMOS devices are low power consumption devices, since one transistor pair is always off and its draws significant amount of power during switching between on and off states. It also allows high density of functions in a chip.

CMOS technology develops both digital as well as analog based applications. In digital world this technology is used in microprocessor, microcontroller, static RAM, etc. While in analog field CMOS is used to design image sensor, data converters, transceiver, etc.

III. FABRICATION MATERIALS

There are three types of materials used to design CMOS VLSI circuits. They are as follows:

- *Insulator:* They are used to isolate semiconducting or conducting materials from each other that are present in VLSI circuits. Insulator requirements depends upon the functionality of material used in designing of ICs.*E.g.: Silicon Nitride, Silicon Dioxid*e
- *Conductors*: They are used in VLSI for electrical connectivity. Conductors are used as a local as well as global interconnects. *E.g.: Silver, Gold*
- *Semiconductors*: They are the base of VLSI structure and used for formation of device. The conductivity of semiconductors are varied through selective doping depending upon the application of voltage. *E.g.: Silicon*

IV. CMOS Fabrication Technology

In CMOS fabrication both the p-type and n-type MOSFETs are arranged in such a manner that the p-type acts as a pull-up network and n-type acts as pull down network. This fabrication technology has become dominant due to its high performance and cost effective VLSI.

There are various approach for fabrication of VLSI.

- *p-well Process*

In p-well structure an n-type is used as substrate in which p-devices are formed bysuitable masking and diffusion. In order to accommodate the n-type devices, a deep p- well is diffused into the substrate. Since p-well concertation affects the threshold and breakdown voltages of n-transistor a deep diffusion is required. Here the p-well acts substrate to n-type devices within the main n-type substrate.

Deep p-well Diffusion process

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Accommodation of n-type and p-type transistors on thinox layer

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Pattern of Polysilicon layer is deposited

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p-diffusion

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n-diffusion

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Contacts are defined

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Metal layer is defined

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Passivation layer is applied for accessing the bonding pads

- *n-well Process*

The n-well regions are created for p-type MOSFET transistors, by impurity implantation into the substrate. This technology is also popular due to its lower substrate bias effect on threshold voltage of transistors.the disadvantage of n-well is that it degrades the performance of p-type transistor.

Formation of n-well region

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Define nMOS and pMOS active areas with polysilicon pattern

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Field and gate oxidations

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p diffusion

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n-diffusion

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Contacts are defined

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Metal layer is defined

Passivation layer is applied for accessing the bonding pads

- *Twin tub process*

It is basically a logical extension of p-well and n-well processes. In this process a high restive n-type transistor is used in which both the p-well and n-well are created. This process has preserved the performance of n-type transistor without compromising the p-type transistor.

- *Silicon on Insulator*

As the name suggests it is technology in which transistors are fabricated on insulator directly. The insulators used is silicon oxide or sapphire. The advantages of SOI are that it possesslow parasitic delay and consumes low dynamic power.

In above all the processes that we have seen, the p-well process is widely used in practice.

V. Fabrication Process Sequence

Silicon Manufacture

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Wafer Processing

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Lithography

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Oxidation

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Diffusion

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Ion Implantation

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Annealing

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Deposition

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Metallization

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Testing

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Packing

Fabrication Sequence

Silicon Manufacturing

In basic process the silica and coke is heated in submerged arc furnace to high temperature. This high temperature removes oxygen leaving behind the silicon. As it is forms it displaces the carbon, this process is called as reduction process.

Wafer Processing

The produced silicon is melted at 1500 ^{0}C in crucible where seed crystal is bought in contact which is withdrawn slowly from

molten silicon. As it is withdrawn the silicon atoms get attach with cool seed forming crystalline structure. With control doping the concentration of n-type and p-type impurity is maintained. This silicon are then manufactured in shape of cylinder of diameter 8-12 inch which is sawed into thin disks of thickness 0.5-0.75mm. This disks are called silicon wafer.

Lithography

The silicon wafer is cleaned and is covered with barrier layer of silicon dioxide with photoresist layer. The photoresist is a photosensitive layer which becomes soluble when exposed to light. The prepared silicon wafer is the substrate on which VLSI circuits are built by soft baking the wafer to set layers. The mask is a plate with design of desired layers of VLSI circuits and this several masks are used to create different feature of VLSI. The layout from mask to wafer is transferred through a wavelength limited light. The lens resolves the layout image created by light into smaller images and this images are reflected on the photoresist layer. The parts of the photoresistexposed to light are washed away, leaving unexposed regions on the wafer. The wafer is then hard baked to set theremaining photoresist. The SiO2 layer is removed by etching from the exposed regions and along with it the remaining photoresist is removed. This entire process is termed as Lithography.

Oxidation

The process of growth of oxide layer on wafer in a high temperature furnace is termed as oxidation. This process are of two types

- Dry Oxidation is an oxidation process in which oxygen is mixed with small amount of hydrochloric acid to give thin oxide layer known as gate oxide layer as these layers are used to form gate structure.
- Wet Oxidation is an another process in which oxygen along with water vapour is mixed with silicon to give a thicker oxide layer called as field oxide layer

Diffusion

The movement of atoms from a high concentration region to low concentration region is termed as diffusion process. In VLSI this process is used to dope impurities in silicon at very high temperature (1000 to 1200 ^{0}C) in order to increase conductivity. The dopants used are boron, phosphorous and arsenic. The penetration of this dopants depends on temperature and processing time.

Ion Implantation

It is another method to dope impurities in semiconductor. In the following process the dopants are ionized at room temperature and this ionized atoms are accelerated between two electrodes at potential difference of 150kV. The atoms then hits the silicon substrate with high velocity and penetrate into the wafer. Here the penetration of ionized atoms depends on accelerating voltage and quantity is controlled by flow of ions. This method is used for control doping of impurities in VLSI.

Annealing

A process in which the wafer is heated and cool down slowly in order to remove the internal stress and remove damage caused due collision of ion during ion implantation process. The process in which the lattice is re-crystallize and becomes stable is termed as annealing.

Deposition

Deposition process is a process of formation of solids on wafer by chemical reaction of gases and vapors.

In VLSI fabrication the conducting layer, insulation layer and protective layer are created on wafer by use of chemical deposition technique which is carried out in a high temperature chamber. The conducting layer such as polysilicon is deposited when silane is heated at 1000 ^{0}C and the insulation layer i.e. silicon dioxide and silicon nitride are deposited by heating it with oxygen and ammonia at 400-700 ^{0}C.

Metallization

Metallization is basically a process in which metals are deposited on entire silicon wafer. The main idea of metallization is to interconnect various electronic component such as transistor, diodes etc. together to form desired VLSI circuit. Sputtering process through which metal layer are deposited.

Testing

Testing is a manufacturing step through which the correctness of fabricated VLSI circuits are verified. The testing also helps in diagnosing the faulty site (if present any). This is carried out in two process

- Test Generation: Software testing
- Test Application: Hardware testing

Thus, it is an important step as it is a quality check of fabricated VLSI circuit before the final packing.

Packing

After being tested the VLSI fabrication process moves to its final stage where the verified circuits are mounted on packages. This verified circuits are termed as dies and the pins of package are interconnected to the die through fine gold wire. Finally, in an inert atmosphere the packages are sealed using plastic or epoxy.

VI. Advantages

- CMOS possess very high input impedance
- The output of CMOS actively drive in both the direction.
- The outputs are pretty much rail-to-rail.
- CMOS logic circuit consumes very less power when operated in a fixed state.
- CMOS gates are simple. The basicgate in CMOS is an inverter, which consist only of two transistors.

VII. Conclusion

The VLSI Technology is currently a booming technology which had created a new era of electronic miniaturization and this evolution in electronic world is enhancing day by day. CMOStechnology has claimed the predominant position in

modern electronic system. It has enabled the active use of microprocessors, communication system and many others electronic devices with smaller size and higher efficiency rate. This growth is clearly seen through rapid fabrication of millions and billions transistor on single silicon chip.

The paper introduces the steps through which a VLSI circuits are developed using the CMOS Fabrication technology which relatively provides high performance VLSI circuit with a low power consumption and small size. The fabrication technique used in following paper is very efficient due to its characteristics and design simplicity.

The future of VLSI circuits is bright and will only flourish in coming years.

REFERENCES

[1] Ashwini Dhawane and PratikshaNichhal*"VLSI and Fabrication"*presentedinWorld Research Journal of Telecommunications Systems in 2012

[2] Appendix A *"VLSI Fabrication Technology"* reprinted in Oxford University Press 2015

[3] Jin Fu Li *"Chapter 6 VLSI Testing"* in National Central University, Taiwan

[4] Roger T. Howe*"Lect.4 IC Fabrication Process"* in EE 105 Springer 1997, University of California, Berkeley

[5] Jagjot Singh &Jeeyun Kim *"Lithography"* in Feb 2004

[6] Neil H. E. Weste and David Money Harris *"CMOS VLSI Design A Circuits and Systems Perspective"*copyright © 2011, 2005, 1993, 1985 Pearson Education, Inc., publishing as Addison-Wesley

[7] Amar Mukerjee*"Introduction to NMOS and CMOS VLSI System Design"* copyright © 1986 Prentice Hall Eglewood Cliffs, New Jersey

[8] Ajit Pal "Chap 2 MOS Fabrication Technology" in Low Power VLSI Circuit and System" copyright © 2015 by Springer India

[9] Carver A. Mead and Lynn A. Conway *"Introduction to VLSI System"* copyright © 1978 by C. Mead and L. Conway

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