DESIGN AND IMPLEMENTATION OF DUAL SOFT CORE PROCESSOR IN FPGA FOR FAULT TOLERANT APPLICATION IN NUCLEAR POWER PLANT

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***Abstract*—Mitigation of transient hardware faults in FPGA requires measures, either in pure software that results in runtime and memory overhead or specific hardware design approach like full or partial duplication of functionalities resulting in an area overhead. In this paper, duplication of CPU using standard soft-core processor and implementation in FPGA for fault-tolerant applications in nuclear power plant is proposed. The combination of FPGA technology and soft processor cores has the potential to allow the integration of system design into a single FPGA device. They can be also combined in one chip, leading to less power consumption, simpler board layout and fewer problems with signal integrity and EMI (electromagnetic interference).This combination can provide previously unavailable design options. Paper work aims towards the realization of a dual core processor on FPGA**

I. INTRODUCTION

The paper aims to find the transient fault in Nuclear Power Station where the data is in high back ground radiation. The data were handled in two sets of soft core processor. Any fault occurs in the first core it automatically changes in another core. In nuclear reactor the data are very vital. The data may be affected by delayed neutrons or by photons and other radiation to take care the reliability system is high.

The transient fault may occur due to the external and radiation effect. A transient fault is a fault that is no longer present if power is disconnected for a short time. Many faults in overhead power lines are transient in nature. At the occurrence of a fault power system protection operates to isolate area of the fault. A transient fault will then clear and the power line can be returned to service.

The dual core processor will help to increase the processor speed. The combination of FPGA technology and soft processor cores has the potential to allow the integration of system design into a single FPGA device. They can be also combined in one chip, leading to less power consumption, simpler board layout and fewer problems with signal integrity and EMI (electromagnetic interference).

A single event upset (SEU) is a change of state caused by ions or electro-magnetic radiation striking a sensitive node in a micro-electronic device, such as in a microprocessor, semiconductor memory, or power transistors. The state change is a result of the free charge created by ionization in or close to an important node of a logic element (e.g. memory "bit"). The error in device output or operation caused as a result of the strike is called an SEU or a soft error.

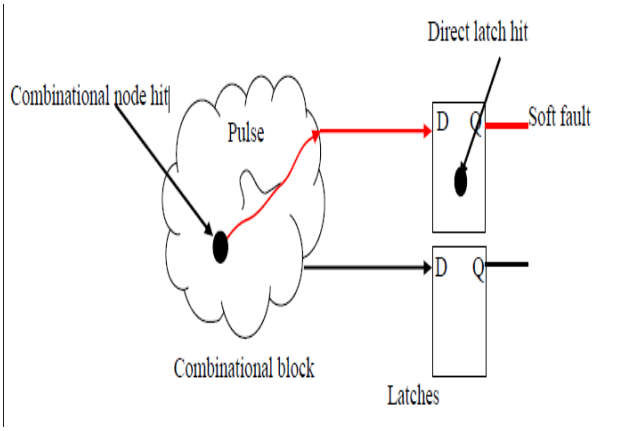
The SEU itself is not considered permanently damaging to the transistor's or circuits' functionality unlike the case of single event latch up (SEL), single event gate rupture (SEGR), or single event burnout (SEB). These are all examples of a general class of radiation effects in electronic devices called single event effects.

II. RADIATION FAULT

In nuclear reactor, radiation affects the performance of the system. The system components may be affected by radiation present in the reactors. It also depends on whether the system component is nearer or farer to the radiation. The types of radiation are Heavy ions, Protons, Alpha, Neutron, Gamma, and Beta.

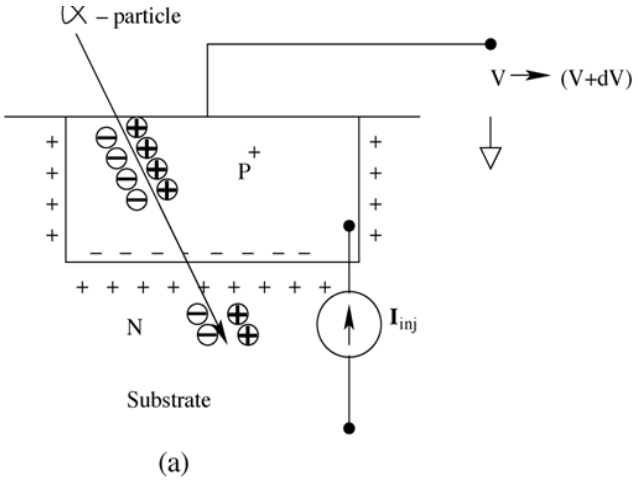
Due to this radiation, the system may be affected by following faults are Combinational node hit, Direct latch hit Direct latch hit are the soft faults that occur when the ionizing particle strikes the latch directly, thus flipping the output instantly.

Combinational node hit are when the ionizing particle strikes a combinational node, it generates a transient noise pulse. Depending on logical, temporal or electrical masking, if this pulse is travels through its propagation path and gets latched at the output of the latch, it results in a soft fault.



III. TRANSIENT FAULT

Transient fault is temporary fault which occur due to radiation or any other external action. If the transient fault occurs means it will causes the loss in the nuclear power plant. Transient fault may occur in the shorter period



IV. DUAL CORE PROCESSOR

In this paper, duplication of CPU using standard soft-core processor and implementation in FPGA for fault-tolerant applications in nuclear power plant is discussed. The combination of FPGA technology and soft processor cores has the potential to allow the integration of system design into a single FPGA device.

They can be also combined in one chip, leading to less power consumption, simpler board layout and fewer problems with signal integrity and EMI (electromagnetic interference).The soft core is CPU core. The CPU consists of the following blocks .They are Memory, Data fetch, Instruction decoder, Execution, Write back, Control

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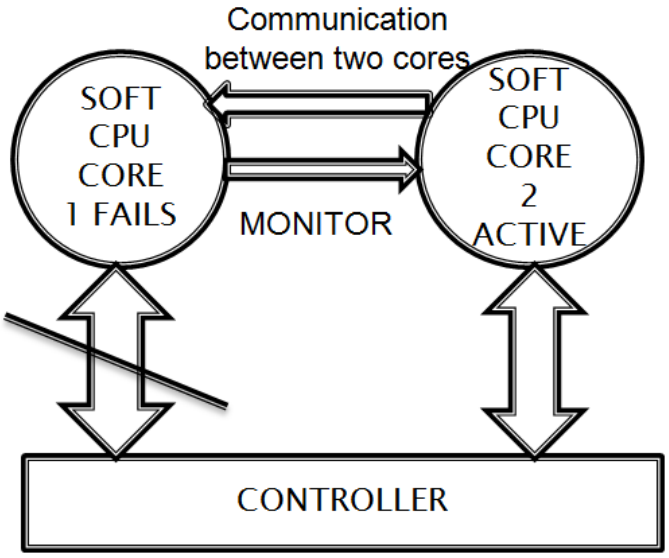
V. PPROPOSED SYSTEM

The general block diagram is shown in figure 4.1. In this project, two soft cores are considered. The soft core may be any core. In this project, a CPU cores is assumed. As the fault occurs in one soft core, the controller is changed to another core. Soft core can work in two modes. One is parallel and another is sequential.

In parallel mode, two cores work simultaneously. In sequential hardware if one soft core fails, the another core gets the information like memory status, data etc. and execute it. In this project, parallel mode operation is to be used in second phase.

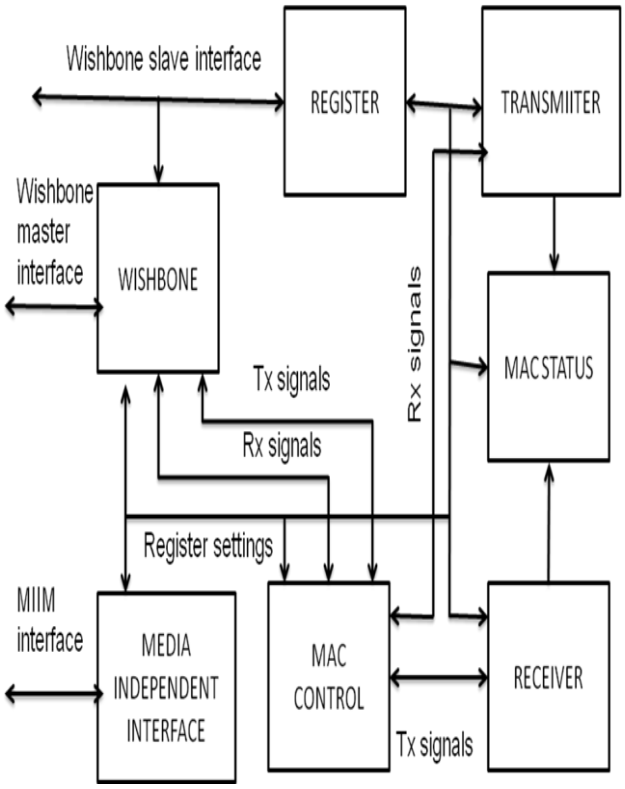


VI. ETHERNET CONTROLLER

The Ethernet IP Core is a MAC (Media Access Controller). It connects to the Ethernet chip on one side and to the WISHBONE SoC bus on the other. The core has been designed to offer as much flexibility as possible to all kinds of applications.

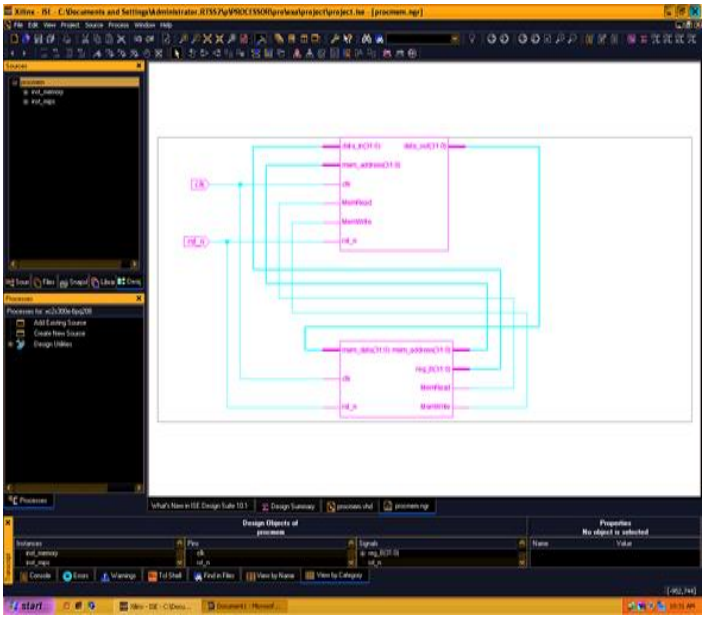
The features of Ethernet are Performing MAC layer functions of IEEE 802.3 and Ethernet, Automatic 32-bit CRC generation and checking, Delayed CRC generation, Preamble generation and removal, Automatically pad short frames on transmit, Detection of too long or too short packets (length limits),Possible transmission of packets that are bigger than standard packets, Full duplex support, 10 and 100 Mbps bit rates supported, Automatic packet abortion on Excessive deferral limit, too small inter packet gap, when enabled, Flow control and automatic generation of control frames in full duplex mode (IEEE 802.3x) ,Collision detection and auto

retransmission on collisions in half duplex mode (CSMA/CD protocol), Complete status for TX/RX packets, IEEE 802.3 Media Independent Interface (MII), WISHBONE SoC Interconnection Rev. B2 and B3 compliant interface, Internal RAM for holding 128 TX/RX buffer descriptors, Interrupt generation an all events.

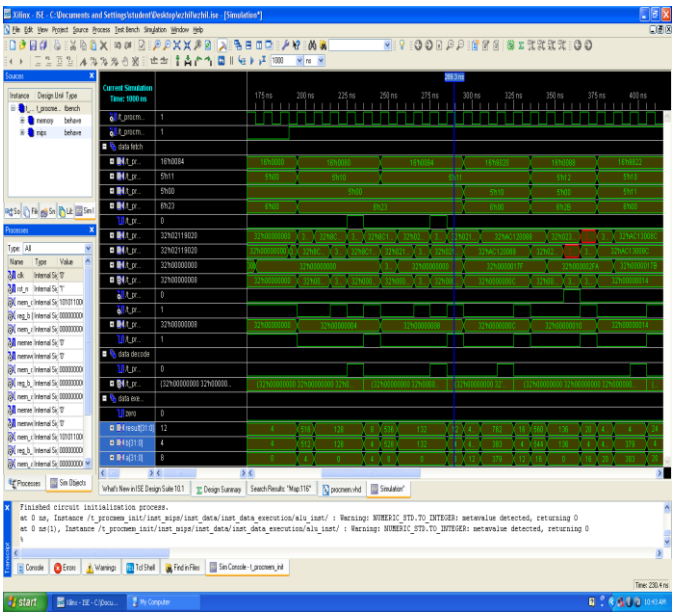


VII. SIMULATION SNAPSHOT

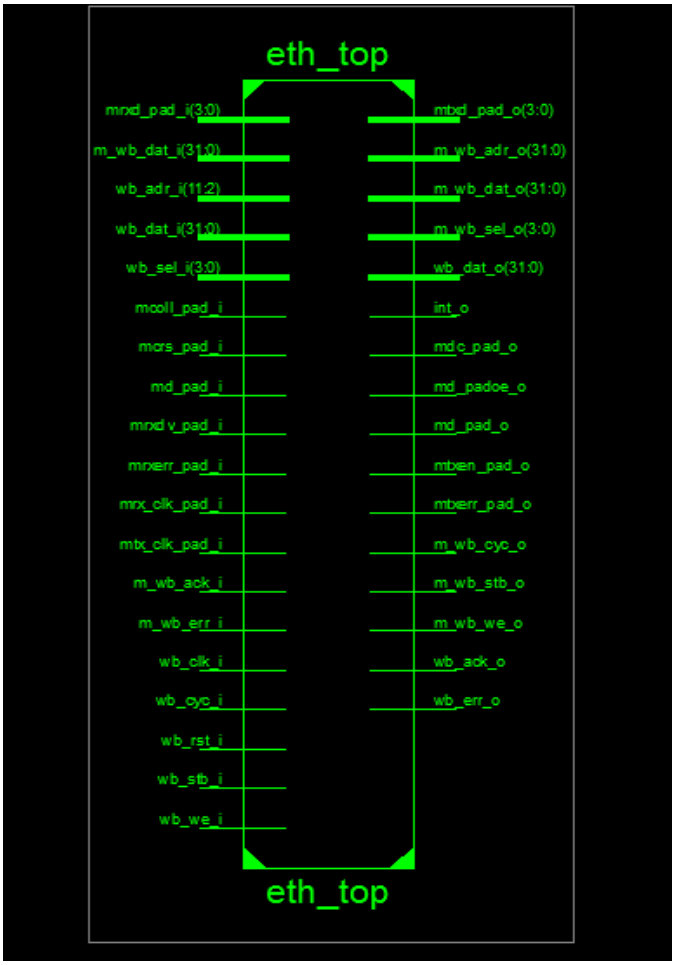
Below shows the RTL of whole CPU core



Below is the simulation result of the CPU core



Below shows the RTL of Ethernet IP Core



VIII. APPLICATION

The dual soft core can be used for many applications where fault occurs. In this paper the application used is sodium pump out in nuclear plant.

IX. CONCLUSION

In this paper the soft core processor was designed and results are verified using simulation. The soft core is just a CPU core. The core consists of so many units like decoder, execution, fetch etc. The duplication of soft core was designed, implemented and check whether the core is changed from one to another when a fault occurs

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